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Fast Bus Voltage Control of Single-Phase Grid-Connected Converter With Unified Harmonic Mitigation

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ABSTRACT This paper presents a comprehensive analysis of the harmonic sources of the single-phase grid-connected voltage source converter (VSC), which leads to an alternative approach for DC bus voltage control of the VSC under grid voltage distortion with a significant switching dead time. A selective current harmonic controller with the zero-reference structure plays a vital role in rejecting the harmonic components in the grid reference current created by the bus voltage control loop and the harmonic components in the grid voltage and in the VSC caused by the switching dead time. Therefore, the bus voltage control can adopt a conventional proportional-integral regulator tuned at a fast bandwidth. The proposed control scheme implemented in the multiple unbalanced synchronous reference frames was validated with a bidirectional 2-kV A VSC under grid voltage distortion and a significant dead time. Furthermore, the proposed control scheme exhibited the transient response and grid current quality superior to the conventional bus voltage control methods with a notch filter and a low-pass filter. The proposed control scheme has inherent frequency adaption.

INDEX TERMS Current distortion, dead time, double-frequency ripple, renewable energy.

I. INTRODUCTION Single-phase voltage source converters (VSCs) are widely used for grid integration of renewable energy sources [1], [2], [3], [4], battery storage systems [5], railway traction systems [6], and on-board battery chargers of plug-in vehicles [7], [8]. Fig. 1 depicts a typical application of the VSC, where the DC bus voltage $v_D(t)$ usually connects to a DC-DC converter or a 3-phase VSC. The control system of such VSCs generally comprises the cascade configuration with the outer DC bus voltage control loop and the inner grid current control loop. The main control objectives are to have low bus voltage fluctuation and fast transient response under a sudden change in the bus power, and low grid current distortion. However, the distorted grid reference current $i_g^*(t)$, the distorted voltage $v_{pcc}(t)$ at the point of common coupling (PCC), and the VSC terminal voltage $v_c(t)$ distorted by a dead-time voltage $v_{DT}(t)$, introduce harmonic components in the grid current $i_g(t)$.

The presence of the double-frequency ripple in the DC bus voltage control loop distorts the reference current for the grid current control loop. The distorted reference current is conventionally minimized by tuning the bus voltage at a bandwidth much lower than the double frequency, says 10 Hz [2]. So, bulky aluminum electrolytic capacitors are used to limit large bus voltage transient fluctuation. In addition, active ripple cancellation circuits [9], [10] decoupled the pulsating power from the average power, which resulted in a lower bus capacitance and a higher loop bandwidth. However, these techniques require extra semiconductor switches, additional passive components, and additional control schemes.

The ripple voltage can be permitted to reduce the bus capacitance [11]. Thus, increasing the bandwidth of the bus voltage control loop decreases the transient voltage fluctuation. Furthermore, distortion in the reference
current is generally minimized by blocking the ripple voltage into the bus voltage control loop. The most common solution is a notch filter to block the double-frequency ripple [1], [12], [13], [14], [15]. Alternative methods are adaptive bus voltage control [16], ripple voltage estimators [17], [18], nonlinear observers [19], and bus voltage sampling synchronized with the grid frequency [20]. Thus, these approaches create a clean reference current with a fast DC bus voltage control.

The harmonic voltages also cause grid current distortion at the PCC and the VSC terminals due to a dead time $T_D$. Feedforward of the PCC voltage partly mitigates the grid current distortion [22]. However, a DC offset in the voltage measurement induces an undesirable DC component injecting to the grid [23]. The dead-time effect is highly nonlinear, depending on the VSC current direction. The dead-time voltage can be minimized by the compensated duty ratio calculated from an adaptive algorithm [24] or an immune algorithm [25]. The PCC and dead-time harmonic voltages are the grid current control loop’s disturbances, which can be mitigated by using a grid current controller with selective harmonic mitigation. Multi-frequency synchronous reference frame controllers [22], multi-frequency proportional-resonant controllers [22], [26], [27], and repetitive controllers (RC) were proven to be effective solutions [21].

To this end, the grid current problems due to the distorted reference current and the harmonic voltages have yet to be considered simultaneously. The bus voltage control schemes in [12], [13], [14], [16], [17], [18], [19], and [20] were carried out under a sinusoidal voltage with negligible dead time. Meanwhile, a sinusoidal reference was applied to the current control loop under the grid voltage harmonics [21], [22] and the dead-time voltage compensation schemes [21], [22], [24], [25], which do not guarantee a sinusoidal grid current with the bus voltage control loop. Therefore, we present a comprehensive analysis of the current harmonic sources of the single-phase grid-connected VSC, which results in an alternative approach to the VSC bus voltage control under a distorted PCC voltage and a significant VSC dead time. This study adopts the unbalanced synchronous reference frame current controller [28] with the zero-reference configuration of selective harmonic compensators for simultaneous attenuation of the harmonic components in the reference current, PCC voltage, and VSC terminals due to the dead time.

With this current control structure, a conventional proportional-integral (PI) regulator can be applied for the bus voltage control. The proposed control structure allows the bandwidth of the DC bus voltage control loop to increase without sacrificing the grid current quality. The proposed control methodology was validated with a single-phase 2-kVA LCL-filtered VSC with a dual active bridge (DAB) DC-DC as the second stage converter, which was compared with the existing control methods under grid frequency variation, distorted grid voltage, and a significant dead time.

II. SYSTEM DESCRIPTION AND ANALYSIS OF HARMONIC SOURCES

A 2-kVA LCL-filtered grid-connected VSC shown in Fig. 2 with the parameters summarized in Table 1 is selected in this study. According to the grid current notation, the VSC is operated as the rectifier mode. The DC bus is connected to a DAB DC-DC converter as the second-stage converter for interfacing with a 400-V bidirectional DC source. This
A. GRID CURRENT DISTORTION DUE TO VOLTAGE HARMONICS

Fig. 3 shows the VSC’s grid current control block diagram in the stationary reference frame. The distorted PCC voltage $v_{\text{pcc}}(t)$ is considered in this study, which is written by

$$v_{\text{pcc}}(t) = \hat{V}_1 \cos \theta + \sum_{h=2}^{n} \hat{V}_h \cos (h \theta + \psi_h) \quad (1)$$

where $\theta = \omega t$, $\hat{V}_1$, and $\hat{V}_h$ are the voltage amplitudes, and $\psi_h$ is the phase angle of each harmonic component. The current controller $G_{c}(s)$ can be a proportional-resonant (PR) regulator in the stationary reference frame or a PI regulator in the synchronous reference frame, which provides an infinite gain at the grid frequency $\omega$ for a zero steady-state error. The LCL filter governs the grid current $i_g(t)$ as follows.

$$L_2 \frac{d^2 i_g(t)}{dt^2} + R_2 i_g(t) = v_{\text{pcc}}(t) - v_f(t) \quad (2)$$

$$v_f(t) = v_{\text{cf}}(t) + R_f (i_g(t) - i_1(t)) \quad (3)$$

$$C_f \frac{dv_{\text{cf}}(t)}{dt} = i_g(t) - i_1(t) \quad (4)$$

$$L_1 \frac{di_1(t)}{dt} + R_1 i_1(t) = v_f(t) - \left( \frac{v_{\text{c}}(t) + v_{\text{DT}}(t)}{v_c(t)} \right) \quad (5)$$

Neglecting the switching frequency components, the VSC ideal output voltage $v_{\text{c}}(t)$ in (5) is controlled through the modulation signal $m^*(t)$ given by

$$v_{\text{c}}(t) \approx V_{D} m^*(t). \quad (6)$$

Equations (2)-(6) illustrate that the grid current $i_g(t)$ is controlled through the modulation signal $m^*(t)$ with $v_{\text{pcc}}(t)$ and $v_{\text{DT}}(t)$ as the disturbances, which will introduce low-order harmonics into the grid current. The dead-time voltage $v_{\text{DT}}(t)$ in (5) can be approximated by

$$v_{\text{DT}}(t) \approx \frac{2 T_{\text{SW}}}{T_{\text{SW}}} \text{sign}(i_1(t)) v_D(t) \quad (7)$$

where $T_{\text{SW}}$ is the switching period. This $v_{\text{DT}}(t)$ can be compensated in $m^*(t)$ using (7). However, for the LCL filter with the grid current feedback control used in this study, an additional current sensor is required for the dead time voltage compensation. A feedforward of $v_{\text{pcc}}(t)$ mitigates the grid current distortion to some extent [22]. However, there can be a DC offset in the voltage measurement, inducing a DC component in the grid current [23].

B. GRID CURRENT DISTORTION DUE TO THE BUS VOLTAGE CONTROL

Fig. 4 depicts the simplified block diagram of the bus voltage control loop, where the grid current control loop is approximated as a unity gain. The bus voltage $v_D(t)$ passes through the bus voltage filter $G_{fb}(s)$ to compare with the reference bus voltage $V_D^*$ for the bus voltage controller $G_{cv}(s)$. The bus voltage filter can be a low-pass filter or a notch filter tuned at 2$\omega$. A PI regulator is normally employed as the bus voltage controller. The bus voltage controller generates the reference current $i_{gq}^*$ representing the required active power drawn from/injected into the grid. The reference current $i_{gq}^*$ is used to set the reactive power. The reference currents $i_{gd}^*$ and $i_{gq}^*$ are multiplied by $\cos \theta$ and $\sin \theta$ templates obtained from a phase-locked loop (PLL), forming the reference signal $i_{g}^*$ for the inner current control loop.

Let us consider that the grid current $i_g(t)$ initially consists of a DC component $i_{g0}$ and the AC fundamental component $AC i_{g1}(t)$ in this analysis. The grid current $i_g(t)$ is given as

$$i_g(t) = i_{g0} + \frac{I_1 \cos (\theta + \phi_1)}{i_{g1}(t)} \quad (8)$$

where $\hat{I}_1$ and $\phi_1$ are the amplitude and phase angle of $i_{g1}(t)$. Asymmetry in semiconductor properties, gate driver delays, and an offset in the grid current measurement cause the DC component current $i_{g0}$ [29]. The grid current $i_{g1}(t)$ can be decomposed into the active and reactive power-producing components $i_{g}(t)$ and $i_{q}(t)$, as given by

$$i_{g1}(t) = \frac{\hat{I}_1 \cos \phi_1 \cos \theta - \hat{I}_1 \sin \phi_1 \sin \theta}{i_{gd}} \quad (9)$$
With the fundamental component of the PCC voltage, the instantaneous grid power can be written as follows

\[ P_g(t) = \frac{1}{2} I_1 \cos \phi_1 + \frac{\dot{V}_1 I_{DCg} \cos \theta}{P_{g1}} + \dot{V}_1 I_{DCg} \cos \theta \]

(10)

The instantaneous grid power consists of the average power \( P_{g1} \) and the oscillating power components \( \dot{p}_{g1}(t) \) and \( \dot{p}_0(t) \) due to the AC and DC components of the grid current. Neglecting losses in the LCL filter and VSC, the power balance at the DC bus can be written as

\[ V_D(t) \left( \frac{dV_D(t)}{dt} \right) = P_g(t) - P_D(t) \]

(11)

where \( P_D(t) \) is the bus output power feeding the DAB DC-DC converter. Assume \( V_D(t) \) is tightly regulated around the reference value \( V_D^* \) [19]. Therefore, the linearization of (11) yields

\[ V_D^* \left( \frac{dV_D(t)}{dt} \right) \approx p_g(t) - P_D(t) \]

(12)

The bus voltage \( V_D(t) \) consists of the average value \( V_D(t) \) and the ripple component \( \tilde{V}_D(t) \) as given by

\[ V_D(t) = V_D(t) + \tilde{V}_D(t). \]

(13)

Thus, substitution of (10) and (13) into (12) results in the average and oscillating components as follows.

\[ V_D^* \left( \frac{dV_D(t)}{dt} \right) \approx \dot{V}_1 I_{DCg} \cos \theta \]

(14)

\[ V_D^* \left( \frac{dV_D(t)}{dt} \right) \approx \dot{p}_{g1}(t) + \dot{p}_0(t). \]

(15)

Note that the dynamic of the average bus voltage (14) is accurate when the loop bandwidth is less than the oscillating frequency components. The oscillating powers \( \dot{p}_{g1}(t) \) and \( \dot{p}_0(t) \) lead to an approximation of the bus voltage ripple as

\[ \tilde{V}_D(t) \approx \frac{1}{V_D^*} \int \left( \dot{p}_{g1}(t) + \dot{p}_0(t) \right) dt \]

\[ V_D(t) \approx \frac{\dot{V}_1 I_1}{4\omega C_D V_D} \sin (2\theta + \phi_1) + \frac{\dot{V}_1 I_{DCg} \cos \theta}{\omega C_D V_D} \]

(16)

The oscillating power component \( \dot{p}_{g1}(t) \) causes the 2\( \omega \) ripple component \( \tilde{v}_{2\omega}(t) \), and the \( \omega \) component \( \tilde{v}_{\omega}(t) \) is due to \( I_{g0} \). These two ripple components pass through the bus voltage control loop. Then, the bus voltage controller \( G_{e_w}(s) \) creates the reference current \( i_{e_w}(t) \) as

\[ i_{e_w}(t) = I_1 \cos \phi_1 + I_{np2} \cos (2\theta + \psi_2) + I_{np1} \cos (\theta + \psi_1) \]

\[ i_{e_w}(t) = i_{e_w}(t) \cos \theta + i_{e_w}(t) \sin \theta \]

(17)

where the ripple components \( \tilde{i}_{g2\omega}(t) \) and \( \tilde{i}_{g2\omega}(t) \) in \( i_{e_w}(t) \) are the residues from the bus voltage regulator. The bus voltage control loop governs the amplitudes \( I_{np2} \) and \( I_{np1} \), and phase angles \( \psi_2 \) and \( \psi_1 \). The reference grid current is given by

\[ i_g(t) = i_e(t) \cos \theta + i_e(t) \sin \theta \]

(18)

Substitution of (17) into (18) results in

\[ i_g(t) = I_1 \cos \phi_1 + I_{np2} \cos (2\theta + \psi_2) + I_{np1} \cos (\theta + \psi_1) \]

\[ i_g(t) = i_g(t) \cos \theta + i_g(t) \sin \theta \]

(19)

The desired components of \( i_g(t) \) are the first two terms in (19). The 2\( \omega \) ripple component creates the 3rd harmonic and additional reactive power components, which are generally attenuated by a low-bandwidth bus voltage control loop [2] or by a notch filter. The DC component \( I_{g0} \) of the grid current causes the DC and 2nd harmonic components in \( i_g(t) \). This DC component \( I_{g0} \) can be minimized by carefully calibrating the grid measurement. Suppression techniques with additional circuits provide an online adjustment of the DC component [29].

### III. ANALYSIS OF HARMONIC MITIGATION TECHNIQUES

#### A. HARMONIC REJECTION ANALYSIS OF THE GRID CURRENT CONTROL LOOP

Fig. 5 shows the equivalent grid current control block diagram in the stationary reference frame. The LCL filter’s transfer functions \( G_{LCL}(s) \) and \( G_{FW}(s) \) are given by

\[ G_{LCL}(s) = \frac{sC_f R_f + 1}{C_f L_1 L_2 s^3 + C_f (L_1 + L_2) R_f s^2 + C_f (L_1 + L_2) s} \]

(20)

\[ G_{FW}(s) = \left( \frac{C_f L_1 s^2}{C_f R_f s + 1} + 1 \right) \]

(21)

where \( L_1, L_2, C_f, \) and \( R_f \) are the LCL filter parameters. The VSC’s ideal voltage \( v_{cl}(t) \) is obtained from the pulse width modulation (PWM) with the modulation signal \( m^s(t) \) from the current controller output. The transfer function of the PWM process is modeled as

\[ G_{PWM}(s) = \frac{v_{cl}(s)}{m^s(s)} = V_D e^{-sT_d} \]

(22)
where $T_d = 2T_s$ is the delay time caused by the sampling process and transport delay [30], with $T_s$ as the sampling period. The current controller $G_{ci}(s)$ can be a proportional-resonant (PR) regulator in the stationary reference frame or a proportional-integral (PI) regulator in the synchronous reference frame.

$$G_{ci}(s) = K_{p1} + \frac{K_{i1}s}{s^2 + \omega^2}$$  \hspace{1cm} (23)

where $K_{p1}$ and $K_{i1}$ are the controller gains. The closed-loop transfer function of the grid current controller is given by

$$G_{cl}(s) = \frac{i_p(s)}{i_g(s)} = \frac{G_{ci}(s) G_{PWM}(s) G_{LCL}(s)}{1 + G_{ci}(s) G_{PWM}(s) G_{LCL}(s)}$$  \hspace{1cm} (24)

The current controller $G_{ci}(s)$ in (23) has an infinite gain at the grid frequency $\omega$, which forces $|G_{ci}(j\omega)| \approx 1$. Meanwhile, the controller’s finite gain at the frequencies $2\omega$ and $3\omega$ still partly tracks the $2\omega$ and $3\omega$ components of $i_g^*(t)$ in (19). The admittances $Y_{DT}(s)$ and $Y_{pcc}(s)$ represent the influence of the dead-time and PCC voltages on the grid current as follows

$$Y_{DT}(s) = \frac{i_p(s)}{v_{DT}(s)} = \frac{-G_{LCL}(s)}{1 + G_{ci}(s) G_{PWM}(s) G_{LCL}(s)}$$  \hspace{1cm} (25)

$$Y_{pcc}(s) = \frac{i_p(s)}{v_{pcc}(s)} = \frac{G_{FW}(s) G_{LCL}(s)}{1 + G_{ci}(s) G_{PWM}(s) G_{LCL}(s)}$$  \hspace{1cm} (26)

Equations (25) and (26) indicate that $G_{ci}(s)$ in (23) can reject only the fundamental components of $v_{DT}(t)$ and $v_{pcc}(t)$.

A feedforward of the PCC voltage optionally improves the dynamic performance and mitigation of the PCC voltage harmonics [22], as given by

$$Y_{pcc}(s) = \frac{i_p(s)}{v_{pcc}(s)} \approx \frac{(G_{FW}(s) - 1) G_{LCL}(s)}{1 + G_{ci}(s) G_{PWM}(s) G_{LCL}(s)}$$

### TABLE 2. Harmonic rejection characteristics of the grid current control structures.

<table>
<thead>
<tr>
<th>Transfer functions</th>
<th>Parallel HC structure in Fig. 6</th>
<th>Zero-reference HC structure in Fig. 7</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_{cl}(s) = \frac{i_p(s)}{i_g(s)}$</td>
<td>$\frac{(G_{cl}(s) + G_{PWM}(s) G_{LCL}(s))}{1 + G_{ci}(s) G_{PWM}(s) G_{LCL}(s)}$</td>
<td>$\frac{(G_{cl}(s) + G_{PWM}(s) G_{LCL}(s))}{1 + G_{ci}(s) G_{PWM}(s) G_{LCL}(s)}$</td>
</tr>
<tr>
<td>$Y_{DT}(s) = \frac{i_p(s)}{v_{DT}(s)}$</td>
<td>$\frac{-G_{LCL}(s)}{1 + G_{ci}(s) G_{PWM}(s) G_{LCL}(s)}$</td>
<td>$\frac{-G_{LCL}(s)}{1 + G_{ci}(s) G_{PWM}(s) G_{LCL}(s)}$</td>
</tr>
<tr>
<td>$Y_{pcc}(s) = \frac{i_p(s)}{v_{pcc}(s)}$</td>
<td>$\frac{G_{FW}(s) G_{LCL}(s)}{1 + G_{ci}(s) G_{PWM}(s) G_{LCL}(s)}$</td>
<td>$\frac{G_{FW}(s) G_{LCL}(s)}{1 + G_{ci}(s) G_{PWM}(s) G_{LCL}(s)}$</td>
</tr>
</tbody>
</table>

### FIGURE 5. Equivalent grid current control block diagram in the stationary reference frame.

### FIGURE 6. Grid current control with parallel HC scheme.

### B. UNIFIED HARMONIC MITIGATION STRUCTURE

Mitigation of the voltage harmonics typically adopts a plugged-in harmonic compensator (HC) $G_{cih}(s)$, of which transfer function in the stationary reference frame is given by

$$G_{cih}(s) = \sum_{h=3}^{n} \frac{K_{ih}s}{s^2 + (h\omega)^2}$$  \hspace{1cm} (28)

where $K_{ih}$ is the controller gain at the harmonic order $h$. This HC $G_{cih}(s)$ can be realized from PI controllers in the multiple-synchronous reference frame, proportional-multi-resonant (PMR) regulators, and repetitive controllers, which exhibit sufficient large gains at the selected frequencies. Fig. 6 shows the typical parallel HC structure of the grid current control with a harmonic controller in the stationary reference frame. The outputs $m_{cl1}^*$ and $m_{cl2}^*$ of the fundamental and harmonic controllers form the modulation signal $m^*$. Equations (29)-(31) in Table 2 summarize the harmonic responses of this parallel structure. Equation 29 indicates that this structure tracks the harmonic components of the reference current $i_g^*(t)$ at the selected frequencies thanks to the HC’s large gains. The large gains of HC attenuate the harmonic components of the PCC and dead-time voltages, as indicated in (30) and (31) [22].

Fig. 7(a) depicts an alternative grid current control structure. This control structure is equivalent to Fig. 7(b), where the reference signal for the selective harmonic controller is zero. The transfer functions of this zero-reference HC structure are summarized in (32)-(34) in Table 2. The large gains of HC at the selected frequencies simultaneously attenuate the harmonic components in $i_g^*(t)$, $v_{DT}(t)$, and $v_{pcc}(t)$. Furthermore, the parallel and zero-reference HC schemes
have identical rejection characteristics of the dead-time and 
PCC voltages, as indicated in (30) and (33), and (31) and 
(34). According to (32), the zero-reference HC scheme 
can increase the bandwidth of the conventional bus voltage 
control to improve the dynamic response and reduce the bus 
capacitance without restriction in grid current distortion. 
On the other hand, the existing bus voltage control schemes 
only focused on creating a clean reference for the grid current 
control loop.

IV. PROPOSED VSC CONTROL SCHEME

A. UNBALANCED SYNCHRONOUS REFERENCE 
FRAME CONTROL

The unbalanced synchronous reference frame control [28] is 
chosen for the fundamental and harmonic component current 
control. Fig. 8 depicts the stationary frame representation 
of the transfer function $H_{DC}(s)$ implemented on the syn-
chronous reference frame at host [31]. The error signals in 
the stationary reference frame $e_{\alpha}(t)$ and $e_{\beta}(t)$ derive from 

$$
\begin{bmatrix}
e_{\alpha}(t) \\
e_{\beta}(t)
\end{bmatrix} = 
\begin{bmatrix}
x_{\alpha\text{ref}}(t) \\
x_{\beta\text{ref}}(t)
\end{bmatrix} - 
\begin{bmatrix}
x_{\alpha}(t) \\
x_{\beta}(t)
\end{bmatrix}
$$  
(35)

where $x_{\alpha}(t)$ and $x_{\beta}(t)$ are the controlled signals, and $x_{\alpha\text{ref}}(t)$ 
and $x_{\beta\text{ref}}(t)$ are the reference signals in the $\alpha\beta-$ axes. The 
error signals $e_{\alpha}(t)$ and $e_{\beta}(t)$ are transformed to the error 
signals $e_{d}(t)$ and $e_{q}(t)$ in the synchronous reference frame 
using the Park transformation as 

$$
e_{d}(t) + j e_{q}(t) = (e_{\alpha}(t) + j e_{\beta}(t)) e^{-j \omega_{0} t}.
$$  
(36)

For the single-phase application, the $\alpha-$component output 
$y_{\alpha}(s)$ is only considered. According to [31], the $\alpha-$component 
output $y_{\alpha}(s)$ is derived from the convolution and modulation 
properties of the Laplace transformation, which yields 

$$
y_{\alpha}(s) = \frac{1}{2} \{(H_{DC}(s + j \omega_{0}) + H_{DC}(s - j \omega_{0})) e_{\alpha}(s)
- \frac{1}{2} j \{(H_{DC}(s + j \omega_{0}) - H_{DC}(s - j \omega_{0})) e_{\beta}(s)\}.
$$  
(37)

Thus, substituting $H_{DC}(s) = K_{ib} / s$ and $e_{\beta}(t) = 0$ into (37), 
the equivalent transfer function in the stationary reference 
frame $H_{AC}(s)$ becomes 

$$
H_{AC}(s) = \frac{y_{\alpha}(s)}{e_{\alpha}(s)} = \frac{K_{ib}s}{s^{2} + (\omega_{0})^{2}}.
$$  
(38)

This so-called unbalanced synchronous reference frame 
control is equivalent to the resonant controller [28]. There are 
different control structures to make the error in the $\beta-$ axis 
zero $e_{\beta}(t) = 0$ with identical performance. Fig. 9 depicts 
the unified structure of the unbalanced synchronous reference 
control. The arbitrary signal $x_{\beta\text{ref}}(t)$ is used for the Park trans-
formations on the reference and feedback sides, which causes 
$e_{\beta}(t) = 0$. Fig. 10 portrays an implementation structure of 
the unbalanced synchronous reference frame control with the 
reference signals in the $dq-$ axes, where the reference signal 
in the $\beta-$ axis $x_{\beta\text{ref}}(t)$ is used as the orthogonal signal for the 
axis transformation of the feedback signal $x_{d}(t)$. The signal 
$x_{d}(t)$ and $x_{q}(t)$ in Fig. 10 are identical to those of the con-
ventional synchronous reference frame control in the steady 
state [28]. Meanwhile, Fig. 11 shows another implementation 
configuration of the unbalanced synchronous reference frame 
control with $x_{\alpha\text{ref}}(t)$ as the reference signal, where $e_{\beta}(t) = 0$. This structure is suitable for an AC reference signal such as
HCs. It has been proven that the error signals $e_d(t)$ and $e_q(t)$ in Fig. 9 are identical to those in Fig. 10 and Fig. 11, which yields a similar performance [28].

### B. PROPOSED BUS VOLTAGE CONTROL SCHEME

The existing bus voltage control methodologies of the single-phase VSC try to create a clean reference for the grid current control loop [12], [13], [15], [18], [20], [32]. This study proposes an alternative approach using a conventional bus voltage control system tuned at a fast bandwidth. However, this makes the grid reference current $i_{g}^{*}(t)$ distorted. So instead, we employ the current control with zero-reference HC scheme in Fig. 7(a) as the main mechanism for simultaneous attenuation of the harmonic components in the grid reference current $i_{g}^{*}(t)$, PCC voltage $v_{pcc}(t)$, and VSC’s dead-time voltage $v_{DT}(t)$.

Fig. 12 shows the proposed bus voltage control scheme of the VSC. The bus voltage control loop applies a conventional PI regulator. The bus voltage passes through the low-pass filter $G_{fv}(s)$ given by

$$G_{fv}(s) = \frac{1}{T_f s + 1}.$$  (39)

Note that $G_{fv}(s)$ is used for loop shaping, not for attenuating the ripple component, which is explained in the controller design. The fundamental current control system $G_{ci}(s)$ adopts the unbalanced synchronous reference frame with the reference current in the $\beta$-axis $i_{g}^{\beta}(t)$ as the orthogonal signal for the Park transformation, which is simplified from Fig. 10. This configuration results in the virtual $\beta$-axis current error signal $e_{g}^{\beta}(t) = 0$. According to (37), the equivalent transfer function of the fundamental current control loop in the stationary reference frame is identical to (23). Moreover, this unbalanced synchronous reference frame control configuration has intrinsic frequency adaptation and power extraction capabilities.

The harmonic current controller $G_{cih}(s)$ is plugged into the fundamental current control $G_{ci}(s)$. This current control structure is equivalent to Fig. 7(a). Fig. 13 illustrates the implementation of $G_{cih}(s)$, where each harmonic component is simplified from the unbalanced synchronous reference frame control in Fig. 11. The transfer function of each harmonic order is equivalent to (28). Therefore, the proposed fundamental and harmonic current controllers in Fig. 12 are equivalent to the stationary reference frame current control system in Fig. 7(a). Note that this configuration of $G_{cih}(s)$ also exhibits inherent frequency adaptability. The harmonic controllers, orders 3rd, 5th, 7th, 9th, 11th, and 13th were adopted. The second-order harmonic controller was also added to suppress the 2$\omega$ component of $i_{g}^{\beta}(t)$ caused by the DC component of the grid current as demonstrated in (19). Furthermore, multiple-resonant regulators with frequency adaptation can be employed as the harmonic controller to reduce the computational effort [22]. The inverse Park transformation PLL is used in this study [33].

The proposed control scheme is compared with the conventional control scheme as shown in Fig. 14 and the notch filter-based control as shown in Fig. 15, where only the fundamental component controller is adopted for the grid current control. Meanwhile, for the notch filter-based control scheme, the low-pass filter is replaced by the notch filter $G_{NF}(s)$ given by

$$G_{NF}(s) = \frac{s^2 + 4\omega_d^2}{s^2 + 2\omega_d s + 4\omega_d^2}.$$  (40)

where $\omega_d$ is the damping frequency. This notch filter blocks the 2$\omega$ component of the bus voltage.

### V. CONTROLLER DESIGN AND HARMONIC REJECTION ANALYSIS

#### A. GRID CURRENT CONTROLLER DESIGN

The LCL filter with the parameters listed in Table 1 has a resonant frequency $f_r$ of 5.03 kHz, and the control system operates.
The open-loop grid current control system is given by

\[ K_{ci} = \frac{\omega C_{max}}{10K_{p1}} \]  

(44)

at which \( \tan^{-1} \left( \frac{\omega_{ci, max} K_{p1}}{K_{i1}} \right) = 85^\circ \). A conservative phase margin of \( \phi_{mi} = 60^\circ \) was selected. With the parameters in Table 1 and \( T_d = 2T_s \), \( K_{p1} \) and \( K_{i1} \) were calculated from (43) and (44) with \( \omega_{ci, max} = 2, 222p \) rad/s. The integral gains \( K_{i2} \) of the harmonic controller should be selected lower or equal to (44) to create the corresponding negligible magnitude contributions at the cross-over frequency [27]. Thus, the integral gains were set as follows

\[ K_{i2} = K_{i3} = K_{i5} = K_{i7} = \frac{K_{i1}}{3} \]

(45)

With this set of harmonic gains, the phase margin reduces to \( \phi_{mi} = 43^\circ \) at the chosen cross-over frequency \( \omega_{ci} \), still large enough to guarantee stability, as shown in Fig. 16. The open-loop gains at the selected frequencies are lower than -100 dB, which attenuates the current error signal at such frequencies. Although the harmonic controller decreases the first harmonic gain, it is still large enough to track the fundamental component current with a zero steady-state error. The extended symmetrical optimum method [37] is adopted, which is proven to have a better transient response and lower grid current distortion [38] than the method in [2]. With this tuning method, the phase angle of the forward path reaches 43°.

The maximum cross-over frequency \( \omega_{ci, max} \) is obtained from [30]

\[ \omega_{ci, max} = \frac{\pi f_r}{2 - \phi_{mi}} \]  

(42)

where \( \phi_{mi} \) is the chosen phase margin. This \( \omega_{ci, max} \) leads to \( K_{p1} \) approximated as

\[ K_{p1} = \frac{\omega_{ci, max} L_s}{V_D} \]  

(43)

The value of \( K_{i1} \) is then determined from

\[ K_{i1} = \frac{\omega C_{max}}{10K_{p1}} \]  

The maximum cross-over frequency \( \omega_{ci, max} \) is obtained from [30]

\[ \omega_{ci, max} = \frac{\pi f_r}{2 - \phi_{mi}} \]  

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(45)

With this set of harmonic gains, the phase margin reduces to \( \phi_{mi} = 43^\circ \) at the chosen cross-over frequency \( \omega_{ci} \), still large enough to guarantee stability, as shown in Fig. 16. The open-loop gains at the selected frequencies are lower than -100 dB, which attenuates the current error signal at such frequencies. Although the harmonic controller decreases the first harmonic gain, it is still large enough to track the fundamental component current with a zero steady-state error. The open-loop system has multiple gain cross-over frequencies with the harmonic controller at the selected frequencies. However, the system stability is measured at the highest gain cross-over frequency [36]. Moreover, the two gain cross-over frequencies around the resonant frequency of the LCL filter with the phase margins \( \phi_{m1} = 43^\circ \) and \( \phi_{m2} = 189^\circ \) shown in Fig. 16 guarantee the stability criteria for the grid current feedback.

**B. BUS VOLTAGE CONTROLLER DESIGN**

Fig. 17 depicts the block diagram of the bus voltage control, simplified from Fig. 4. The grid current control loop is approximated as a unity gain, and the grid oscillating powers \( P_{g1}(t) \) and \( P_{g2}(t) \) are considered the disturbances. The extended symmetrical optimum method [37] is adopted, which is proven to have a better transient response and lower grid current distortion [38] than the method in [2]. With this tuning method, the phase angle of the forward path reaches 43°.

**FIGURE 14.** Conventional bus voltage control of the single-phase grid-connected VSC.

**FIGURE 15.** Notch filter-based bus voltage control of the single-phase grid-connected VSC.
the maximum at the cross-over frequency $\omega_{cv}$. The phase margin $\phi_{mv}$ is chosen from a constant $\beta$ as

$$\phi_{mv} = \tan^{-1} \left( \frac{\beta - 1}{2\beta^{1/2}} \right). \quad (46)$$

The recommended values of $\beta$ are from 4 to 16, which relates to $\phi_{mv}$ of $36^\circ$ to $60^\circ$. The PI controller parameters $K_{pv}$ and $K_{iv}$ and the low-pass filter time constant $T_f$ are co-designed from the desired bandwidth $\omega_{mv}$ as follows

$$T_f = \left( \frac{\sqrt{\beta \omega_{cv}}}{1} \right)^{-1} \quad (47)$$

The parameters obtained from (47) yield the closed-loop transfer function given by

$$\frac{V_p(s)}{V_d(s)} = \frac{\beta^{1/2} s/\omega_{cv} + 1}{s^2/\omega_{cv} + \beta^{1/2} s^2/\omega_{cv}^2 + \beta^{1/2} s/\omega_{cv} + 1}. \quad (48)$$

The bus voltage control loop was designed at $\omega_{cv} = 50\pi$ rad/s and $\beta = 5.83$ with $\phi_{mv} = 45^\circ$. This study compares the proposed control method with the conventional bus voltage control in Fig. 14 with $\omega_{cv} = 20\pi$ rad/s and $\omega_{cv} = 50\pi$ rad/s. The notch filter in Fig. 15 is simplified as the low-pass filter with $T_f = \omega_d/(2\alpha \omega)$ so that so that the above design method of the bus voltage control can be adopted. The notch filter $G_{NF}(s)$ tuned at $2\omega$ with $\omega_d = 140\pi$ rad/s has a frequency response below $2\omega$ close to a low-pass filter for $\omega_{cv} = 50\pi$ rad/s. Thus, $K_{pv}$ and $K_{iv}$ for the notch filter-based control can be adopted from the conventional control with $\omega_{cv} = 50\pi$ rad/s.

C. HARMONIC REJECTION ANALYSIS

Fig. 18 shows the closed-loop frequency response of the grid current control with the reference current plotted from (32). The closed-loop grid current system exhibits a unity gain with a zero-phase angle at the grid frequency, which provides a zero steady-state error. Meanwhile, the harmonic controller rejects the reference current at the selected frequencies. Fig. 19 illustrates the frequency responses of the admittances $Y_{DT}(j\omega)$ in (33) and $Y_{pcc}(j\omega)$ in (34). The proposed grid current control scheme with the harmonic controller $G_{cih}(s)$ rejects the disturbances from the dead-time voltage $v_{DT}$ and grid voltage $v_{pcc}$ at the fundamental and selected harmonic frequencies. On the other hand, the harmonic components of

VI. SIMULATION

A switched-circuit model of the VSC was developed in MATLAB/Simulink. Voltage harmonic orders $3^{rd}$ of 5%, order $5^{th}$ of 2%, and orders $7^{th}$, $9^{th}$, $11^{th}$, $13^{th}$ of 1% to the fundamental component of the PCC voltage were added. The added harmonics resulted in a total harmonic distortion (THD) of 5.74%. The dead-time voltage $v_{DT}(t)$ determined from (7) with $T_{DT} = 4\mu s$ was added to the VSC terminal voltage $v_{g}(t)$. The bus voltage control loop was tuned at a bandwidth of $50\pi$ rad/s with a PLL bandwidth of $20\pi$ rad/s. The VSC was simulated to operate in mode with the nominal bus power of $P_D = 2$ kW and $i_D^* = 0$ for a unity power factor.

Fig. 20 compares the steady state performance of the conventional control and the proposed control schemes under the sinusoidal PCC voltage in Fig. 20(a), the sinusoidal PCC voltage and the dead-time voltage in Fig. 20(b), the distorted PCC voltage in Fig. 20(c), and the distorted PCC and dead-time voltages in Fig. 20(d). The conventional control scheme’s grid current $i_{g}(t)$ under the sinusoidal PCC alone still distorts. Meanwhile, the proposed control method with HC rejects the harmonic contents in the reference current $i_D^*(t)$, as shown in Fig. 20(a). As a result, the distorted PCC and dead-time voltages heavily affect the grid current waveform with the conventional control scheme, as depicted in Fig. 20(b) to
voltages, (c) Distorted PCC voltage, (d) Distorted PCC with the dead-time
(a) Sinusoidal PCC voltage, (b) Sinusoidal PCC with the dead-time
harmonic voltage

Fig. 20 shows the transient response of the \( v_D(t) \) and \( i_D(t) \) under the distorted PCC voltage and \( T_{DT} = 1 \) ms when the output power changes from 2 kW to zero. The reference current \( i_D^*(t) \) in the discrete-time control system was sent to an embedded 12-bit digital to analog converter of the microcontroller with appropriate scaling. The proposed bus voltage control system compares the conventional control schemes tuned at \( \omega_{cv} = 20\pi \) rad/s and \( \alpha_{cv} = 50\pi \) rad/s and the notch filter-based control system tuned at \( \alpha_{cv} = 50\pi \) rad/s. The proposed control, 50\pi -rad/s conventional and notch filter-based control schemes, have voltage fluctuations of approximately 50 V and recover to the 400-V reference within two cycles. The experimental transient response agrees with the simulation result in Fig. 21. However, the 20\pi -rad/s conventional control gives rise to \( v_D(t) \) to 540 V. It takes ten cycles to go back to the 400-V reference, which temporarily forces the grid current control into the unstable range. Thus, the bus capacitance \( C_D \) should be increased for this 20\pi -rad/s conventional control scheme.

Fig. 24 compares the steady-state waveforms of \( v_{pcc}(t), v_D(t), i_D(t) \) and \( i_D^*(t) \) of different control schemes when the VSC operates in the rectifier mode with the output power of 2 kW under the sinusoidal PCC voltage and \( T_{DT} = 1 \) ms. Although the reference current \( i_D^*(t) \) of the proposed control system contains ripple components, the grid current waveform is still near sinusoidal. Meanwhile, \( i_D(t) \) under the 50\pi -rad/s conventional control scheme under the sinusoidal voltage is slightly distorted due to the ripple component of \( i_D^*(t) \). The 20\pi -rad/s conventional and notch filter-based control systems under the sinusoidal voltage create the clean reference current \( i_D^*(t) \), which also results in near sinusoidal grid currents.

B. EXPERIMENTAL RESULTS

Fig. 20(d). On the other hand, the proposed control method with HC forces the grid current to be near sinusoidal with the simultaneous presence of the dead-time voltage and PCC harmonic voltage \( v_h(t) \).

Fig. 21 depicts the transient response of the proposed bus voltage control system under the distorted grid voltage and dead-time voltage \( v_{DT}(t) \). The DC bus initially supplies a power of \( P_D = 2 \) kW. Although there is a \( 2\omega \) ripple component in the reference current \( i_D^*(t) \), the grid current \( i_D(t) \) remains sinusoidal similar to that in Fig. 20. At \( t = 0.2 \) s, \( P_D \) is removed, which behaves as a step load change. The bus voltage \( v_D(t) \) increases by approximately 50 V and recovers to \( V_D^* = 400 \) V within 50 ms.

VII. EXPERIMENTAL VALIDATION

A. EXPERIMENTAL SETUP

Fig. 22 illustrates the experimental setup of this study. The VSC and DAB DC-DC converter were assembled from Infineon FF50R12RT4 insulated-gate bipolar transistor (IGBT) modules with the control schemes implemented on a 32-bit TMS320F28379D microcontroller. Dead times of \( T_{DT} = 1 \) ms and \( T_{DT} = 4 \) ms in each VSC leg were adjusted on the microcontroller’s PWM outputs. A Chroma 61860 60-kVA grid simulator emulated the PCC voltage. The DC output voltage \( V_B \) for the DAB DC-DC converter was set at a constant voltage of 400 V using a Chroma 17020 bidirectional DC source. The output power was controlled in the range of \( \pm 2 \) kW through the angle \( \delta^* \) of the single phase-shift modulation implemented on the same microcontroller. The \( q \)-axis reference current was set at \( i_q^* = 0 \) for a unity power factor.

Chroma 61860 Grid Simulator
VSC and DAB DC-DC Converter
Chroma 17020 Bidirectional DC Source
Fig. 23. Transient response of the VSC when the output power changing from 2 kW to zero under the distorted PCC voltage and $T_{DT} = 1 \mu s$ ($v_{pcc}(t)$ and $v_{D}(t)$: 100 V/division, $i_{g}(t)$ and $i_{d}^{*}(t)$: 10 A/division).

Fig. 24. Steady state waveforms of the VSC with the output power of 2 kW under the sinusoidal PCC voltage and $T_{DT} = 1 \mu s$, $v_{g}(t)$ and $v_{D}(t)$: 100 V/division, $i_{g}(t)$ and $i_{d}^{*}(t)$: 10 A/division).

Fig. 25. Harmonic components of the VSC current with the output power of 2 kW under the sinusoidal PCC voltage with $T_{DT} = 1 \mu s$, and $T_{DT} = 4 \mu s$).

Fig. 25 compares the resultant harmonic components of the grid current under the sinusoidal PCC voltage with $T_{DT} = 1 \mu s$ and $T_{DT} = 4 \mu s$. The proposed bus voltage system effectively mitigates the grid current harmonics caused by the large dead time $T_{DT} = 4 \mu s$ with THD$_i = 1.85\%$ compared with THD$_i = 1.18\%$ for the short dead time $T_{DT} = 1 \mu s$. The current harmonics components under the two dead-time values are within the IEEE1547 standard. Although the 20$\pi$-rad/s conventional and notch filter-based control systems regulate the grid current with THD$_i = 1.40\%$.
FIGURE 26. Steady state waveforms of the VSC with the output power of 2 kW under the sinusoidal PCC voltage and $T_{DT} = 1 \mu s$, ($v_p(t)$ and $v_D(t)$: 100 V/division, $i_g(t)$ and $i_d^*(t)$: 10 A/division).

FIGURE 27. Harmonic components of the VSC current with the output power of 2 kW under the distorted grid voltage with $T_{DT} = 1 \mu s$ and $T_{DT} = 4 \mu s$.

FIGURE 28. THD values of the grid current with the output power under: (a) sinusoidal PCC voltage, and (b) distorted PCC voltage.

FIGURE 29. THD values of the grid current under sinusoidal PCC voltage and $T_{DT} = 1 \mu s$ at the output power of 2 kW with varied grid frequency.

For the distorted PCC voltage and the sizeable dead time $T_{DT} = 4 \mu s$ in Fig. 26, grid current distortion can be observed with the conventional and notch filter-based control schemes. The dead time mainly distorts $i_g(t)$ during the zero crossings [21]. The distortion due to the PCC voltage harmonics can be observed during the peaks of the current waveform. The harmonic controller $G_{cl} (s)$ of the proposed control scheme mitigates the harmonic disturbances due to the dead-time effect and PCC voltage. The grid current harmonics with the proposed control system under the distorted PCC voltage in Fig. 27 are very close to those under the sinusoidal voltage in Fig. 25, which confirms the effectiveness of the

and THD$_i = 1.84\%$, for $T_{DT} = 1 \mu s$, the two control schemes are affected by the dead-time voltage harmonics with the THD$_i$ approximately of 5% for $T_{DT} = 4 \mu s$. A large loop bandwidth does not attenuate the $\omega$ component in $v_D(t)$ caused by the DC component of $i_g(t)$. Therefore, the $2^{nd}$ harmonic component of the grid current is noticeable for the $50\pi$-rad/s conventional and notch filter-based control systems compared with the $20\pi$-rad/s conventional system. Meanwhile, the harmonic controller $G_{cl} (s)$ of the proposed control scheme successfully damp the $2^{nd}$ harmonic current.

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TABLE 3. Performance comparison of the proposed control schemes with the existing methods.

<table>
<thead>
<tr>
<th>Control schemes</th>
<th>Distorted PCC voltage</th>
<th>Large dead time</th>
<th>Fast bus voltage control</th>
<th>Frequency adaptation</th>
<th>Power extraction</th>
<th>2nd harmonic current</th>
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<td>Dead-time compensations [24, 25]</td>
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<td>Fundamental component + paralleled HC current control [21, 22, 27]</td>
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proposed harmonic mitigation structure. Meanwhile, the distorted PCC voltage adversely affects the grid current waveforms under the conventional and notch filter-based control schemes.

Fig. 28 compares the THD$_i$ values under the sinusoidal and distorted PCC voltages and the dead times of $T_{DT} = 1$ $\mu$s and $T_{DT} = 4$ $\mu$s with the output power of $\pm 2$ kW. The proposed bus control system exhibits the lowest THD$_i$ values. The difference is highly noticeable with PCC voltage harmonics and a significant dead time. Fig. 29 compares the current distortion under the sinusoidal voltage and $T_{DT} = 1$ $\mu$s with the output power of 2 kW with the allowable frequency between 47-52 Hz for Thailand’s grid. The proposed control system has inherent frequency adaptation. The detuned notch frequency causes THD$_i$ to vary with the grid frequency. The conventional control scheme with a bandwidth of 20$\pi$ rad/s, far below 2$\omega$, virtually has no impact on the grid frequency variation compared with the 50$\pi$-rad/s bandwidth.

Table 3 compares the performance of the proposed bus voltage control scheme with the existing VSC control methods. The power extraction in the table refers to the decomposition capability of the grid current. It indicates that the proposed methodology covers all the performance criteria, which has advantages over the existing methods.

VIII. CONCLUSION

Grid current control with selective harmonic mitigation is proposed for bus voltage control of the single-phase grid-connected VSC. Zero-reference current configuration of the harmonic controller rejects harmonic components in the grid reference current, VSC dead-time harmonics, and PCC voltage harmonics. Thus, a conventional bus voltage control with the proposed selective harmonic mitigation structure tuned at a fast bandwidth minimizes the bus capacitance without sacrificing the grid current quality. The proposed control scheme implemented in the unbalanced synchronous reference frame has superiority over the low-bandwidth conventional and notch filter-based control schemes as follows

1) Simultaneous rejection of harmonic components in the reference current, dead-time voltage, and grid voltage at the selected frequencies.
2) Second harmonic mitigation due to a DC component in the grid current.
3) Inherent frequency adaptation through the axis transformation.

REFERENCES


bus voltage controller for a grid-connected DC/AC converter,” IEEE Trans.


[22] S. Somkun and V. Chankung, “Improved DC bus voltage control of single-phase grid-connected converters with harmonic mitigation, power extraction and fre-


connected PWM inverters of single-stage PV systems,” IEEE Trans.


[37] S. Preitl and R.-E. Precup, “An extension of tuning rules after symmet-

[38] S. Somkun and V. Chankung, “Improved DC bus voltage control of single-
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