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Efficient surface passivation of black silicon using spatial atomic layer deposition

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Efficient surface passivation of black silicon using spatial atomic layer deposition

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In this work we show that surfaces of nanostructured silicon (black silicon, b-Si) can be passivated with Al_2O_3 using industrially viable line speeds in a prototype Spatial ALD reactor Beneq SCS 1000. Charge carrier lifetimes up to 1.25 ms were obtained, which were slightly higher than with temporal ALD passivation on similar wafers (0.94 ms).

1 Introduction

Black silicon (b-Si) has gained increasing amount of interest in photovoltaics due to the low reflectance and light trapping properties of the nanostructured silicon surface on a wide spectral range. The large surface area of b-Si leads to a high surface recombination velocity and, therefore, efficient surface passivation is of utmost importance in employing b-Si in photovoltaic devices. Usage of temporal ALD to coat b-Si surfaces with aluminum oxide (Al_2O_3) has already been demonstrated to provide efficient surface passivation [1,2]. ALD-passivated b-Si has been used as a material in record-breaking photovoltaic devices reaching efficiencies above 22 % [3].

Spatial ALD (SALD) is a modification of ALD aimed to increase the deposition rate of high-quality conformal coatings and to broaden the reach of ALD. In this study we evaluate its suitability for surface passivation of planar and nanostructured silicon and compare results to temporal ALD passivation.

Figure 1: Beneq SCS 1000 SALD reactor installed at the Beneq facilities in Espoo, Finland.

2 Experimental

For SALD experiments we used large-area sheet-to-sheet Beneq SCS 1000 reactor, presented in Figure 1, with various line speeds at 150°C. Temporal ALD passivation was realized with Beneq TFS 500 at 200°C [1]. In both cases TMA and H_2O were used as precursors and samples were double-side passivated with about 20 nm thick Al_2O_3 layers.

Float Zone wafers (p-type, 1 Ωcm, 4 inch, 250 μm) were used as substrates. b-Si surface was prepared on both sides of wafers using cryogenic deep reactive ion etching (ICP-RIE) with process parameters reported by Repo *et al.* in [1]. An SEM image of a typical b-Si surface is presented in Figure 2. Unetched planar wafers were coated as reference samples. Charge carrier lifetime τ was characterized using photoconductance method in the transient mode (WTC-120 Sinton Instruments).

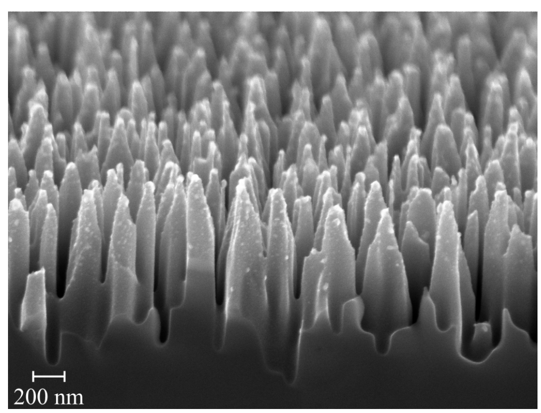

Figure 2: An SEM image of freshly etched b-Si surface.

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3 Results

The industrial feasibility of processing with the utilized SALD tool was evaluated by coating planar and b-Si substrates with line speeds of 1.5, 4.5 and 9 m/min. Growth per cycle ranged from 1.27 to 1.49 Å/c depending on the line speed. Comparison of τ for the samples is presented in Figure 3.

The highest lifetime for b-Si samples was obtained with the slowest line speed, 1.5 m/min (1.25 ms at an excess carrier density of 10^{-15} cm^{-3}). Also faster line speeds yielded efficient passivation with lifetimes in the same order of magnitude. As the highest lifetime was obtained with the slowest line speed, it is possible that the longer precursor exposure time provides a more uniform passivation layer than with higher line speeds. For planar samples the charge carrier lifetimes followed a different trend than for b-Si samples. The highest lifetime in planar substrates was obtained with 9 m/min, which yielded τ = 3.44 ms.

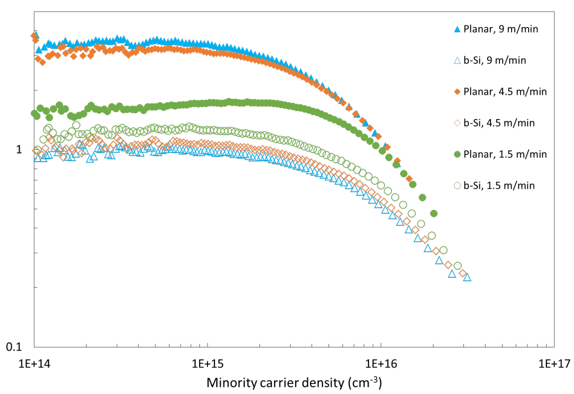

Figure 3: τ of planar and b-Si samples coated with SALD with different line speeds.

Processing with the prototype SALD tool was confirmed to be a viable technique for the surface passivation of both planar and b-Si surfaces. The highest charge carrier lifetimes were compared with the results obtained with temporal ALD. τ as a function of minority carrier density for SALD and for temporal ALD passivated wafers are presented in Figure 4. It can be seen that SALD passivation yields slightly higher τ in both planar and b-Si wafers.

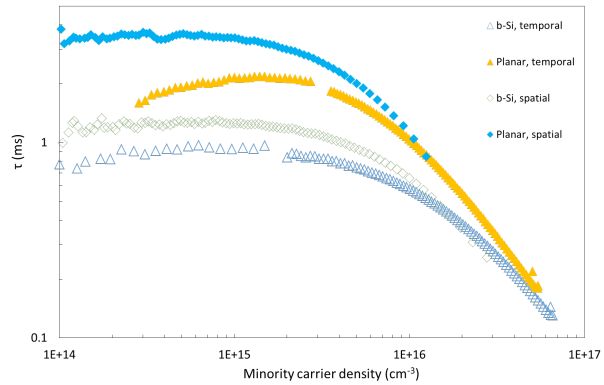

Figure 4: τ of planar and b-Si samples coated with SALD and temporal ALD.

4 Conclusions

We have shown that SALD can provide as efficient surface passivation of nanostructured silicon as temporal ALD. Results indicate that the conformal coating of high surface area structures such as b-Si is indeed feasible, and possibly even more efficient with SALD than with temporal ALD. Efficient passivation of both planar and b-Si substrates was achieved with all line speeds, even with 9 m/min, which demonstrates excellent process scalability and suitability for industrial-scale applications.

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References

[1] Repo P *et al.* Effective passivation of black silicon surfaces by atomic layer deposition. IEEE J Photovolt 2013;3:90-94.

[2] Repo P*et al.* Effect of different ALD Al_2O_3 oxidants on the surface passivation of black silicon. 6th International Conference on Silicon Photovoltaics, SiliconPV2016, Energy Procedia 2016;92:381-385.

[3] Savin H *et al.* Black silicon solar cells with interdigitated back-contacts achieve 22.1% efficiency. Nat Nanotech 2015;10:624-629.