Najmussadat, Md; Ahamed, Raju; Varonen, Mikko; Parveg, Dristy; Kantanen, Mikko; Halonen, Kari A.I.

220-240-GHz High-Gain Phase Shifter Chain and Power Amplifier for Scalable Large Phased-Arrays

Published in:
IEEE Access

DOI:
10.1109/ACCESS.2023.3253764

Published: 01/01/2023

Document Version
Publisher's PDF, also known as Version of record

IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 29 January 2023, accepted 26 February 2023, date of publication 6 March 2023, date of current version 13 March 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3253764

RESEARCH ARTICLE

220-240-GHz High-Gain Phase Shifter Chain and Power Amplifier for Scalable Large Phased-Arrays

MD. NAJMUSSADAT[1], RAJU AHAMED[1], MIKKO VARONEN[2], DRISTY PARVEG[2], MIKKO KANTANEN[2], AND KARI A. I. HALONEN[1]

[1]Department of Electronics and Nanoengineering, Aalto University, 02150 Espoo, Finland
[2]VTT Technical Research Centre of Finland Ltd., 02044 Espoo, Finland

Corresponding author: Md. Najmussadat (md.najmussadat@aalto.fi)

This work was supported by the Academy of Finland through the Project Compact Millimeter-wave Radiometers (MilliRAD) under Grant 314542, the Project TeraCOM under Grant 319681, and the Project Millimeter-wave Integrated Circuit Development for Earth Remote Sensing, Radio Astronomy and Imaging Applications (MIDERI) under Grant 310234.

ABSTRACT This paper focuses on the design aspects of the key components for a scalable phased-array system over the 200 GHz frequency range. A high-gain phase shifter chain for 220 to 240 GHz frequency range and a high-gain power amplifier (PA) with a high output power are designed in a 0.13-μm SiGe BiCMOS technology. The phase shifter chain includes a low-noise amplifier (LNA), a vector modulator phase shifter (PS), and a gain-enhancing amplifier. The LNA is a five-stage cascode design. The vector modulator core is realized by two variable gain amplifiers based on the Gilbert cell architecture. A four-stage cascode design is used for the gain-enhancing amplifier. The phase shifter chain shows a measured gain of 18 dB at 230 GHz with a 360° phase tuning range and more than 10 dB of gain control. The chip achieves a minimum measured noise figure of 11.5 dB at 230 GHz and shows a wideband noise characteristic. The complete phase shifter chain chip consumes a dc power of 153 mW and occupies a 1.41 mm^2 area. A high-power PA that is critical for a large phased-array system is designed. This paper presents a unique 4-way power combining technique utilizing a differential quadrature coupler. The realized balanced PA occupies an area of 0.67 mm^2 and shows a measured peak gain of 21 dB at 244 GHz. The PA consumes 819 mW of dc power and delivers a maximum saturated output power (P_{sat}) of 7.1 dBm at 244 GHz and more than 4.3 dBm of P_{sat} from 230 to 255 GHz.

INDEX TERMS Differential coupler, gain tuning, low-noise amplifier, millimeter-wave, MMIC, phased-array, phase shifter, power amplifier, receiver, transmitter.

I. INTRODUCTION

Millimeter wave (mm-wave) and terahertz (THz) bands are extremely interesting regions of electromagnetic radiation for applications such as security and medical imaging, space radiometry, and ultra-high-speed wireless communications [1]. In communications, the new standard from 5G and beyond emphasizes smaller cell sizes for wider data bandwidth per user and can feature wireless data rates of around 100 Gbit/s [2]. Even with a highly efficient modulation technique, a significant capacity increase to multi-gigabit or even terabit wireless transmission requires larger bandwidths. However, bandwidth is bounded due to extremely limited spectral resources in the conventional frequency range. Thanks to the 200-300 GHz frequency band that can offer advantages such as providing a smaller system size with a smaller antenna aperture, thus improving the resolution of the imaging system, as well as providing high absolute bandwidth for high-speed wireless communications [3].

Traditionally, THz and upper millimeter-wave frequency (200-300 GHz) front-end circuits and systems are mainly implemented using III-V compound semiconductor technologies [4], [5], [6], [7], [8]. Due to recent improvements in silicon-based technologies, both CMOS and BiCMOS offer

The associate editor coordinating the review of this manuscript and approving it for publication was Yiming Huo.

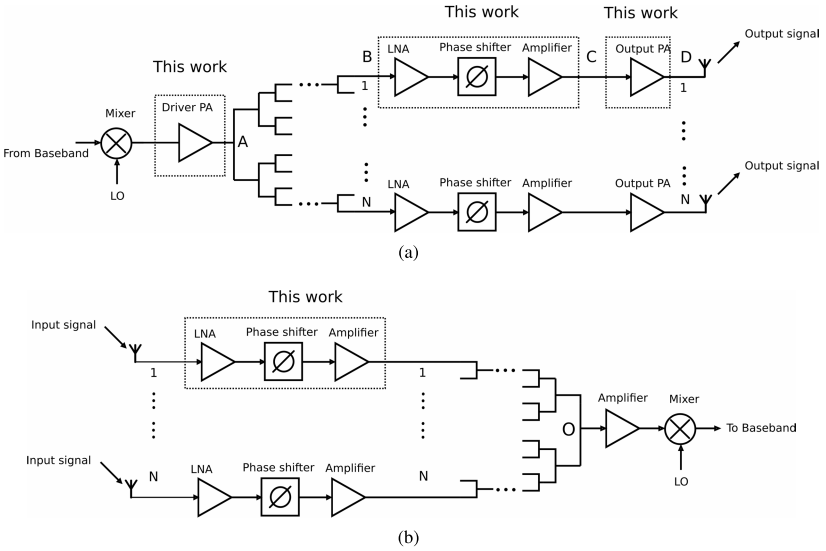


FIGURE 1. Block diagram of N-path phased-array system (a) transmitter and (b) receiver.

higher throughput and lower cost as compared to III-V processes, which enable the possibility of integrating circuits and systems at 200-300 GHz [9]. Recently, SiGe HBT with f_t of 300 GHz and f_{max} of 500 GHz has been presented in [10].

In the last decade, the number of circuits and systems in the 200-300 GHz using CMOS and BiCMOS has increased gradually. Several transceivers based on silicon technologies have been reported in different articles, such as a 220 and 320 GHz sub-harmonic receiver with integrated LO is presented in [11] and [12]. Also, a fully integrated CMOS transceiver in 65-nm CMOS for wireless chip-to-chip communication at 260 GHz has been presented in [13].

Although several transceivers have been demonstrated for frequencies from 200 to 300 GHz, designing a high data rate transceiver still remains a challenging task due to high path loss, a high noise figure(NF) of the receiver, and a low output power of the transmitter. A phased-array technique can be used to overcome these challenges at these frequencies. Along with beamforming, phased-arrays have the advantages of higher effective isotropic radiated power (EIRP) in the transmitter and a higher signal-to-noise ratio (SNR) in the receiver [14]. Recent works for phased-array system-on-chip around 100 GHz have been demonstrated in [15] and [16]. A 280-GHz power generation and beam-steering array are reported in [17]. In [8], a 320-GHz 1×4 fully integrated phased-array transmitter using SiGe BiCMOS technology is demonstrated. A 220-250 GHz four-element RF phase-shifting array is presented in [18]. However, quite a few phased-array circuits are reported that could be used to demonstrate a large array in 200-300 GHz.

The main challenge with a large phased-array system at higher mm-wave frequencies is the lack of output power required to drive a large number of arrays in the transmitter and achieve a low noise figure with high gain in the receiver. Although the performance of both CMOS and BiCMOS has improved in recent years, the gain at higher frequencies remains very limited. So, it is evident that for building a large phased-array receiver system, the phase-shifting path needs to have a high gain and a low noise figure to have better performance as a receiver. Again, the phase-shifting path needs to provide high output power for building a large phased-array transmitter system.

This work presents a high-gain phase shifter (PS) chain circuit suitable for a large phased-array system that includes a low-noise amplifier, a phase shifter, and an amplifier at 220-240 GHz. This phase shifter chain can be used both in the transmitter and the receiver. Moreover, a separate power amplifier can be added to this PS chain if more transmit power is needed when it is used as a transmitter. The phase shifter circuit achieves a high gain of 28 dB at 220 GHz. At 230 GHz, it shows a gain of 18 dB with a 360° phase tuning range and 10 dB of gain control with a noise figure of 11.5 dB. This work also presents a power amplifier that uses a unique power combination technique at 240 GHz and can be used with the phase shifter chain circuit to provide high output power. The power amplifier shows a measured peak gain of 21 dB and a P_{sat} of 7.1 dBm at 244 GHz and delivers a saturated power above 4.3 dBm from 230-255 GHz.

This paper starts with a detailed overview of how the designed phase shifter chain circuit and power amplifier can be used to build a large RF phase-shifting transmitter and receiver system in Section II. Section III describes the circuit design of individual blocks and the measurement results of the phase shifter chain. In Section IV, the detailed design procedure and the measurement results of the power amplifier are presented followed by the conclusion in Section V.

II. SYSTEM OVERVIEW

Phase shifters are essential components in a phased-array system. A phased-array system consists of several antennas

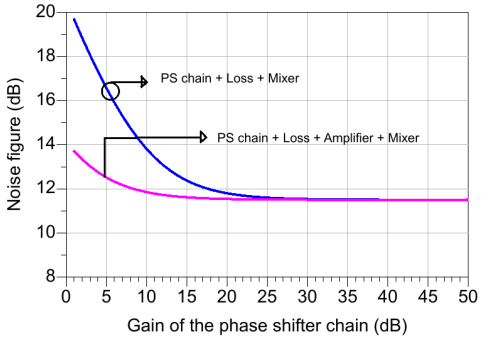


FIGURE 2. Noise figure variation with the gain of the phase shifter (PS) chain.

that can direct the beam in a specific direction. By providing high gain and high output power in the phase shifter path, a large phased-array system can be built. Fig. 1 shows a block diagram of the proposed N-path transmitter and receiver RF phase-shifting system based on the designed phase shifter chain and power amplifier. In both the transmitter and the receiver, the same phase shifter chain is used.

Fig. 1a represents the N-path RF phase-shifting transmitter. Each path consists of a phase shifter chain and a separate PA for high output power to the antenna. All the N-paths are connected to point A in Fig. 1a and are driven by a driver PA. In this proposed architecture, the same circuit is used as output PA and driver PA. In the case of an N-way split from point A to point B, the power at point B is 10·log(1/N) dB less than the power at point A. Depending on the increase or decrease of N, the power difference between points A and B will increase or decrease, respectively. Mathematically, if the power at point D is P_D, the gain of the output PA is G_{PA} and the gain of the PS chain is G_{PS}, then the power at point B is:

$$P_B = P_D - G_{PA} - G_{PS} \tag{1}$$

From equation (1), it is seen that if the G_{PA} and G_{PS} are higher, then the required power at point B is decreased. It is found from our PA design and also from literature [19] that a +5 dBm output power from PA is feasible in the 225-250 GHz range. In the RF phase-shifting transmitter path, if we want to feed the antenna with a +5 dBm power, then the power at point D will be +5 dBm. If the gain of the output PA (G_{PA}) is 20 dB, then the required power at point C is −15 dBm. Again, if the gain of the phase shifter chain (G_{PS}) is 18 dB, the power needed at point B will be −33 dBm. Now, if we want to build a 1024-element RF phase-shifting transmitter array with −33 dBm power at point B, the required power at point A will be +2 dBm according to the calculation of N-way splitting and considering a typical power division ratio of 3.5 dB from a 2-way splitter [18] around 230 GHz. So, if we use a PA that can deliver +5 dBm output power as the driver PA then it will drive the 1024-element RF phase-shifting transmitter array according to our calculation. Otherwise, if the gain of the phase shifter chain (G_{PS}) and gain of the PA (G_{PA}) are very low, then we need a very high power driver PA, which is difficult to realize at 220-250 GHz for a similar number of elements in the RF phase-shifting transmitter array.

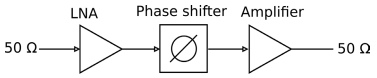


FIGURE 3. Block diagram of the phase shifter chain circuit.

Fig. 1b shows an N-path RF phase-shifting receiver system where all the RF paths are combined at point O. In this architecture, the gain and noise figure of the phase shifter chain define the number of paths that can be connected. The number of parallel paths can be connected as long as the total noise figure does not degrade compared to the noise figure of a stand-alone phase shifter chain. Considering all the losses of the combiner and adding an amplifier and mixer after point O, the total noise figure of the system can be calculated according to Friis's formula for noise factor as in equation (2).

$$F_{total} = F_{PS} + \frac{L-1}{G_{PS}} + \frac{F_A - 1}{G_{PS} \cdot L} + \frac{F_{Mix} - 1}{G_{PS} \cdot L \cdot G_A} \tag{2}$$

Here, F_{PS} and G_{PS} are the noise factor and the gain of a single phase shifter path, respectively. L represents the total loss due to the RF power combiners. F_A and G_A are the noise factor and gain of the amplifier, and F_{Mix} is the noise factor of the mixer after point O. Fig. 2 shows the simulated noise figure for different gains for a single phase-shifter chain considering the loss of combining the 1024 paths and the characteristic of the mixer at 240 GHz as in [20]. From Fig. 2, it is found that the NF of the receiver system remains similar to the stand-alone phase shifter chain if the phase shifter chain can provide more than 20 dB gain, and the NF of the system will degrade by around 5 dB if the gain of the single phase shifter chain drops from 20 dB to 5 dB. Again, it is also seen from Fig. 2 that if we add a high-gain amplifier as in [21] after point O, then it can reduce the gain requirement of a single phase shifter chain and thus significantly reduce the power consumption of the RF phase shifting receiver system. So, from the analysis, it is evident that a large receiver array is possible if the phase shifter path can provide a high gain and a low noise figure.

III. PHASE SHIFTER CHAIN

The phase shifter chain consists of an LNA and phase shifter followed by a gain-enhancing amplifier. The block diagram of the phase shifter chain is given in Fig. 3.

A. LNA DESIGN

Since the LNA is the first block in the receiver chain, the gain and noise figure of the LNA play a critical role in determining the noise figure of the whole receiver system. Therefore, low noise figure and high gain are major requirements for the LNA design over the frequency band of interest.

Common emitter (CE) and cascode topologies are the most popular topologies for LNA design. It has been seen that

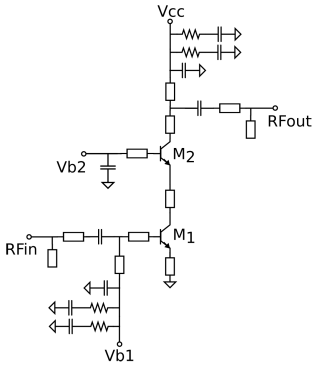


FIGURE 4. A simplified schematic of single stage of the cascode LNA.

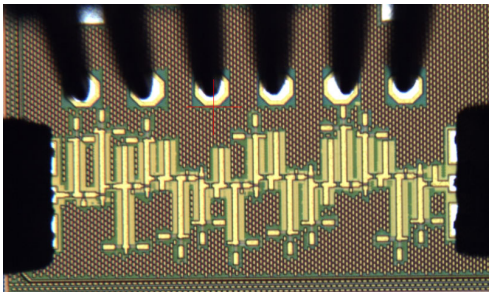


FIGURE 5. Die micrograph of the 7-stage LNA.

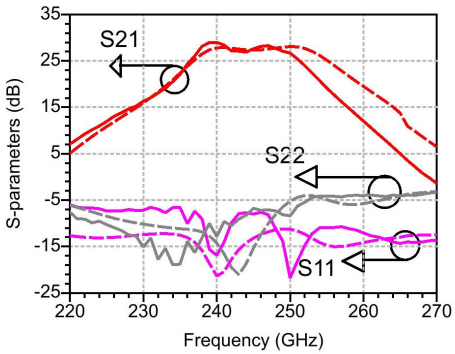


FIGURE 6. S-parameter results of the 7-stage LNA. Solid lines represent the measured data. The dashed line represents simulated values.

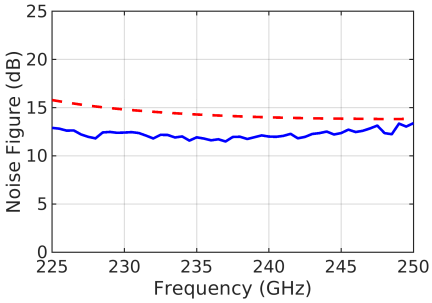


FIGURE 7. Noise figure of the 7-stage LNA. Solid lines represent the measured data. The dashed line represents simulated values.

a CE topology can provide a lower noise figure compared to common-base (CB) and cascode topologies. However, at frequencies close to f_t and f_{max}, the gain of the CE amplifiers drops significantly. Usually, cascode amplifiers provide higher gain but have a degraded noise figure compared to a CE amplifier. It is seen in [21] that the noise figure is almost 2 to 2.5 dB better in CE at 220-260 GHz compared to cascode topology. However, cascode's maximum available gain (MAG) becomes significant (6 to 7 dB higher MAG compared to a CE). Also, if we compare the NF of a cascode to the NF of a two-stage CE, the NF is only 1 to 1.2 dB higher in a cascode. Therefore, the cascode topology was chosen for this design since the cascode topology provides better performances in terms of gain, isolation, and 3-dB bandwidth for the given technology.

The design goal for the LNA was to find the transistor size for low noise figure and higher gain. Source impedance points for minimum noise figure for different transistor sizes in a single-stage cascode amplifier were examined for choosing the correct size. In this technology, it is seen that a transistor with an emitter size of $6 \times (0.90 \times .07)\ \mu\text{m}^2$ provides a better source impedance point with higher gain for better matching. Based on this transistor size, we have designed a stand-alone 7-stage prototype LNA. Fig. 4 shows the schematic of a single stage of the designed LNA. In this 7-stage amplifier, the bias connections for the V_{cc} V_{b2} and V_{b1} are provided separately. The detailed design of the 7-stage LNA can be found in [21]. Fig. 5, Fig. 6 and Fig. 7 show the chip photograph, S-parameters, and noise figure of the 7-stage LNA, respectively. The chip size is 0.45 mm^2. The 7-stage LNA achieves a measured gain of 28.5 dB and 11.7 dB of measured noise figure at 237 GHz. The comparison of the LNA with other published LNAs could be referred to in [21]. This LNA demonstrates the highest gain and highest figure of merit in terms of GHz/mW in the frequency range of 240 GHz.

In the phase shifter chain LNA design, the transistors were optimized with high bias compared to the prototype 7-stage LNA, and bias was realized with current mirror biasing. As a result, a high gain could also be obtained if we reduced the number of amplifying stages compared to the stand-alone 7-stage LNA. Also, because we have a gain amplifier after the phase shifter in the phase shifter chain, the gain requirement from the LNA can be relaxed because LNA and gain-enhancing amplifier can now control the overall gain of the chain. Considering these facts and the reduced chip area, a 5-stage cascode design was chosen for the LNA in the phase shifter chain.

Every cascode stage schematic in this 5-stage LNA is similar to the schematic shown in Fig. 4, with each transistor having an emitter size of $6 \times (0.90 \times .07)\ \mu\text{m}^2$. For optimization, the source impedance was selected for a low noise figure in the first stage and for a higher gain in the other stages. The output impedance of each stage was transformed into the source impedance of the next stage in such a way that the first stage could provide a low noise figure and other stages could provide a higher gain. In this way, all five stages

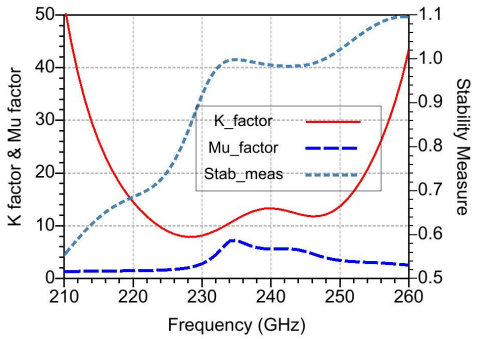


FIGURE 8. Simulated stability analysis of the LNA for the phase shifter chain.

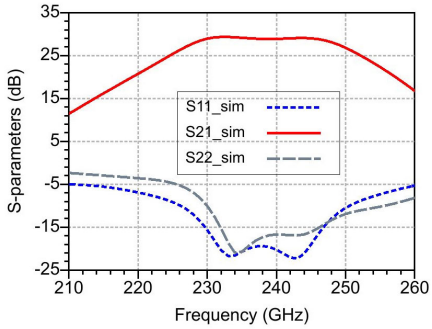


FIGURE 9. Simulated S-parameter result of the LNA for the phase shifter chain.

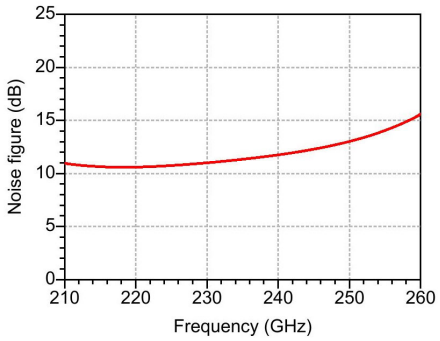


FIGURE 10. Simulated noise figure of the LNA for the phase shifter chain.

were optimized for higher gain while maintaining a low noise figure. The input matching, interstage matching, and output matching were realized by transmission lines and capacitors. A transmission line, equivalent to a series inductance, has been placed between the CE and CB stages in the cascode for gain enhancement and improving the NF of the amplifier.

All the transmission lines, capacitors, and other connections were EM simulated for the post-layout simulation results. The unconditional stability of the amplifier was checked by stability factor (K) simulation. Fig. 8 shows the overall amplifier's simulated stability analysis. The simulated K factor value was greater than 1 in the 1-300 GHz range, which indicates the unconditional stability of the designed

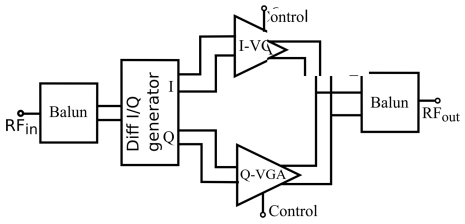


FIGURE 11. Simplified block diagram of the phase shifter.

five-stage cascode LNA. We also simulated the stability measure (B1) and Mu factor, which ensure the stability of the 5-stage LNA.

The 5-stage LNA occupies an area of 0.29 mm^2. Fig. 9 and Fig. 10 show the post-layout simulation result of S-parameters and noise figure of the 5-stage LNA, respectively. The bias current is 35 mA from a 3.4 V supply. From Fig. 9, it is found that 5-stage LNA has a peak gain of 28 dB, and input and output matching are better than 10 dB from 230-250 GHz. The simulated NF of the 5-stage LNA has a good match with the measured NF of the 7-stage LNA.

B. PHASE SHIFTER DESIGN

The simplified block diagram of a vector modulator phase shifter is shown in Fig. 11. The RF input signal is converted to a differential signal using a Marchand balun. A differential signal is fed to the differential I/Q generator. A compact, low-loss, and wideband differential coupler is used as the differential I/Q generator in this work. The differential I/Q generator creates differential in-phase and quadrature signals. The differential I and Q signals are fed to the differential VGAs. The differential output is the vector sum of the outputs of I and Q VGAs. The differential signal is converted back to a single-ended signal by a Marchand balun.

Although the Marchand balun is generally large, it was employed because of its wideband characteristics. The structure is made smaller by bending the lines. Thus, it becomes feasible to use this balun in our design. The Marchand balun is made of two sections of coupled lines, each with a length of $\lambda/4$ at the design frequency. The topmost metal layer is used to realize the Marchand balun, and metal 3 is used as the ground plane. A 3D layout view of the Marchand balun is shown in Fig. 12. The Marchand balun is designed and optimized for a 50 Ω system with ADS momentum. The optimized line spacing and width are 2 μm and 7 μm, respectively. The simulation results are shown in Fig. 13. The balun provides less than 0.6 dB of amplitude mismatch from 200 GHz to 260 GHz and less than 1° of phase imbalance from 200 GHz to 280 GHz.

A low-loss, compact, and wideband differential coupler operating from 180 GHz to 280 GHz is used as the differential I/Q generator in the phase shifter. The physical implementation of the differential coupler is shown in Fig. 14. A differential signal is fed to Port 1, and I/Q output signals are taken from Port 2 and Port 3. The detailed design of the wideband

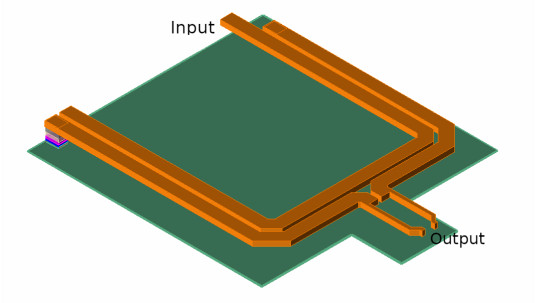


FIGURE 12. 3D layout view of the Marchand balun realized by the topmost metal layer.

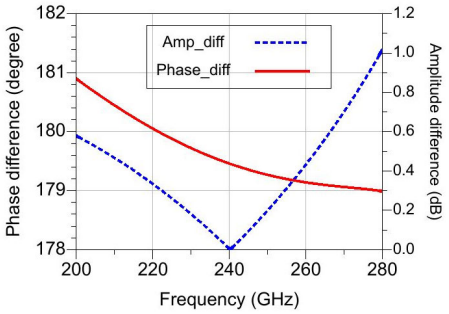


FIGURE 13. Simulated phase and amplitude differences of the Marchand balun.

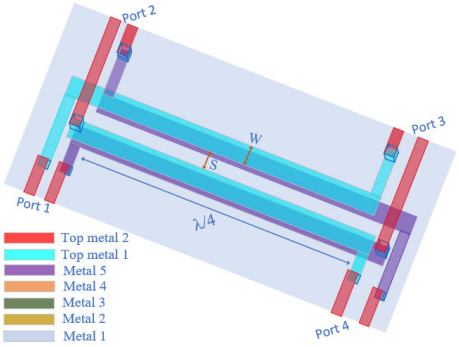


FIGURE 14. Physical construction of the differential I/Q coupler with solid ground beneath the structure.

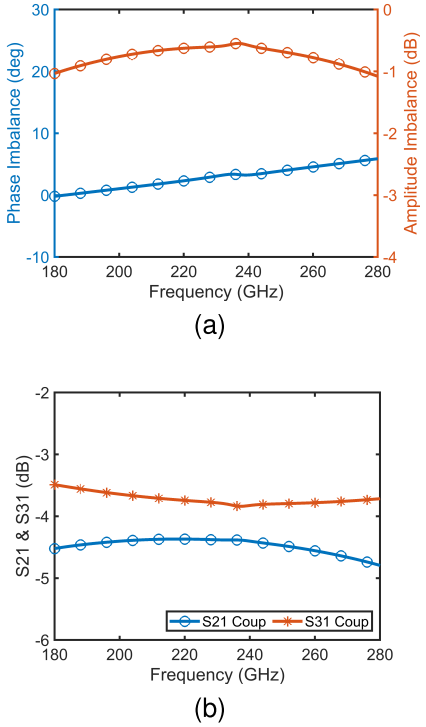


FIGURE 15. (a) Amplitude and phase imbalance of the differential coupler. (b) S_{21} and S_{31} of the differential coupler.

differential coupler is presented in [22]. The main design parameters used to estimate the dimension of the differential coupler are the width of the conductors W, the spacing between the adjacent lines S, and the line length L. Top metal 1 and metal 5 layers are used to realize the coupler. A solid metal layer is placed beneath the whole coupler so that the structure is not exposed to the lossy silicon substrate. After simulation and optimization, the values are finally found to be W $= 4$ μm, S $= 11$ μm, and L $= 160$ μm. The realized coupler shows a very wideband response. The simulated results are shown in Fig. 15. The coupler shows less than 1 dB of amplitude imbalance from 180 GHz to 280 GHz and less than 5° of phase imbalance from 180 GHz to 260 GHz.

The vector modulator consists of two identical VGAs. The VGA is designed based on the Gilbert-cell topology. The vector modulator core is shown in Fig. 16. In this configuration, the gain of the differential I signal is controlled by the analog control signals (V_{c1}, V_{c2}). Transistors (M_3-M_6) are used for the gain control stage of the Gilbert cell. Input transistors M_1 and M_2 work as a transconductance stage. The input of the Gilbert cell is matched to the output of the differential coupler by a 100 Ω differential transmission line, TL_1. TL_2- TL_5 are small lines for connecting the transistors. The I and Q signals with variable amplitudes are combined to obtain the desired signal through a symmetrical matching network that consists of differential transmission lines TL_7-TL_{11}. The differential lines TL_7 and TL_{11} combine the I and Q signals by reactive matching. TL_9 is a quarter-wave short-circuited transmission line that is used for biasing. TL_8 and TL_{10} work as interconnects and form a matching network with capacitor C_3 that matches the impedance of the Marchand balun. The vector modulator draws 15 mA from a 3.5-V supply.

A stand-alone compact and wideband vector modulator phase shifter operating from 200 GHz to 250 GHz is designed separately for testing the phase shifter. The chip micrograph of the stand-alone phase shifter is shown in Fig. 17. It occupies a core area of 0.09 mm^2. This phase shifter is measured separately, and a detailed measurement procedure can be found in [22]. Fig. 18 shows the measured and simulated S-parameters of the designed phase shifter. Simulated and measured S-parameters are in fairly close agreement with

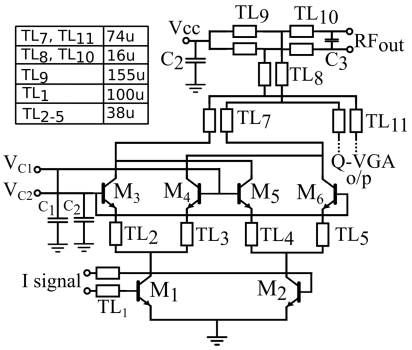


FIGURE 16. Simplified block diagram of the vector modulator core. Identical Q VGA is not shown.

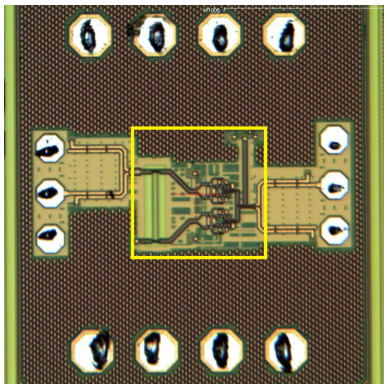


FIGURE 17. Die micrograph of the phase shifter chip.

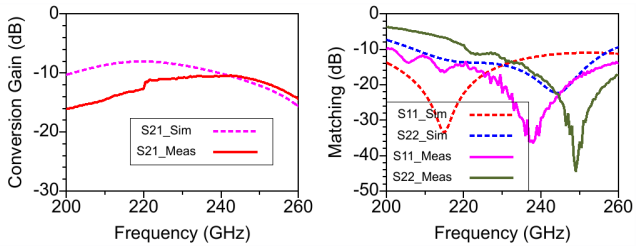


FIGURE 18. Measured (solid) and simulated (dashed) S-parameters of the phase shifter for the maximum gain setting.

each other. The measured conversion gain of the phase shifter is −10.3 dB for the maximum gain setting at 230 GHz with a 3-dB bandwidth of 40 GHz. Both input and output matching are better than 10 dB from 220 GHz to 260 GHz. Fig. 19 shows the measured polar plot of the S_{21} at 230 GHz. The phase shifter shows 360° phase control and 10 dB of gain control. The maximum gain with a full 360° phase control range is −17 dB. Other measured and simulated results of this phase shifter and a comparison of the performance of this phase shifter with that of other published phase shifters in the same frequency range can be found in [22]. This stand-alone phase shifter shows very wideband performance and uses an I/Q generator, which is the best I/Q generator considering the area, loss, and bandwidth.

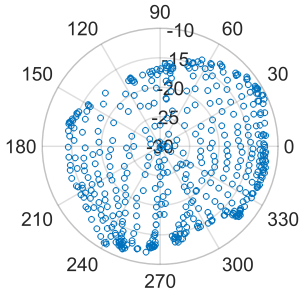


FIGURE 19. Polar plot of the measured S_{21} of the phase shifter at 230 GHz.

C. GAIN ENHANCING AMPLIFIER DESIGN

In order to compensate for the losses introduced by the phase shifter and also to further increase the gain and output power capability of the phase shifter chain, an amplifier is designed and placed after the phase shifter. Fig. 20 shows the schematic of the amplifier. The amplifier consists of four cascode stages with different transistor sizes in each stage. The first two stages are optimized for higher gain, and the last two stages of the amplifier are optimized for maximum output power. For optimization, we performed a load pull simulation for each stage. From the load pull simulation, we selected an optimum load impedance based on gain or power for a certain stage. After selecting the load impedance, the source impedance was transformed in such a way that the previous stage could deliver optimum gain or power. In this way, we select load impedance for optimum power in stages three and four and load impedance for optimum gain in stages one and two. The transistors (M_1, M_2) in the first stage have an emitter size of $4 \times (0.90 \times .07)\ \mu\text{m}^2$. The transistors (M_3, M_4) in the second stage have an emitter size of $6 \times (0.90 \times .07)\ \mu\text{m}^2$ and transistors (M_5, M_6) in the third stage have an emitter size of $8 \times (0.90 \times .07)\ \mu\text{m}^2$. The final stage is implemented using transistors (M_7, M_8) with an emitter size of $10 \times (0.90 \times .07)\ \mu\text{m}^2$.

Transmission lines (TL_{b1}-TL_{b8}) together with capacitors (C_1, C_3, C_4, C_6, C_7, C_9, C_{10}, *and* C_{12}) act as an RF choke. Although the length of the transmission lines (TL_{b1}-TL_{b8}) is less than a quarter-wavelength, they still provide a very high impedance at the base of CE and collector of CB of the cascode stages at the designed frequency.

The input matching, interstage matching, and output matching networks are implemented by the series and open-ended transmission lines (TL_1-TL_{11}). Small transmission lines (TL_{c1}-TL_{c5}) used for the connection to transistor terminals and MIM capacitors (C_{B1}-C_{B5}) used as a DC block are also part of the matching network. The bias current was 34 mA with a supply voltage of 3.4 V. Fig. 21 shows the S-parameters, and Fig. 22 shows the power gain and output power of the amplifier. From Fig. 21, it can be seen that the four-stage amplifier shows a peak gain of 22.5 dB with a 3-dB bandwidth from 225-250 GHz. The simulated saturation

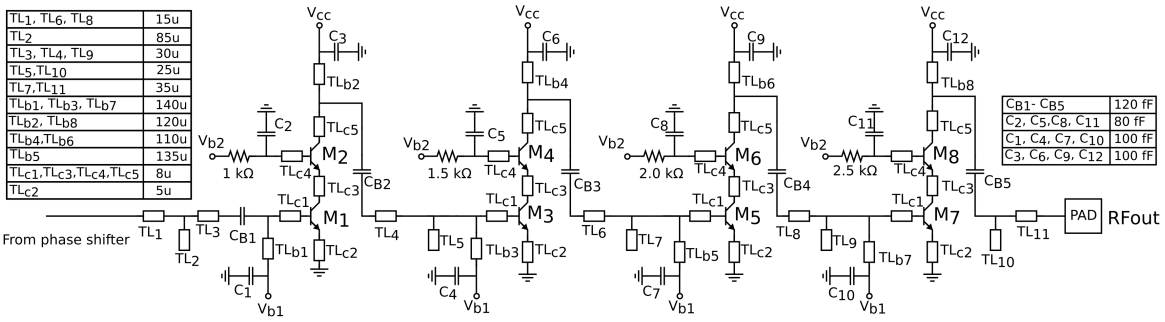


FIGURE 20. A simplified schematic of the 4-stage amplifier.

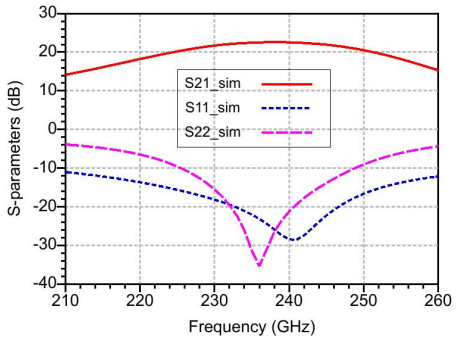


FIGURE 21. Simulated S-parameter of the 4-stage ampliflier.

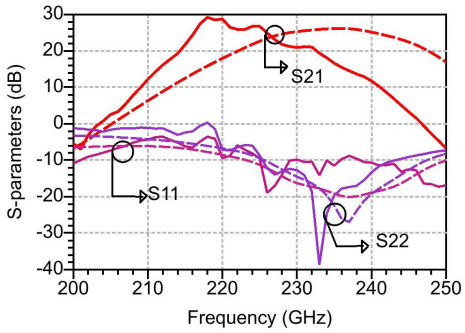


FIGURE 24. S-parameter of the phase shifter chain. Solid lines represent the measured data. The dashed line represents simulated data.

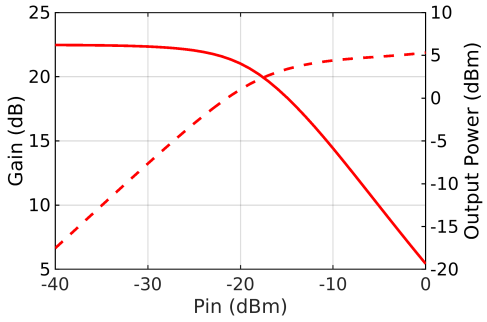


FIGURE 22. Simulated gain (solid line) and output power (dashed line) of the 4-stage amplifier.

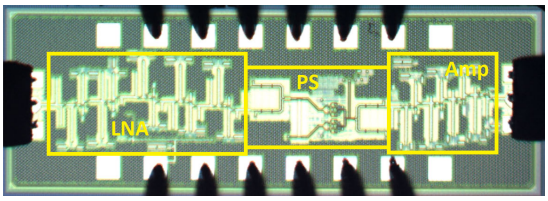


FIGURE 23. Die micrograph of the phase shifter chain.

power is 4 dBm at 240 GHz, and the 1-dB output compression (OP_{1dB}) point is 0 dBm.

D. EXPERIMENTAL RESULTS OF PHASE SHIFTER CHAIN

The 5-stage LNA, phase shifter, and 4-stage amplifier are integrated together to form the phase shifter chain circuit. The die micrograph of the phase shifter chain is shown in Fig. 23. The complete chip occupies a 1.41 mm^2 area. S-parameters of the implemented phase shifter chain were measured on-wafer over 140-325 GHz. An Agilent network analyzer is used in combination with WR3 and WR5 VNA extenders using 100-μm pitch GSG on-wafer probes. LRRM calibration was performed in this measurement. In the simulation, the 5-stage LNA and 4-stage amplifier were biased for a bias current of 35 mA and 34 mA, respectively to maximize the gain in the phase shifter chain. During the measurement with the original designed bias points as in the simulation for the LNA and the gain-enhancing amplifier, the phase shifter chain shows very peaky behavior. S_{21} becomes peaky at 225 GHz and 234 GHz. The S_{11} and S_{22} became positive at 225 GHz. The reason for the peaky behavior in the S-parameter measurement could be due to the feedback through the input and output probes because of the high gain of the phase shifter chain chip. After reducing the bias of the LNA and gain-enhancing amplifier to 19 mA and 18 mA, respectively, the gain of the phase shifter chain decreases, and probably the feedback between the input and output probes also decreases, and as a result, the phase shifter chain becomes stable. Fig. 24 shows the measured S-parameters of the designed phase shifter chain for reduced bias current of the LNA and gain-enhancing amplifier. The measured maximum gain of the phase shifter chain is 28 dB at 220 GHz for the nominal control voltage of 0.8 V for the two controls of the phase shifter. The measured polar plot of

TABLE 1. Phase shifter chain performance summary.

Reference	This work	[18]
Process	130nm SiGe BiCMOS	130nm SiGe BiCMOS
Freq (GHz)	220-240	220-250
Gain with 360° (dB)	18@230 GHz	-4@220 GHz (one channel)
Gain control (dB)	10	18
Phase control (deg)	360	360
Area (mm²)	1.41	4.0 (4 channel)
P_{DC} (mW)	153	167

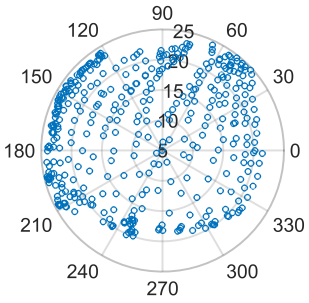


FIGURE 25. Measured polar plot of the phase shifter chain at 230 GHz.

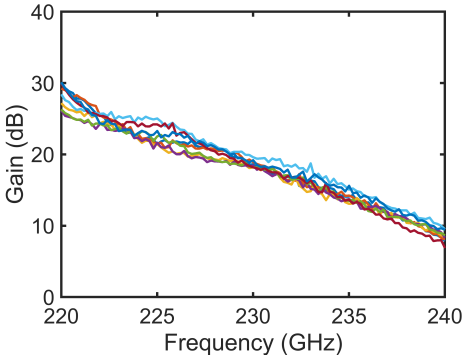


FIGURE 26. Measured 8 gain states of the phase shifter chain.

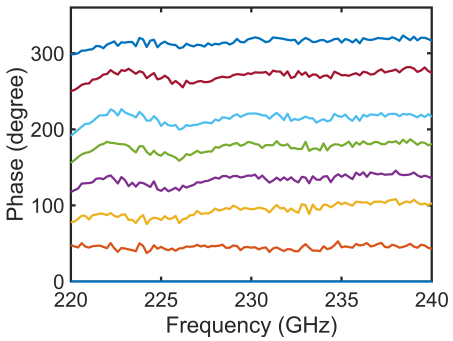


FIGURE 27. Measured 8 relative phase states of the phase shifter chain.

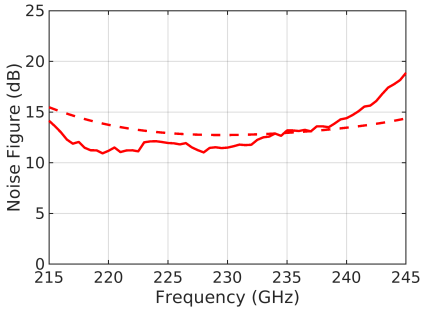


FIGURE 28. Noise figure of the phase shifter chain. Measured data is in solid line and simulated data is in dashed line.

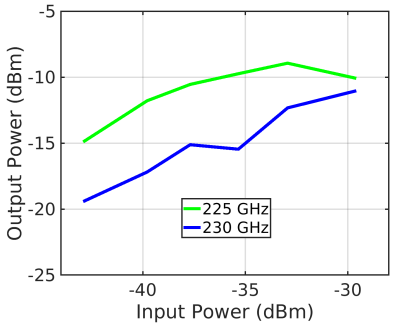


FIGURE 29. Measured output power of the phase shifter chain.

the S_{21} at 230 GHz is shown in Fig. 25. The phase shifter chain shows 360° phase control and 10 dB of gain control. The maximum gain with a full 360° phase control range is 18 dB.

Fig. 26 shows the measured 8 gain states of the phase shifter chain with 45° steps. The corresponding measured 8 phase states of the phase shifter chain with a 45° step from 220 GHz to 240 GHz are shown in Fig. 27. The maximum rms gain and phase errors are 1.55 dB and 16° from 222 GHz to 240 GHz, respectively. The measured minimum NF of the phase shifter chain is 11.5 dB at 230 GHz, as shown in Fig. 28. If we compare the measured noise figure of the phase shifter chain with the measured noise figure of the stand-alone 7-stage LNA from Fig. 7, we can say that they match fairly with each other from 225-239 GHz, which indicates that the design procedure for the LNA in the phase shifter chain work was successful. Fig. 29 shows the measured output power vs. input power of the phase shifter chain. The gain-enhancing amplifier was biased with 34 mA current to provide a simulated output power of 0 dBm. Due to the possible feedback oscillation in the phase shifter chain measurement, the gain-enhancing amplifier was later biased with a current of 18 mA. Hence, the phase-shifter chain did not achieve the expected output power of 0 dBm. The maximum output power from the phase shifter chain is −11 dBm at 230 GHz and −10 dBm at 225 GHz. Table 1 presents the summary of the phase shifter chain and compares the results with a published phased-array circuit [18] in a similar frequency range. From Table 1, it is seen that our designed phase shifter chain has a better performance in terms of gain with 360° phase tuning.

IV. POWER AMPLIFIER

In addition to the high-gain phase shifter chain, transmitted power in the RF phase-shifting transmitter can be increased

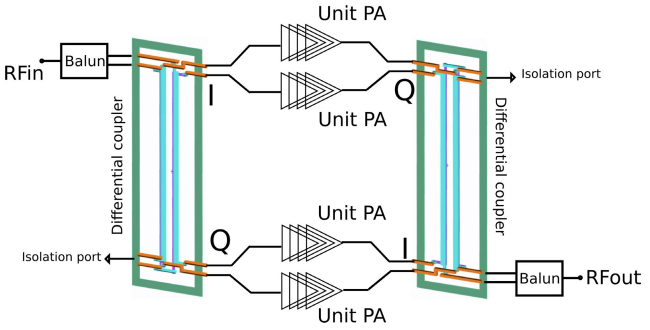


FIGURE 30. Simplified block diagram of the PA.

by providing high output power from a power amplifier. In a phased-array transmitter system, high output power from a driver PA is also needed to build a large phased-array. However, providing a large output power level above 200 GHz is challenging due to the fact that the transistor's maximum available gain decreases rapidly at these frequencies [23]. A common approach is to combine the power of several power amplifiers to achieve high output power. Different methods can be adopted for power combining. One of them is the Wilkinson power combiner, which offers better isolation between the PA units. Other approaches are to combine them using transformers or transmission lines. In these cases, the combining structure is also utilized as the matching network, achieving better PAE compared to the Wilkinson power combiner [19]. The transmission line combiner can offer more scalability and low loss, whereas a transformer-based combining network can provide a smaller area with a narrower bandwidth.

In this work, a unique 4-way combining technique using a compact, low-loss differential coupler is utilized in the PA design. The block diagram of the 4-way PA is shown in Fig. 30. In this design, two differential couplers are used, one at the input, which acts as a splitter, and another one at the output, which combines the unit PAs output, thus improving the matching of the amplifier. A similar design procedure for a differential coupler as in [22] is used here to generate differential I and Q paths, thus providing a 4-way path from a single coupler. Two units of PAs are connected to the I branch, and the other two units of PAs are connected to the Q branch of the input differential coupler. At the output, the signal from the PA connected to the input coupler's I branch is now connected with the Q branch of the output coupler, and vice versa for in-phase combination. Two compact Marchand baluns are used to realize the single-ended to the differential transformation of the signal. The unit PA is a four-stage cascode design. The schematic of the unit PA is similar to the amplifier described in Fig. 20 with a modification in the matching network to match the input and output of the coupler.

The die micrograph of the 4-way PA is shown in Fig. 31. The core PA occupies 0.67 mm^2. S-parameters of the implemented PA were measured on-wafer over 220-325 GHz.

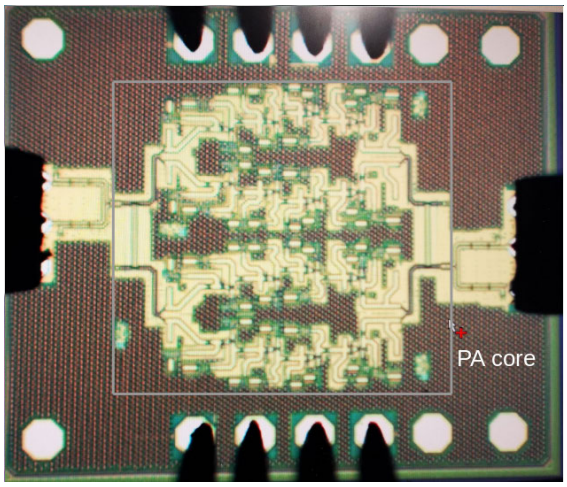


FIGURE 31. Die micrograph of the PA.

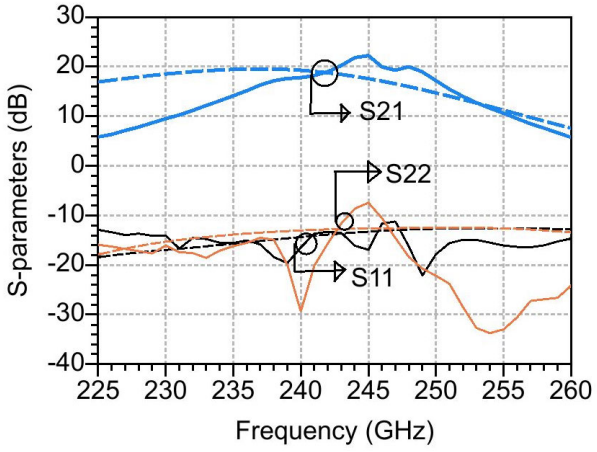


FIGURE 32. S-parameters of the PA. The solid line represents the measurement value and the dashed line represents the simulated value.

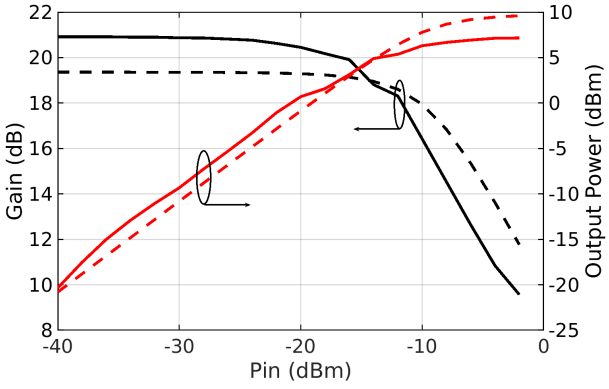


FIGURE 33. Output power and power gain of the PA. Solid line represents measurement data and dashed line represents simulated data.

Fig. 32 shows the measured S-parameters of the output PA. It shows a measured peak gain of 21 dB at 244 GHz with a 3-dB bandwidth of 11 GHz from 240 GHz to 251 GHz.

TABLE 2. State-of-the-art Silicon/SiGe PA performance beyond 200 GHz.

Ref.	[24]	[19]	[25]	[26]	[27]	[28]	This work
Technology	130 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe	65 nm CMOS	130 nm SiGe
fmax (GHz)	500	500	500	500	450	395	500
Frequency (GHz)	204-239	200-255	252	208-258	228-258	227-257	240-251
3-dB bandwidth (GHz)	35	55	11	40	30	30	10
Gain (dB)	22.5 (225 GHz)	12.5	21.5	9	10	13	21
$P_{sat}(dBm)$	9.5 (208 GHz)	12	0	0	5	-3.3	7.15
$OP_{1dB}(dBm)$	6 (215 GHz)	9	-3.7	-2.5	NA	-5.1	4.1
$PAE_{1dB}(\%)$	1.6	1	0.3	0.4	NA	NA	0.5
DC power (mW)	245	740	149	255	400	23.8	819
Area (mm^2)	0:16	0.83	0.17	1.2	NA	0.053	0.67(core)

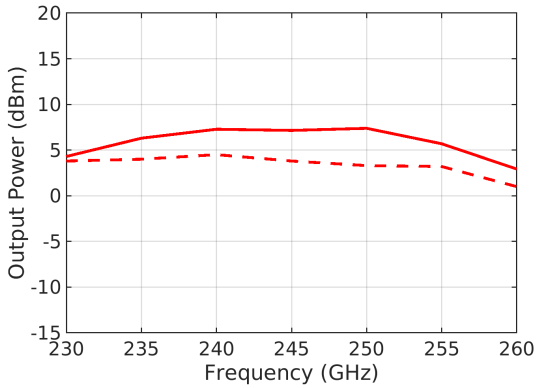


FIGURE 34. Measured Psat (solid line) and P_{1dB} (dashed line) against frequency.

At 230 GHz, this PA exhibits a measured gain of 10.1 dB. The input and output matching are better than 10 dB in almost all the regions from 225-260 GHz. The bias current is 59.4 mA in a unit PA with a 3.45 V supply. Fig. 33 shows the measured output power and power gain of the PA. The measured peak P_{sat} is 7.15 dBm at 244 GHz. At 230 GHz, P_{sat} is 4.3 dBm and P_{1dB} is 4.0 dBm. Fig. 34 shows the saturated power and P_{1dB} against the frequency. It can be seen from Fig. 34 that P_{1dB} is close to 4 dBm or better from 230-250 GHz. Also, the P_{sat} is equal to or better than 4.3 dBm over the frequency range from 230-255 GHz. In the measurement, the result shows a deviation from the simulation result. The gain in the measurement is higher than the simulation result. This could be due to the actual g_m of the transistor being higher than the model we used for the simulation. Thus, the PA could achieve a higher gain even with a lower collector current compared to the simulation. The peak gain is shifted towards high frequencies by 5 GHz. This might be due to the parasitic effect of all the connections to the transistor terminals, which our EM modeling did not capture accurately. All these effects might contribute to the narrow measured bandwidth of the PA compared to the simulation bandwidth.

The PA measurement results are summarized in Table 2 with other published PAs. From Table 2, it is found that the designed PA has better gain than any other PA and better output power except the PA in [19] in the 225-255 GHz range.

V. CONCLUSION

In this paper, we have presented the design of the key elements for the phased-array scaling above 200 GHz in a 0.13-μm SiGe BiCMOS technology. The implemented phase shifter chain demonstrates a measured gain of 28 dB at 220 GHz and operates from 220 GHz to 240 GHz with a minimum measured noise figure of 11.5 dB at 230 GHz. It achieves 18 dB of peak gain at 230 GHz with 360° phase tuning and 10 dB of gain control. Also, a 4-way power amplifier is implemented in a unique way, utilizing a differential quadrature coupler as a power combiner to increase the transmit power. The implemented PA shows a measured peak gain of 21 dB and saturated output power (Psat) of 7.1 dBm at 244 GHz. The realized PA delivers a saturated power better than of 4.3 dBm from 230-250 GHz. This PA shows better gain than any other published design in the 220-250 GHz range. To demonstrate a large phased-array, it is critical to have a very high gain, low noise figure RF phase-shifting path for a receiver. In the transmitter, along with the high-gain RF phase-shifting path, a power amplifier with high gain and high output power is needed to deliver higher transmit power. Based on the detailed discussions on

the proposed architecture and measured performances of our designed circuits, a large phased-array system can be realized with our designed phase shifter chain and the power amplifier.

REFERENCES

[1] Z. D. Taylor, R. S. Singh, D. B. Bennett, P. Tewari, C. P. Kealey, N. Bajwa, M. O. Culjat, A. Stojadinovic, H. Lee, J.-P. Hubschman, E. R. Brown, and W. S. Grundfes, "THz medical imaging: In vivo hydration sensing," *IEEE Trans. Terahertz Sci. Technol.*, vol. 1, no. 1, pp. 201–219, Sep. 2011.

[2] S. Cherry, "Edholm's law of bandwidth," *IEEE Spectr.*, vol. 41, no. 7, pp. 58–60, Jul. 2004.

[3] N. Sarmah, J. Grzyb, K. Statnikov, S. Malz, P. Rodriguez Vazquez, W. Föerster, B. Heinemann, and U. R. Pfeiffer, "A fully integrated 240-GHz direct-conversion quadrature transmitter and receiver chipset in SiGe technology," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 562–574, Feb. 2016.

[4] Z. Wang, P.-Y. Chiang, P. Nazari, C.-C. Wang, Z. Chen, and P. Heydari, "A CMOS 210-GHz fundamental transceiver with OOK modulation," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 564–580, Mar. 2014.

[5] K.-C. Huang and Z. Wang, "Terahertz terabit wireless communication," *IEEE Microw. Mag.*, vol. 12, no. 4, pp. 108–116, Jun. 2011.

[6] I. Kallfass, J. Antes, T. Schneider, F. Kurz, D. Lopez-Diaz, S. Diebold, H. Massler, A. Leuther, and A. Tessmann, "All active MMIC-based wireless communication at 220 GHz," *IEEE Trans. Terahertz Sci. Technol.*, vol. 1, no. 2, pp. 477–487, Nov. 2011.

[7] K. Sengupta and A. Hajimiri, "A 0.28 THz power-generation and beam-steering array in CMOS based on distributed active radiators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3013–3031, Dec. 2012.

[8] X.-D. Deng, Y. Li, J. Li, C. Liu, W. Wu, and Y.-Z. Xiong, "A 320-GHz 1×4 fully integrated phased array transmitter using 0.13-μm SiGe BiCMOS technology," *IEEE Trans. Terahertz Sci. Technol.*, vol. 5, no. 6, pp. 930–940, Nov. 2015.

[9] D. Parveg, D. Karaca, M. Varonen, A. Vahdati, and K. A. I. Halonen, "Demonstration of a 0.325-THz CMOS amplifier," in *Proc. Global Symp. Millim. Waves (GSMM) ESA Workshop Millimetre-Wave Technol. Appl.*, Espoo, Finland, Jun. 2016, pp. 1–3.

[10] P. Chevalier, T. F. Meister, B. Heinemann, S. Van Huylenbroeck, W. Liebl, A. Fox, A. Sibaja-Hernandez, and A. Chantre, "Towards THz SiGe HBTs," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Oct. 2011, pp. 57–65.

[11] E. Ojefors, B. Heinemann, and U. R. Pfeiffer, "Subharmonic 220- and 320-GHz SiGe HBT receiver front-ends," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1397–1404, May 2012.

[12] E. Ojefors, B. Heinemann, and U. R. Pfeiffer, "A 220 GHz subharmonic receiver front end in a SiGe HBT technology," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Baltimore, MD, USA, Jun. 2011, pp. 1–4.

[13] J.-D. Park, S. Kang, S. V. Thyagarajan, E. Alon, and A. M. Niknejad, "A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication," in *Proc. Symp. VLSI Circuits (VLSIC)*, Honolulu, HI, USA, Jun. 2012, pp. 48–49.

[14] Y. Yu, P. G. M. Baltus, A. De Graauw, E. van der Heijden, C. S. Vaucher, and A. H. M. van Roermund, "A 60 GHz phase shifter integrated with LNA and PA in 65 nm CMOS for phased array systems," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1697–1709, Sep. 2010.

[15] M. Varonen, A. Lamminen, M. Kantanen, J. Holmberg, A. Rantala, M. Lahdes, J. Saily, D. Parveg, M. Kaunisto, and J. Aurinsalo, "Receive and transmit beamforming SiGe BiCMOS ICs for scalable E-band phased arrays," in *Proc. 51st Eur. Microw. Conf. (EuMC)*, London, U.K., Apr. 2022, pp. 273–276.

[16] Y. Zhao, E. Ojefors, K. Aufinger, T. F. Meister, and U. R. Pfeiffer, "A 160-GHz subharmonic transmitter and receiver chipset in an SiGe HBT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 10, pp. 3286–3299, Oct. 2012.

[17] K. Sengupta and A. Hajimiri, "A 0.28 THz 4×4 power-generation and beam-steering array," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2012, pp. 256–258.

[18] M. Elkhouly, S. Glisic, C. Meliani, F. Ellinger, and J. C. Scheytt, "220–250-GHz phased-array circuits in 0.13-μm SiGe BiCMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 3115–3127, Aug. 2013.

[19] M. H. Eissa and D. Kissinger, "A 13.5 dBm fully integrated 200-to-255 GHz power amplifier with a 4-way power combiner in SiGe: C BiCMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2019, pp. 82–84.

[20] Y. Mao, K. Schmalz, J. Borngraber, and J. C. Scheytt, "245-GHz LNA, mixer, and subharmonic receiver in SiGe technology," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 12, pp. 3823–3833, Dec. 2012.

[21] M. Najmussadat, R. Ahamed, M. Varonen, D. Parveg, Y. Tawfik, and K. A. I. Halonen, "Design of a 240-GHz LNA in 0.13 μm SiGe BiCMOS Technology," in *Proc. 15th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Utrecht, The Netherlands, Jan. 2021, pp. 17–20.

[22] R. Ahamed, M. Varonen, D. Parveg, M. Najmussadat, Y. Tawfik, and K. A. I. Halonen, "A 200–250-GHz phase shifter utilizing a compact and wideband differential quadrature coupler," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 7, pp. 883–886, Jul. 2022.

[23] P. Stärke, C. Carta, and F. Ellinger, "High-linearity 19-dB power amplifier for 140–220 GHz, saturated at 15 dBm, in 130-nm SiGe," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 4, pp. 403–406, Apr. 2020.

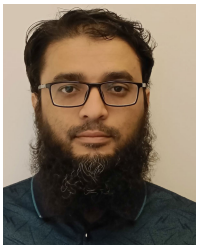
[24] Z. Li, J. Chen, H. Li, Z. Wang, D. Hou, P. Yan, Z. Chen, and W. Hong, "A 220-GHz power amplifier with 22.5-dB gain and 9-dBm P_{sat} in 130-nm SiGe," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 10, pp. 1166–1169, Oct. 2021.

[25] H. Li, J. Chen, D. Hou, P. Zhou, J. Yu, P. Yan, L. Peng, H. Lu, and W. Hong, "A 250-GHz differential SiGe amplifier with 21.5-dB gain for sub-THz transmitters," *IEEE Trans. Terahertz Sci. Technol.*, vol. 10, no. 6, pp. 624–633, Nov. 2020.

[26] M. H. Eissa, A. Malignaggi, M. Ko, K. Schmalz, J. Borngräber, A. C. Ulusoy, and D. Kissinger, "A 216–256 GHz fully differential frequency multiplier-by-8 chain with 0 dBm output power," in *Proc. 47th Eur. Microw. Conf. (EuMC)*, Nuremberg, Germany, Oct. 2017, pp. 216–219.

[27] N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "235–275 GHz (x16) frequency multiplier chains with up to 0 dBm peak output power and low DC power consumption," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Tampa, FL, USA, Jun. 2014, pp. 181–184.

[28] D.-W. Park, D. R. Utomo, B. H. Lam, S.-G. Lee, and J.-P. Hong, "A 230–260-GHz wideband and high-gain amplifier in 65-nm CMOS based on dual-peak G_{max}-core," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1613–1623, Jun. 2019.



MD. NAJMUSSADAT received the B.Sc. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology, in 2008, and the M.Sc. degree in communications technology (microelectronics track) from Ulm University, Germany, in 2012. He is currently pursuing the Ph.D. degree with the Department of Electronics and Nanoengineering, Aalto University, Finland. His current research interests include millimeter-wave RF circuits and RFIC/MMIC design for wireless transceivers for high-speed data communication.

RAJU AHAMED received the B.Sc. degree in electrical and electronic engineering from the Chittagong University of Engineering and Technology (CUET), Chittagong, Bangladesh, in 2013, and the M.Sc. degree in nano and radio sciences from Aalto University, Espoo, Finland, in 2017, where he is currently pursuing the Ph.D. degree with the Department of Electronics and Nanoengineering. He is also a RFIC Design Engineer with CoreHW Oy, Finland. His current research interest includes the development of millimeter-wave integrated circuits in silicon technologies for high-speed wireless communication.

MIKKO VARONEN received the M.Sc., Lic.Sc., and D.Sc. degrees (Hons.) in electrical engineering from Aalto University (formerly the Helsinki University of Technology), Espoo, Finland, in 2002, 2005, and 2010, respectively. In 2011, he was a NASA Postdoctoral Program Fellow with the Jet Propulsion Laboratory (JPL), California Institute of Technology (Caltech), Pasadena, CA, USA. In 2012, he was a Postdoctoral Researcher and an Academy of Finland Postdoctoral Researcher with the Department of Micro- and Nanosciences, Aalto University, from 2013 to 2016. During his Postdoctoral Fellowship, he was a Visiting Scientist with JPL, Electrical Engineering Department, Caltech, and the Fraunhofer Institute of Applied Solid-State Physics, Freiburg im Breisgau, Germany. He is currently a Senior Scientist and an Academy of Finland Research Fellow with VTT Technical Research Centre of Finland Ltd., Espoo. His current research interests include the development of millimeter-wave integrated circuits using both silicon and compound semiconductor technologies for applications ranging from astrophysics and earth remote sensing to millimeter-wave communications.

DRISTY PARVEG received the B.Sc. degree in electrical and electronics engineering (EEE) from the Rajshahi University of Engineering and Technology (RUET), Rajshahi, Bangladesh, in 2004, the M.Sc. degree in electronic/telecommunications engineering from the University of Gävle, Gävle, Sweden, in 2009, and the Ph.D. degree in electrical engineering (EE) from Aalto University, Espoo, Finland, in 2018. During his Ph.D. studies, he was a Visiting Scientist on several occasions with the High-Speed Integrated Circuit Laboratory (Prof. Ali Hajimiri's Group), California Institute of Technology (Caltech), Pasadena, CA, USA. In 2022, he was a JPL Postdoctoral Researcher in the Microwave Systems Technology group at NASA Jet Propulsion Laboratory, California Institute of Technology (Caltech), Pasadena, CA, USA. Currently, he is a Research Scientist in the Antennas and RF technology department at VTT Technical Research Centre of Finland, Espoo. His current research interests include mmWave radio front-end IC designing for miniaturized earth remote sensing receivers, transceiver front-ends for FMCW radars, and microwave/mmWave systems and packaging designs for wireless communication. Since 2016, he has been serving as an active reviewer for several IEEE journals and letters in the research area of microwave theory and techniques.

MIKKO KANTANEN received the M.Sc., Lic.Sc., and D.Sc. degrees in electrical engineering from Aalto University (formerly the Helsinki University of Technology), Espoo, Finland, in 2001, 2006, and 2017, respectively. Since 2001, he has been with MilliLab, VTT Technical Research Centre of Finland Ltd., Espoo, where he is currently a Senior Scientist. His research interests include millimeter-wave integrated circuit design, millimeter-wave measurements, and millimeter-wave systems. He was a recipient of the 47th European Microwave Conference Microwave Prize and the co-recipient of the Asia–Pacific Microwave Conference Prize, in 2006.

KARI A. I. HALONEN received the M.Sc. degree in electrical engineering from the Helsinki University of Technology, Finland, in 1982, and the Ph.D. degree in electrical engineering from Katholieke Universiteit Leuven, Belgium, in 1987. Since 1988, he has been with the Electronic Circuit Design Laboratory, Helsinki University of Technology (since 2011, Aalto University). Since 1993, he has been an Associate Professor with the Faculty of Electrical Engineering and Telecommunications, where he has been a Full Professor, since 1997. In 1998, he became the Head of the Electronic Circuit Design Laboratory, and he was appointed as the Head of the Department of Micro- and Nanosciences, Aalto University, from 2007 to 2013. He is the author or coauthor of more than 450 international and national conferences and journal publications on analog and RF integrated circuits. His research interests include CMOS and BiCMOS analog and RF integrated circuits, particularly for telecommunication and sensor applications. He has served as the TPC Member for ESSCIRC and ISSCC. He was a recipient of the Beatrice Winner Award at the 2002 ISSCC Conference. He has been an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, and the Technical Program Committee Chairperson of the European Solid-State Circuits Conference, in 2000 and 2011.