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The authors investigate a wafer scale tunnel junction fabrication method, where a plasma etched via through a dielectric layer covering bottom Al electrode defines the tunnel junction area. The *ex situ* tunnel barrier is formed by oxidation of the bottom electrode in the junction area. Room temperature resistance mapping over a 150 mm wafer gives local deviation values of the tunnel junction resistance that fall below 7.5% with an average of 1.3%. The deviation is further investigated by sub-1 K measurements of a device, which has one tunnel junction connected to four arrays consisting of N junctions ($N=41$, junction diameter 700 nm). The differential conductance is measured in single-junction and array Coulomb blockade thermometer operation modes. By fitting the experimental data to the theoretical models, the authors found an upper limit for the local tunnel junction resistance deviation of $\sim$5% for the array of $2N+1$ junctions. This value is of the same order as the minimum detectable deviation defined by the accuracy of the authors' experimental setup. © *2010 American Vacuum Society.* [DOI: 10.1116/1.3490406]

I. INTRODUCTION

Metallic tunnel junctions are the main ingredients of electronic devices that are based, for example, on single electron tunneling[1] and/or the Josephson effect.[2] Aluminum oxide is the tunnel barrier material most widely used as it combines good junction properties with a controlled fabrication process due to the stable oxide layer formed by thermal oxidation. The standard fabrication method for submicron tunnel junction devices, for laboratory use, involves e-beam lithography and the shadow evaporation technique.[3] A well-known wafer scale fabrication method of (few micron size) tunnel junctions uses trilayer films,[4] where the size of the junctions is defined through postpatterning. This trilayer fabrication is a relatively mature technique and it has been used for small scale production of superconducting sensors and multilayer Josephson junction structures for more than 20 years.[4–6]

The shadow evaporation and the trilayer processes are *in situ* methods, i.e., the metal-tunnel junction-metal structure is defined without breaking the vacuum. In this article, we investigate *ex situ* tunnel junction fabrication method, which utilizes a through dielectric via defining the tunnel junction areas. A similar method has been successfully utilized in creating few micrometer sized tunnel junctions for x-ray sensors[7] and quantum information devices.[8] We use this via method to fabricate high resistance junctions on micron/submicron scale. We target a junction resistance regime on the order of 20 kΩ that is suitable for Coulomb blockade thermometers (CBTs),[9,10] which are primary thermometers based on single electron tunneling in the weak Coulomb blockade regime. In the past, the CBT devices have been fabricated by electron beam lithography with the shadow angle method. We characterize our process, first, by mapping the junction resistance across a 150 mm wafer at room temperature. The definitive characterization is obtained by single-junction[10] and array[9] CBT measurements of a device with 700 nm diameter junctions.

II. EXPERIMENT

Our tunnel junction structure consists of three layers: bottom aluminum, dielectric (here SiO$_2$), and top aluminum [see Fig. 1(a)]. The tunnel junctions are defined by a through dielectric via. We have fabricated the devices on 150 mm Si wafers. The fabrication process starts by growing a 300-nm-thick thermal SiO$_2$. This is followed by deposition of 250 nm

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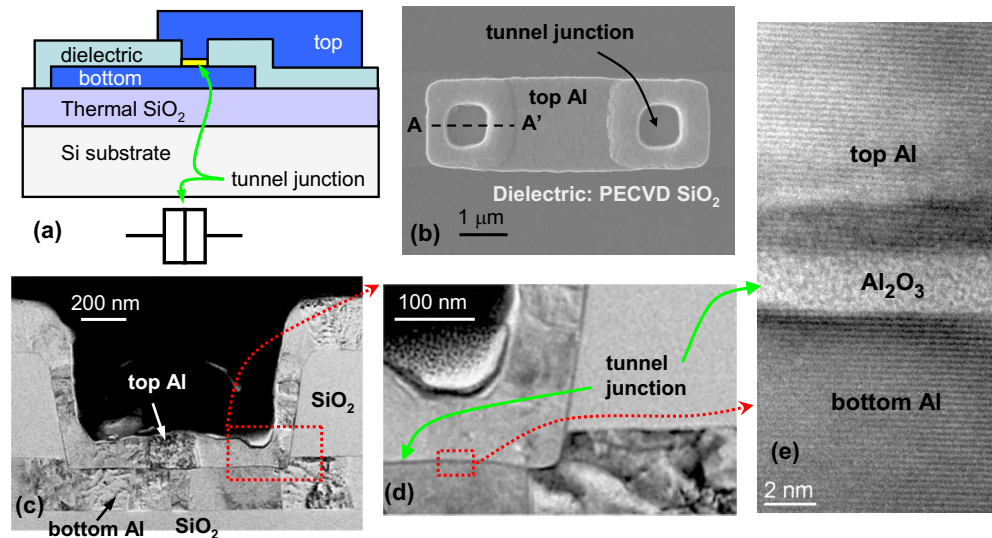
FIG. 1. (Color online) (a) Schematic cross-section of a tunnel junction and circuit symbol. (b) Top view SEM image of a rectangular double tunnel junction. (c) TEM cross-section along *A-A′*. (d) Blow up of the junction edge. (e) High resolution TEM image of the junction.

Al bottom electrode. The Al films are deposited by a dc magnetron sputter in a multimaterial deposition system CS 730 S from von Ardenne Anlagentechnik GmbH (at a base pressure of 2×10^{-8} mbar). The bottom electrode is patterned by UV lithography and plasma etching. Here, all lithography steps involve i-line projection lithography system Canon FPA-2600i3. The bottom electrode is etched with a $Cl_2 + BCl_3$ plasma in a LAM 9600 transformer coupled plasma system. The dielectric layer (250-nm-thick SiO_2) is deposited with an Oxford DP100 plasma enhanced chemical vapour deposition system. In this step, the substrate temperature is maintained at 180 °C. Next, the vias are defined in the SiO_2 dielectric. In patterning, we utilize $CF_4 + CHF_3$ plasma in a LAM 4520 oxide etcher. After resist stripping, the wafers are loaded to the von Ardenne sputter system and the native oxide is removed on top of the bottom Al by Ar plasma. This is followed by oxidation and Al deposition without breaking the vacuum. The oxidation is performed at elevated temperature, with the back of the wafer heated to 180 °C by an irradiative heater and with pure oxygen at a chamber pressure of 110 mbars for 6000 s. Finally, the 250-nm-thick top Al electrodes are defined utilizing UV lithography and $Cl_2 + BCl_3$ plasma etching.

Figure 1(a) depicts a cross sectional schematics overview of one tunnel junction and clarifies how the tunnel barrier is embedded between the electrodes and the surrounding dielectric. Figure 1(b) shows a top view SEM image of an Al island with two tunnel junctions. The bottom electrode edges are clearly visible only in the regions covered by the top Al. Cross-sectional transmission electron microscope (TEM) images are shown in Figs. 1(c) and 1(d). Note that the Al is thinner on the side walls of the junction via due to poor step coverage of Al. Argon sputtering in the native oxide removal step reduces the thickness of the bottom electrode in the junction areas [see Figs. 1(c) and 1(d)]. Here, the excess Ar bombardment after the native oxide breakthrough has led to

~50 nm Al loss. Figure 1(e) shows a high resolution TEM image revealing crystalline Al layers and amorphous Al_2O_3 tunnel barrier. The dark region in the top Al above the tunnel barrier is an experimental artifact following from focused ion beam sample preparation.

A single processed 150 mm wafer contains various tunnel junction devices and test structures. At room temperature, the junction resistance was mapped across the wafer utilizing a test structure designed for four point measurement of a single junction. After dicing the wafer, a single chip was mounted to a sample holder of a dilution refrigerator equipped with filtered dc lines made of thermocoax cables. The chip contains a device, which has one tunnel junction connected to four arrays consisting of N junctions ($N=41$, junction diameter of 700 nm). This device layout is suitable for simultaneous single-junction[10] and array CBT (Ref. 9) operation modes. Differential conductance measurements as a function of applied bias voltage were performed in the two modes at substrate temperature of $T=224$ mK. A magnetic field on the order of 50 mT was applied in order to keep Al in the normal state.

III. RESULTS AND DISCUSSION

Figure 2(a) shows the tunnel junction resistance mapped across a 150 mm wafer in a 2×2 mm^2 grid (nominal junction area is 1 μm^2). The measurement region has a diameter of 110 mm. Within this region the junction resistance values fall between ~10 and 14 kΩ and we find neither shorted nor open junctions. The average tunnel junction resistance is 12.2 kΩ and deviation over this area is 6.5%. However, for many device applications, this large length scale deviation is not so relevant. The most important figure of merit is the local deviation $D = \delta R/R$, i.e., the local junction resistance deviation within a single device. We have investigated D by measuring two adjacent junctions. We define $D = 2|R_1$
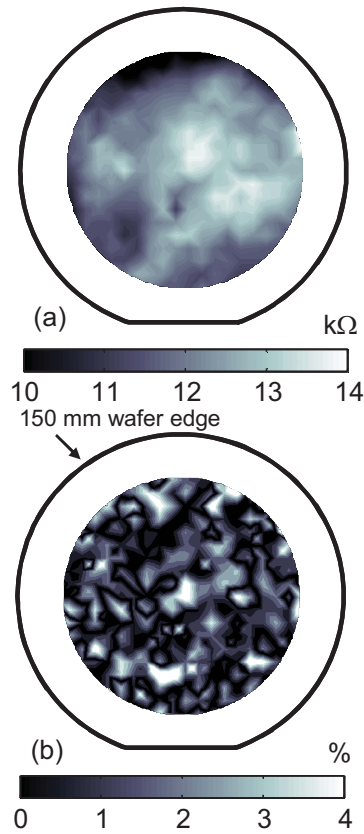
FIG. 2. (Color online) (a) Gray scale plot of junction resistance on a single 150 mm wafer at room temperature of rectangular 1 μm^2 junctions. The scale bar is in kΩ. (b) Local deviation D in the junction resistance. A single data point is obtained from the resistances R_1 and R_2 of two junctions whose distance on the wafer is 400 μm: $D=2|R_1-R_2|/(R_1+R_2)$. The scale bar is in %.
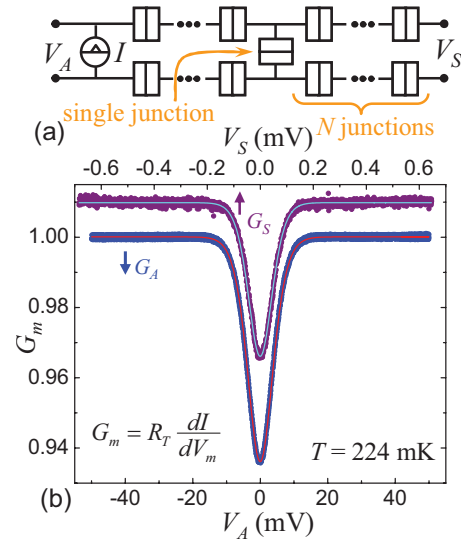

FIG. 3. (Color online) (a) Illustration of two CBT configurations. Voltage $V_{S(A)}$ gives the single-junction (array) CBT bias voltage values. (b) Symbols are the measured differential conductances in the two configurations with $N=41$ at substrate temperature of $T=224$ mK. The nominal junction diameter is 700 nm. The conductance values are normalized and an offset of 0.01 is added to G_S. The solid curves are fits to the theoretical models (see text), which give the temperatures $T_S=222$ mK and $T_A=221$ mK from G_S and G_A, respectively.

$-R_2|/(R_1+R_2)$, where R_1 and R_2 are the resistances of junctions with a distance of 400 μm. The local deviation map (2×2 mm^2 grid) is shown in Fig. 2(b). In the measurement region $D<7.5\%$ and the average value is 1.3%. The junction quality stays at this level down to 700 nm junction diameter, below which deviation increases and significant amount of open junctions can be found. Note that 700 nm is still quite far from the i-line wavelength and this degradation is due to the chosen lithography parameters.

We have explored the junction properties further by differential conductance measurements at low temperature as a function of applied bias voltage. We have adopted the single-junction and array CBT measurement configurations depicted in Fig. 3(a). In these measurements, voltage V_m with $m=S(A)$ gives the corresponding single-junction (array) bias voltage and the normalized differential conductance $G_m=R_T dI/dV_m$, where R_T is the asymptotic high bias resistance and I is the bias current. Experimental G_m measured from a device with 700 nm diameter circular junctions at substrate temperature $T=224\pm15$ mK is shown in Fig. 3(b). This junction size leads to small charging energy and weak Coulomb blockade, which is observed as a small dip in G_m at zero bias. Weak Coulomb blockade with quasicontinuous island charge is observed when the ratio of the charging en-

ergy and thermal energy, $u=e^2/2Ck_BT$, is sufficiently small (C is the capacitance of a single junction). At the $u\ll1$ limit, the normalized differential conductance is given by[9,10]

$$G_m = 1 - \frac{\delta_m}{k_B T_m} g(eV_m/k_B T_m), \tag{1}$$

where $g(x)=e^x[e^x(x-2)+x+2]/(e^x-1)^3$ and the prefactor δ_m depends on the junction capacitances. The full-width-half-maximum voltage ($V_{1/2}^m$) of the dip is proportional to the temperature, which provides the primary thermometry by CBT sensors. From $g(x)$ or full master equation model, one finds $T_m=eV_{1/2}^m/5.439N_m k_B$, where $N_A=2N+1$ and $N_S=1$.[9,10]

The solid curves in Fig. 3(b) are fits to the full master equation model, which is modified to take into account overheating effects due to the applied bias voltage and finite electron-phonon coupling, as described in Ref. 11. The fitting procedure gives CBT temperatures $T_S=222$ mK and $T_A=221$ mK.

As T_S does not depend on uniformity of the junction network, the above temperature fitting results can be utilized in analyzing junction resistance deviation D in the arrays. The error in the array temperature reading arising from D is given by $\delta T_A/T_A\approx-kD^2$, where numerical factor $k\approx0.73+(N_A-1)/N_A$ with $N_A=2N+1$ (here $N=41$).[12] Now, if we substitute $\delta T_A/T_A\rightarrow2(T_S-T_A)/(T_A+T_S)$, we find the measured resistance deviation $D_{meas}\approx5\%$, which coincides with the room temperature results. However, we should note that this deviation value is already better than the accuracy of our experimental setup. This is mainly determined by the relative gain error of $<1\%$ of our voltage preamplifiers. By setting $\delta T_A/T_A=1\%$, we find the minimum detectable deviation

$D_{min} \approx 7.6\%$. Thus, as $D_{min} > D_{meas}$, we conclude that, because of the robustness of the temperature reading versus D, the junction resistance deviation obtained from the CBT measurements is limited by the accuracy of the experimental setup.

The depth of the dip in the conductance curves $\Delta G_m = (\delta_m/k_B T_m)g(0)$ [$g(0) = 1/6$] allows the determination of the junction capacitance C. For the array configuration $\delta_A = (e^2/C)(N_A - 1)/N_A$ when we have $C = e^2(N_A - 1)/(6N_A k_B T \Delta G_A)$ (Ref. 12) and from the experimental data, we find $C \approx 22$ fF. This corresponds to a specific capacitance ~ 50 fF/μm^2, which is a typical value for aluminum oxide tunnel junctions. Another noteworthy property for the tunnel junction quality is the linearity of the current-voltage characteristics; we find a constant differential conductance up to an applied voltage of 20 mV per junction and an increase of conductance of 1.5% at 40 mV per junction. These are very typical values for aluminum oxide tunnel barriers.[13]

IV. SUMMARY AND CONCLUSIONS

We have investigated *ex situ* tunnel junction fabrication method to produce high resistance (~ 12 kΩ-μm^2) tunnel junctions on wafer scale. Our fabrication method utilized plasma etched via in a dielectric that covers bottom Al electrode. The *ex situ* tunnel barrier was formed by bottom electrode oxidation after Ar plasma removal of the native oxide in the junction area. After the tunnel barrier formation, the top Al electrode was sputter deposited without breaking the vacuum.

Room temperature tunnel junction resistance mapping over 150 mm wafer gives local deviation values of the tunnel junction resistance below 7.5% with an average value of 1.3%. The junction resistance deviation was further investigated by low temperature measurements that utilized single-junction and array CBT operation of a device with 700 nm diameter junctions. The low temperature measurements agreed with the room temperature junction resistance mapping. By fitting the experimental CBT data to the theoretical models, we found a local tunnel junction resistance deviation of $\sim 5\%$ (array of 83 junctions). However, the estimation of the local junction resistance deviation from the CBT measurements was in the end limited by the accuracy of our low temperature experimental setup ($\sim 7.6\%$). We conclude that the small (local) tunnel junction resistance deviation indicated by the room temperature and low temperature measurements suggests that our fabrication process can be used for high-yield production of primary CBT sensors.

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