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A Compact and Wideband mmWave Passive CMOS Circulator Based on Switched All-Pass Networks

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Abstract—This paper presents a compact and wideband passive CMOS circulator for mmWave phased array transceivers. The paper focuses on achieving a compact die area while still offering competitive performance in terms of loss, isolation, and linearity. Our implemented circulator includes two reciprocal phase shift branches as well as a single-path non-reciprocal phase shift branch. We propose to use first-order lattice all-pass filters with coupled inductors to create the required phase shifts, which offer more compact, wideband, and predictable results compared to conventional lattice all-pass filters with two separate inductors. We also propose to use four identical first-order lattice cells in reciprocal and non-reciprocal branches. This can further reduce the size of the non-reciprocal branch due to fewer inductors compared to a typical second-order all-pass filter like bridged-T. The circuit is implemented in a 28 nm CMOS process, compared to a typical second-order all-pass filter like bridged-T. The circuit is implemented in a 28 nm CMOS process, compared to a typical second-order all-pass filter like bridged-T. We propose to use first-order lattice all-pass filters for the circulator is crucial to enable a cost-effective solution since the size of antennas is still large due to the use of overlapping clock signals at the same frequency as the input signal, making it difficult to implement at higher frequencies. N-path filter based circulator was also examined [17], [18]. This approach achieves a more compact die area by avoiding TLs, yet the number of inductors could still be further reduced. Furthermore, the designed structure operates only at 6.5 GHz and it needs to be scaled up to the mmWave ranges.

In order to address the discussed challenges, this paper presents an integrated circulator that is fabricated on a 28 nm CMOS process. The introduced mmWave circulator aims to achieve a compact die area while still offering competitive performance in terms of loss, isolation, and linearity. In Chapter II we describe the circulator design. Chapter III covers the measurement results, and Chapter IV concludes the paper.

II. Circuit Design and Operation

The circulator is realized using a ring that includes two reciprocal branches with -90° phase shift in either direction and a non-reciprocal branch with 0°/-180° phase shift depending on the signal direction as shown in Fig. 1. The arrangement of phase shifts results in constructive interference in one direction
while destructive interference in the opposite direction, which allows signals to propagate only in one direction across the ring. Both reciprocal and non-reciprocal branches create the required phase shifts using passive filters. For this purpose, we have employed all-pass networks, which can offer significant benefits over TL-based structures, including a more compact die area and wider bandwidth [18]. The -90° phase shifts required by reciprocal branches are provided by first-order lattice all-pass filters. The non-reciprocal branch, on the other hand, demands passive filters that are placed between I/Q mixers switched at a frequency lower than the input frequency to facilitate low-power operation. A lower switching frequency corresponds to a longer time delay introduced by the internal filter. When considering a TL-based implementation, as proposed in [15], the corresponding line needs to be extended. This requires more equivalent LC sections ($\frac{C}{L} \times \frac{m}{\pi}$ sections), resulting in a larger die area to provide the required phase shift, thereby falling into the common tradeoff with loss. However, utilizing a second-order all-pass filter, as suggested in [18], can ideally provide the required phase shift without affecting the amplitude. Furthermore, this approach increases the bandwidth thanks to the highly linear phase response around the center frequency, thus maintaining the required phase relationship over a large frequency band. As the input frequency deviates from the designed center of the all-pass filter, the components $\omega_{in} \pm \omega_m$ move accordingly, and the phase relationship is maintained as long as they both are in the linear region, until one of them falls into the phase plateau regime.

The detailed phase-frequency domain analysis of the non-reciprocal branch is shown in Fig. 1. In the A to D direction, the incoming signal at frequency $\omega_m$ is first mixed with I clock at frequency $\omega_m$, generating two mixing products at $\omega_{in} \pm \omega_m$. The difference and sum frequency components undergo a second mixing stage with Q clock at frequency $\omega_m$, thus generating mixing products at $\omega_{in} \pm 2\omega_m$. The four mixing products at $\omega_{in}$ are in phase and can add up constructively, providing lossless transmission with $a = -\varphi_1 - 90° = -\varphi_2 + 90°$ phase shift. In the D to A direction, the same analysis shows that $a = -\varphi_1 + 90° = -\varphi_2 - 90°$ phase shift lossless transmission can be obtained. The resulting S-parameters are:

$$S = \begin{bmatrix} 0 & +e^{j(-\varphi_1 + 90°)} \\ +e^{j(\varphi_1 - 90°)} & 0 \end{bmatrix}$$

Thus, the phase-domain conditions for a non-reciprocal operation can be calculated as:

$$\begin{cases} e^{j(-\varphi_1 \pm 90°)} = \pm 1 \rightarrow \varphi_1 = 90° \\ -\varphi_2 + 90° = -\varphi_2 \pm 90° \rightarrow \varphi_2 = 270° \end{cases}$$

The non-reciprocal branch can be realized using a single- or dual-path configuration, wherein in the dual-path case, an additional quadrature path is placed parallel to the original path. While the dual-path structure is frequently used to minimize the adverse effects of duty cycle mismatch in I/Q clock generation [14], [18], we have utilized a single-path structure to achieve a compact die area. Our simulations show that using a single-path structure, reasonable levels of clock impairment still guarantee high-performance characteristics for the circulator. For instance, a 10% deviation from the 50% duty cycle would degrade the overall loss by 1 dB as shown in Fig. 2. Despite this degradation, the circulator loss based on a single-path non-reciprocal branch would still fall within the same range as the dual-path case. This is primarily due to the substantial impact of the ON-resistance (RON) of the switches, contributing to nearly one-third of the circulator loss [14]. By removing the quadrature path, we can effectively double the size of the switches, leading to a 50% reduction in RON while maintaining the same total parasitic capacitance as the dual-path configuration. Additionally, the simulations reveal that the circulator based on a single-path non-reciprocal branch maintains isolation levels over 20 dB and IP1dB over 14 dBm, even when subjected to a duty cycle deviation of up to 10%.

We have further reduced the die area by realizing the required lattice cells with coupled inductors as shown in Fig. 3. It is well-known that utilizing coupled inductors allows for achieving the intended inductance with nearly half the size required by using two separate inductors. In addition to the lattice capacitance itself, the layout of the coupled inductors introduces two parasitic shunt capacitances at the input and output of each lattice cell ($C_{PL} < C_{PO}$), arising from the capacitive coupling between the traces of the inductors. This helps to absorb a significant part of the parasitic capacitances of the switches into the reciprocal and non-reciprocal branches ($C_{PS} + C_{PL} \approx 2C_{PO}$). As a result, the implemented circulator can provide wider bandwidth and improved linearity compared to the previous designs.
Fig. 4: Measurement setup and chip photo (a), measured vs simulated loss/isolation (b), measured TX to ANI IIP3 (c).

Fig. 4a presents the measurement setup and microphotograph of the chip fabricated on a 28 nm CMOS process. Active die area is only 0.17 mm$^2$. We chose to operate with a modulation index of $3 \left( f_m = \frac{f_{n}}{3} = 7 \text{ GHz} \right)$ to prevent a significant decrease in bandwidth while facilitating clock generation, compared to $f_m = 21 \text{ GHz}$. The power consumption of the circulator is 28.8 mW from a 0.9 V supply voltage. We have used a differential vector network analyzer to measure the $S$-parameters by probing two differential ports at a time, while a mmWave probe terminated with a broadband termination is landed on the third port. The impedance matching at all ports is always below -10 dB. The measured loss and isolation results after calibration and de-embedding non-circulator losses are depicted in Fig. 4b. The circuit operates over a 1 dB bandwidth of 14-28 GHz, thus yielding a 66% fractional bandwidth, with a 3.8 dB IL and over 20 dB isolation. Finally, the circulator’s linearity performance has also been measured. The measurement setup limits the measured IP1dB of TX-to-ANT and the result depicts that the circulator does not yet compress at a TX power level of 10 dBm. The measured IIP3, on the other hand, shows the highly linear operation of the proposed circulator with an IIP3 of +19 dBm.

IV. CONCLUSION

This paper presents a compact and wideband passive CMOS circulator. We proposed (1) to use first-order lattice all-pass filters with coupled inductors to create the required phase shifts, and (2) to use four identical first-order cells in reciprocal and non-reciprocal branches. These techniques offer more compact, wideband, and predictable results. Table I shows the performance summary of the proposed circulator and compares it to the state of the art. The implemented circulator can provide state-of-the-art level characteristics in terms of loss, isolation, and linearity, while it is the most compact and wideband mmWave circulator structure reported.

ACKNOWLEDGMENT

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TABLE I: MEASURED PERFORMANCE COMPARISON

<table>
<thead>
<tr>
<th>Architecture</th>
<th>This work [6]</th>
<th>MWCL2014</th>
<th>Switched</th>
<th>Coupled</th>
<th>APN</th>
<th>Active</th>
<th>Current-Reuse</th>
<th>Active</th>
<th>Power Divider</th>
<th>Switched</th>
<th>LPF</th>
<th>Switched</th>
<th>BPF</th>
<th>Switched</th>
<th>APN</th>
<th>Switched</th>
<th>LPF</th>
<th>28nm</th>
<th>FDSOI</th>
<th>65nm</th>
<th>Parametric</th>
<th>NR TL</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS Process</td>
<td>28nm</td>
<td>25mm</td>
<td>180mm</td>
<td>180mm</td>
<td>45nm SOI</td>
<td>45nm SOI</td>
<td>40mm</td>
<td>28nm FDSOI</td>
<td>65nm</td>
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<tr>
<td>1dB BW (GHz)</td>
<td>14-28</td>
<td>21.5-2.5</td>
<td>24.17-24.55</td>
<td>22.7-27.3</td>
<td>50-56.8</td>
<td>5.6-7.4</td>
<td>0.05-3.5</td>
<td>92.5-107.5</td>
<td>10</td>
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<tr>
<td>LO Frequency (GHz)</td>
<td>7</td>
<td>N/A</td>
<td>N/A</td>
<td>8.35</td>
<td>8.6</td>
<td>1.3</td>
<td>1.65</td>
<td>10</td>
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<tr>
<td>IL (dB)$^3$</td>
<td>3.8/3.8</td>
<td>3.7/3.2</td>
<td>5.7/5.7</td>
<td>3.3/3.2</td>
<td>3.6/3.1</td>
<td>2/2.2</td>
<td>2.5/2.6</td>
<td>4.5/4.5</td>
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<tr>
<td>Isolation (dB)</td>
<td>$&gt;20$</td>
<td>$&gt;25$</td>
<td>$&gt;20$</td>
<td>$&gt;18.5$</td>
<td>$&gt;20$</td>
<td>$&gt;18$</td>
<td>$&gt;20$</td>
<td>$&gt;20$</td>
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<tr>
<td>Isolation BW (%)</td>
<td>66</td>
<td>16</td>
<td>1.6</td>
<td>18</td>
<td>14.6</td>
<td>28</td>
<td>200</td>
<td>15/1.6$^4$</td>
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<tr>
<td>IIP3 (dBm)</td>
<td>19</td>
<td>N/A</td>
<td>N/A</td>
<td>20/19.9</td>
<td>19.43/19.03</td>
<td>$&gt;17.5$</td>
<td>N/A</td>
<td>N/A</td>
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<tr>
<td>PWR (mW)</td>
<td>28.8</td>
<td>1.5</td>
<td>7.2</td>
<td>7.84</td>
<td>41.04</td>
<td>12.4</td>
<td>20</td>
<td>N/A</td>
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<tr>
<td>Area (mm$^2$)$^5$</td>
<td>0.17</td>
<td>0.615</td>
<td>0.715</td>
<td>2.16</td>
<td>1.72</td>
<td>0.45</td>
<td>0.96</td>
<td>0.245</td>
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</table>

1 Estimated from the measured results. The reported 2.5dB BW is 0.05-7GHz.
2 Estimated from the measured results. The reported 2dB BW is 85-110GHz.
3 TX to ANI / ANI to RX loss.
4 20dB isolation BW / 45dB isolation BW.
REFERENCES


