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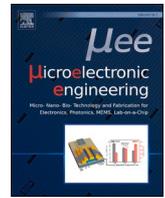
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Research paper

# Low-Temperature Wafer-Level Bonding with Cu-Sn-In Solid Liquid Interdiffusion for Microsystem Packaging

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## ABSTRACT

This work demonstrates the potential use of Cu-Sn-In metallurgy for wafer-level low-temperature solid-liquid interdiffusion (LT-SLID) bonding process for microelectromechanical system (MEMS) packaging. Test structures containing seal-ring shaped SLID bonds were employed to bond silicon and glass wafers at temperatures as low as 170 °C. Scanning acoustic microscopy (SAM) was utilized to inspect the quality of as-bonded wafers. The package hermeticity was characterized by cap-deflection measurements and evaluated through finite element modelling. The results indicate the bonds are hermetic, but residual stresses limit the quantitative analysis of the hermeticity. The microstructural studies confirm the bonds contain a single-phase intermetallic  $\text{Cu}_6(\text{Sn},\text{In})_5$  that remains thermally stable up to 500 °C. This work shows Cu-Sn-In based low-temperature bonding method as a viable packaging option for optical MEMS or other temperature-sensitive components.

## 1. Introduction

Wafer-level bonding is a cost-effective technology for microelectromechanical system (MEMS) packaging. The process enables components to be protected at the early manufacturing stage, which leads to an increase in production yield [1,2]. The main criterion of effective packaging is ensuring a hermetically sealed environment to maintain optimal device operation [3]. However, optical MEMS also requires the package to have a sensing “window”, which limits the choices of material [4,5].

The operating conditions of optical MEMS devices, such as microbolometers and micromirrors, require the cap to have good transparency for light to pass through while maintaining a hermetic environment. Thus, glass-based materials are often selected for their wide transparency window and low gas permeability [6,7]. Nonetheless, hermetic silicon-to-glass bonding process remains a challenging topic, mainly due to the thermomechanical stresses from high processing temperatures.

The glass frit is a commonly used method for silicon-to-glass bonding due to its high yield and good bond hermeticity. However, this process is typically conducted at high temperatures (>400 °C), could induce contamination to the components from the bonding material, and requires large footprints (>150 μm) [8]. Silicon-to-glass anodic bonding offers a much smaller footprint, but it is typically limited to ion-

conductive materials and requires applied voltage, which can damage some MEMS components [9]. Moreover, the bonding temperatures are still moderately high (>300 °C) [10]. Metal-based thermocompression bonding could be a solution for bonding at low-to-moderate temperatures (200–300 °C) [7,11]. Alternatively, room-temperature silicon-to-glass bonding has also been successfully reported with the help of plasma-activated surfaces [12]. However, the process typically requires very high surface quality (RMS < 0.6 nm) and cleanliness that comes with high fabrication costs [13,14].

Solid-liquid interdiffusion (SLID) represents a promising option for silicon-to-glass bonding. Compared to other bonding methods, the SLID process benefits from low-to-moderate processing temperatures and does not demand strict surface conditions. The resulting bonds have a higher remelting temperature than the processing temperature, low gas permeability, and adequate mechanical strength [15,16]. Furthermore, the bonds are electrically conductive, which means they can be utilized with through silicon or glass vias (TSVs/TGVs) to form vertical interconnects in heterogeneous integration [17].

SLID bonding based on Cu–Sn metallurgy is mostly used due to the materials' availability and relatively low bonding temperatures between 250 °C to 300 °C. However, the coefficient of thermal expansion (CTE) mismatch between the metal bonds and the substrates remains high and potentially leads to residual stresses during the cooling down process

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[18]. The maximum local stresses can be identified at the bond and substrate interface where CTE mismatch is highest [19]. While at wafer scale, temperature-induced stresses cause warpage, which results in varying device performance across the wafer [20,21]. Au–In based SLID bond offers a much lower bonding temperature of 180 °C. However, the system reacts readily at room temperature, creating problems in ensuring fresh bonding surfaces and causing multiple phases to form during the bonding process. Thus, the resulting bonds have poor thermal and mechanical stability [22,23].

Recently, wafer-level low-temperature SLID (LT-SLID) bonding based on the Cu–Sn–In ternary system has been successfully demonstrated to bond wafers at even lower temperatures. The bonding process was successfully conducted at temperatures as low as 150 °C, almost half of the processing temperatures of Cu–Sn based system. Moreover, this process has also been demonstrated to bond various wafers with CTE mismatches as high as  $4.6 \times 10^{-6} \text{ K}^{-1}$  [24]. In addition, microstructural and thermodynamic studies on the Cu–Sn–In metallurgy show the resulting intermetallic phase remains stable up to 500 °C [19,25]. Incorporating In to the Cu–Sn metallurgy is also expected to improve the bond's mechanical properties [26,27]. However, there are limited studies on LT-SLID for packaging applications. Consequently, this study would like to demonstrate the possibility to use Cu–Sn–In for MEMS packaging through silicon-to-glass bonding.

In this work, wafer-level LT-SLID bonding were carried out for bonding process at temperature as low as 170 °C. The process utilize seal-ring shaped features to form encapsulation. The hermeticity of the bonds was first investigated using scanning acoustic microscopy (SAM). Then cap deflection measurements were carried out using white light interferometry, and the results were assessed through finite element modelling. Microstructural characterizations and tensile tests were conducted to study the bond quality and strength.

## 2. Experimental method

### 2.1. Test vehicle fabrication and characterization

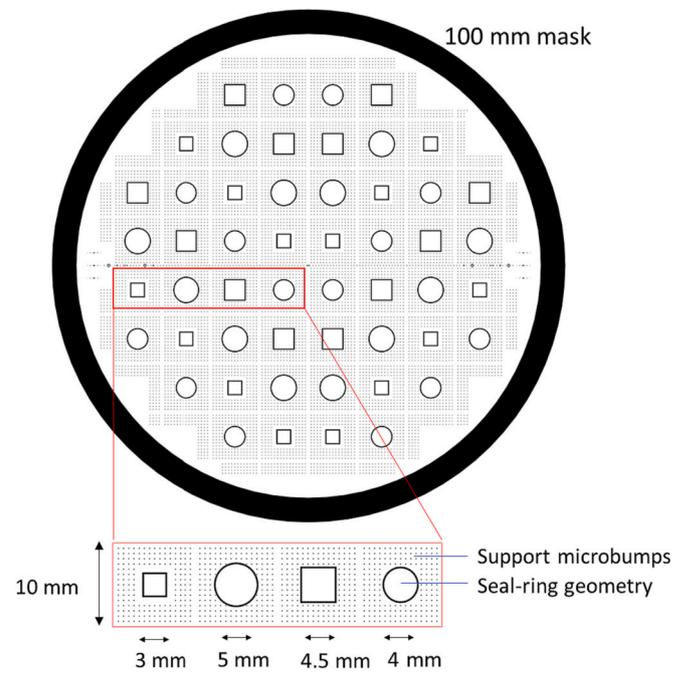
The details of the wafers and bonding temperatures used in this study are listed in Table 1. Borofloat®33 is a borosilicate glass with excellent transmissivity, good thermal resistance, and chemical durability, which make it suitable for micro- and optoelectronics packaging applications. The fabrication procedures were based on the processes presented in [19,24]. First, the backsides of the silicon wafers were patterned for dicing marks with lithography process followed by reactive ion etching. In preparation for the bonding process, 30 nm of TiW adhesion layer and 120 nm Cu seed layers were sputter deposited on the front side. Then, seal-ring type features were patterned using lithography process. Two types of seal-rings with different shapes and sizes were distributed over the wafer into 52 pieces of 10 mm × 10 mm chips, as illustrated in Fig. 1. Square support bumps with a width of 50 μm were also distributed surrounding the sealing ring to provide structural integrity. Cu–Sn–In metal stacks for the bonding process were then deposited by electroplating process with a thickness of  $3.5 \pm 0.2 \mu\text{m}$ ,  $1.8 \pm 0.1 \mu\text{m}$ , and  $2.3 \pm 0.4 \mu\text{m}$ , respectively. Prior to the bonding process, the photoresist was stripped, and TiW/Cu seed layers were removed.

During the bonding process, two wafer pairs containing symmetric patterns were optically aligned face-to-face using an EVG Smart-View®NT2 bond aligner and were subsequently bonded on an EVG520IS. First, the chamber was flushed with forming gas (4%H<sub>2</sub>/96%

**Table 1**

List of samples fabricated in this work.

No	Device Wafer	Cap Wafer	Bonding Temperature (°C)
1	Silicon	Silicon	200
2	Silicon	Silicon	170
3	Silicon	Borofloat®33	170



**Fig. 1.** Masks design for the test vehicle containing four types of seal-ring geometries.

N<sub>2</sub>). Then, the chamber was pumped down and when the vacuum conditions reached 0.1 Pa, the wafers were brought into contact with a contact force of 7.5 kN and heated up to their respective bonding temperature and kept for 1 h. During the bonding process, the vacuum was improved to  $10^{-2}$  Pa.

After the bonding process, the wafers were directly characterized with SAM. During this characterization, the bonded wafers were immersed in water which can be used as an initial qualitative test for the bond hermeticity. Leak test for defining seal-ring hermeticity based on helium bombing found in Mil-STD-883 K method 1014.15 could not be carried out for this work since the cavity volume used in this study is smaller than  $10^{-3} \text{ cm}^3$  [28,29]. Therefore, the hermeticity evaluation was carried out from cap deflection measurements from the silicon side using white light interferometry. This method has been reported for hermeticity detection of devices having small cavities [28,30,31]. In this experiment, Bruker Contour GT-X was used in vertical scanning interferometry mode, which yield precision in the nanometer range.

The wafers were then diced, and the deflection was remeasured using contact and optical profilometer. Some of the chips were then cross-sectioned for microstructural observation utilizing scanning electron microscopy (SEM) equipped with energy-dispersive spectroscopy (EDS), focus ion beam (FIB) and electron backscatter diffraction (EBSD). The bonds' mechanical strength was inspected through tensile tests. Shear strength test was not conducted to mitigate the effects of different failure modes coming from microbumps and seal-ring structure. Additionally, the melted metal could form a squeeze-out at the bond edge which also affects the accuracy of shear stress measurement. The tensile test set-up was designed according to the standard Mil-STD-883 K Method 2027.2 for estimating substrate attach strength, as closely as possible [29]. Ten chips from each sample type containing a 3 mm × 3 mm sized square-shaped seal-ring were mounted in copper brass studs. The studs were then installed into the mechanical tensile tester and a strain rate of 0.1 mm s<sup>-1</sup> was applied. After the mechanical tensile test, the fracture surfaces were directly characterized with SEM.

### 2.2. Finite element simulation

A finite element study was carried out in COMSOL Multiphysics® 6.0

to validate the cap deflection observed in the chips as a result of pressure difference. The structure used in the model is based on the circular sealing ring SLID bond with a diameter of 5 mm sandwiched between a 10 mm × 10 mm sized device (bottom) and cap (top) layer. The support microbumps were not included in the model for simplicity. Furthermore, since the model was axis-symmetric, only a quarter of the model was used for computational purposes as shown in Fig. 2(b).

Standard [100] silicon with a thickness of 380 μm is used as the device substrate. The seal-ring geometry has a width of 200 μm and Cu-Cu<sub>6</sub>(Sn,In)<sub>5</sub>-Cu structure with a thickness of about 2 μm, 6 μm, and 2 μm, respectively. Cu<sub>6</sub>(Sn,In)<sub>5</sub> was selected as the intermetallic layer material based on the experimental result, and its properties were obtained from [27]. The cap substrate was varied between silicon with a thickness of 380 μm and Borofloat®33 with a thickness of 500 μm. The material properties used in the simulation, except for Cu<sub>6</sub>(Sn,In)<sub>5</sub>, were obtained through the COMSOL Multiphysics® library and listed in Table 2.

In this work, two case studies were conducted to evaluate the cap deflection. The first one is cap deflection estimation without considering residual stress, while the second study implements residual stresses. The boundary conditions for the first study were as follows: First, a symmetry function was applied to the two quadrant cross-sections. Then atmospheric pressure of  $1.01 \times 10^5$  Pa was applied to the cap substrate, while the cavity internal pressure was varied between 0.1 and  $1.01 \times 10^5$  Pa, which refers to the cavity vacuum condition. Fixed constraints were applied to the sidewalls of the substrate since the modelled chip were assumed to be constrained by the neighbouring chips in the wafers. The 3D model in Fig. 2(b) illustrates the area where these boundary conditions were applied. For the second study, similar boundary conditions were applied to the geometry. Additionally, residual stresses were incorporated by adding a thermal expansion node to the model based on the work presented in [18]. To model the cooling down process, the initial temperature was set to the bonding temperature, while the final temperature was set to room temperature of 20 °C. Furthermore, the copper layer was assumed to be under plastic loading with an initial yield stress of 250 MPa and isotropic tangent modulus of 2 GPa [18,32].

### 3. Results and discussions

#### 3.1. Hermeticity investigation

Fig. 3 shows the SAM images taken from the as-bonded wafers under water immersion. No contrast variations were observed in the microbumps and seal-ring features, which means the formed bonds were

**Table 2**

Material properties used in the finite element simulation.

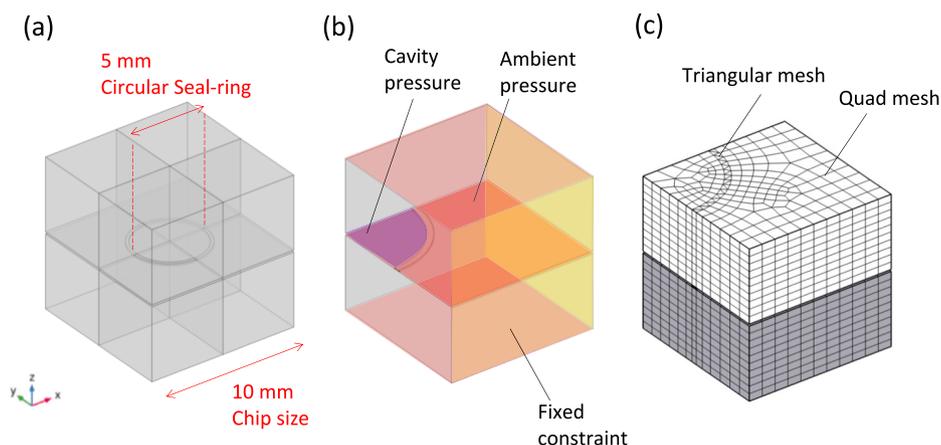
Materials	Young's Modulus (GPa)	Poisson's Ratio	CTE (ppm/°C)
Silicon	130	0.28	2.6
Borofloat®33	64	0.2	3.25
Cu	127.6	0.35	18.2
Cu <sub>6</sub> (Sn,In) <sub>5</sub>	149.5	0.29	20.16

homogenous. Areas with a darker shade denote where the water permeates between the wafers. The enlargement image on the 4 mm circular seal-ring in the center area shows that the water did not penetrate through the SLID bonding, implying that the bonds are impermeable to water. Additionally, globular shapes observed next to the seal-ring show a squeeze-out formation that indicates the melting of tin-indium.

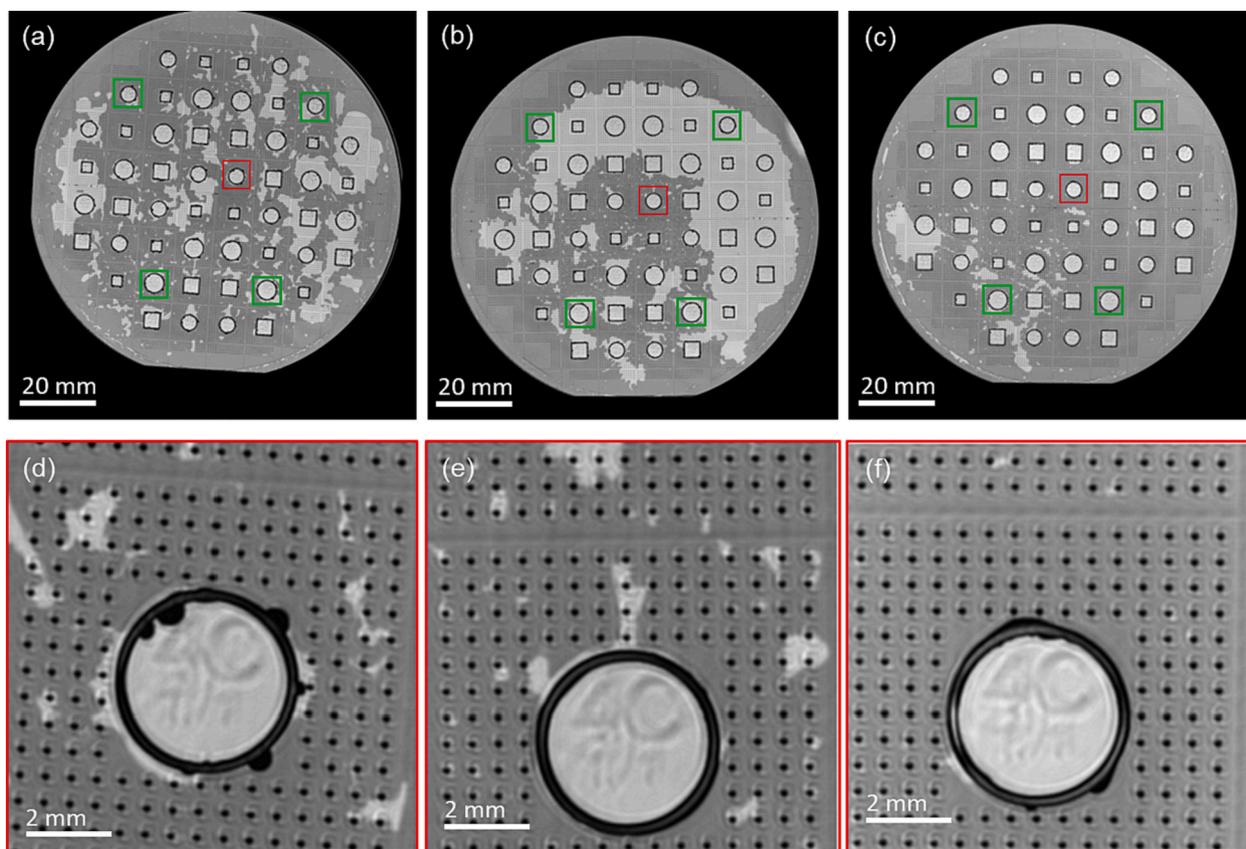
The hermeticity was further characterized using white-light interferometry to measure the cap deflection. It has been reported previously that hermetic encapsulation causes concave cap deflection due to the pressure difference between the ambient air and vacuum inside the packaging [32,33]. Fig. 4(a), (b), and (c) illustrates cap deflection measurements on the circular seal-ring chips located close to the edge of the wafer for each sample, as marked in Fig. 3. Based on the observations, concave cap-deflection for all samples occur in the range of 0.3 μm – 1 μm, which could be attributed to the pressure difference. However, cap-deflection measurements on the same chip observed in SAM presented in Fig. 3(d), (e) and (f), do not show that all chips exhibit any hermeticity from cap deflection, as presented in the supplementary fig. S1. This could mean although the seal-ring is watertight, it is not fully hermetic. White light interferometry characterization also highlighted that the surface of the chips was uneven, especially close to the edge, which could be attributed to the effects of residual stress and wafer warpage.

After the dicing process, the cap deflections were re-measured using a contact profilometer. Measurements conducted on four chips located close to the edge of the wafer, as marked in Fig. 3, show a maximum concave deflection of  $0.93 \pm 0.4$  μm for Si–Si bonded at 200 °C,  $0.86 \pm 0.5$  μm for Si–Si bonded at 170 °C, and  $1.22 \pm 0.3$  μm for Si-Borofloat®33 bonded at 200 °C. This shows that the hermeticity is retained through the dicing process. Fig. 4(d), (e), and (f) illustrate one of the cap deflections measured with a contact profilometer and a summary of the measurement is presented in supplementary table S2. The square-shaped dip observed in the profile comes from the RIE marking on the wafer's backside.

Due to the 380 μm silicon cap thickness used in this experiment, cap deflection could not be estimated using diaphragm deflection analytical



**Fig. 2.** (a) Single chip model containing seal ring geometry and (b) 3D representation of a quadrant of the chip used for finite element study. In the model, atmospheric pressure was applied in the areas shaded with red colour, cavity pressure was applied at the region shaded in blue, and fixed constraints were applied at the region shaded in yellow. (c) The model meshes. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)



**Fig. 3.** SAM images of the samples after the bonding process: (a,b) Si—Si bonded at 200 °C, (c,d) Si—Si bonded at 170 °C, and (e,f) Si-Borofloat®33 bonded at 170 °C. Red squares indicate the seal-ring enlarged at (d, e, f) and green squares indicate the seal-rings used in cap-deflection measurements. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Eqs. [31]. Therefore, the results from the cap deflection should be evaluated by finite element modelling. The graph in Fig. 5(a) shows the simulated deflection as a function of cavity pressure for the two study cases. The result shows cap deflection follows a linear trend as a function of cavity pressure. Without any residual stress estimation, the maximum cap deflection for both 380  $\mu\text{m}$  silicon and 500  $\mu\text{m}$  Borofloat®33 were around 110 nm, which differs significantly from the measured result.

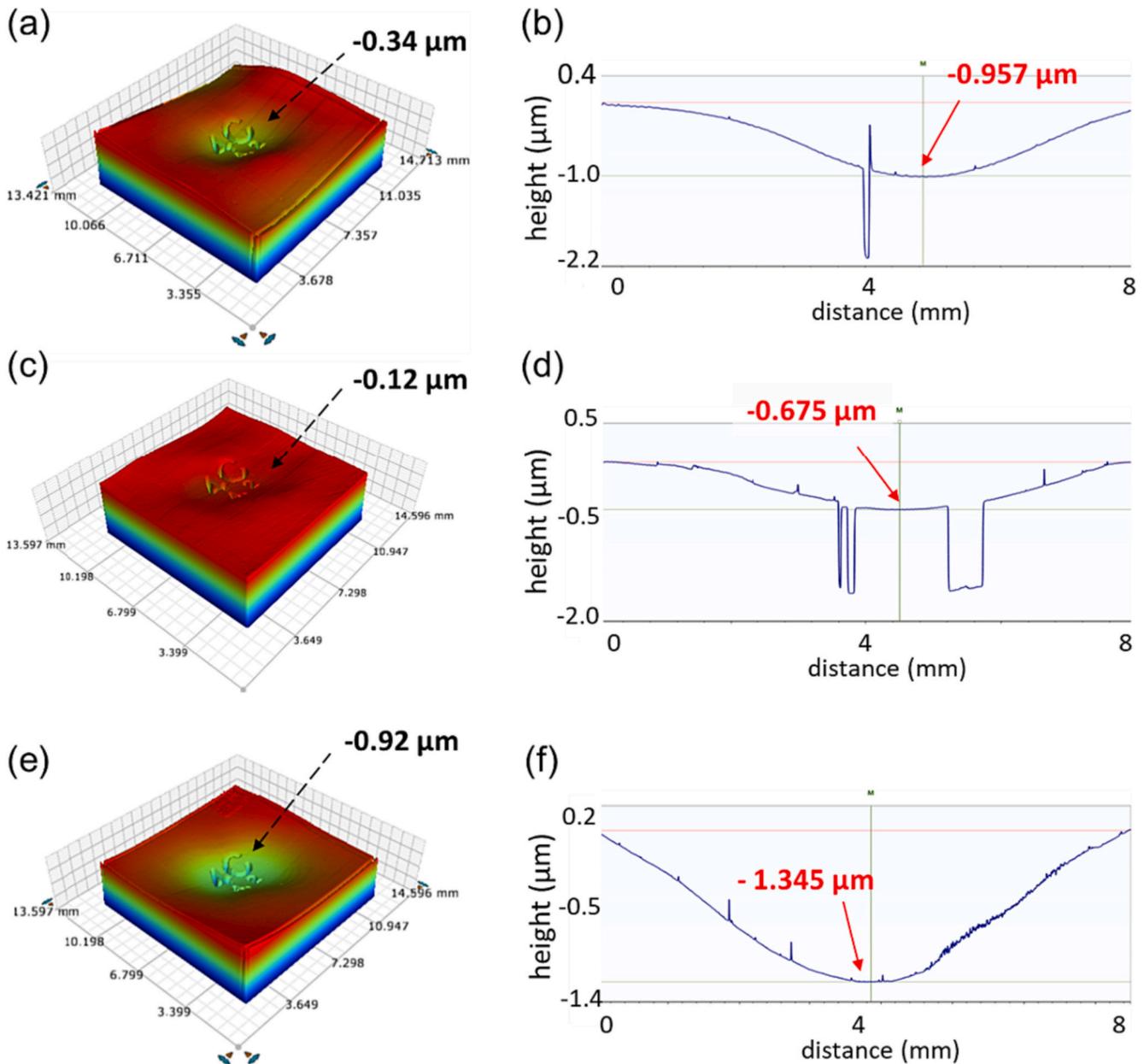
Interestingly, when residual stress was taken into account for the simulation, the cap deflection was estimated to be much higher. This simulation agrees with the results reported in [32], which reported inward deflection caused by residual stress for a sealed cavity. Furthermore, the simulation also shows that after the cavity loses its vacuum, i. e. cavity pressure is the same as ambient pressure, the cap deflection remains quite significant. These residual stress effects become more prominent with increasing bonding temperature and higher CTE mismatch, as in the case for bonded Si-Borofloat®33 wafer pairs. Fig. 5 (b) shows the measured cap deflection superimposed with the simulated cap deflection. Initial measurement shows a profile that is closer to the simulated values incorporating the effect of residual stress. This emphasises that the residual stress does play a critical factor in the resulting cap deflection. This observation also explains the observed results which show bonded Si-Borofloat®33 has a higher maximum deflection ( $1.22 \pm 0.3 \mu\text{m}$ ) in comparison to the bonded Si—Si ( $0.93 \pm 0.4 \mu\text{m}$  at 200 °C,  $0.86 \pm 0.5 \mu\text{m}$  at 170 °C). Large variations observed in the measurements results can be attributed to several factors. One possibility is the fluctuating cavity vacuum level during the bonding process due to materials outgassing and changes in vacuum before the bond is fully formed [28]. Another possibility could also be attributed to the non-uniform residual stress due to the differences in the electroplated metal thickness.

### 3.2. Bond microstructure

Fig. 6 summarizes the microstructural observations on the seal-ring cross-sections. The micrographs show that a good bond was formed connecting the two wafers. The bond structure consisted of an intermetallic layer sandwiched between the copper layers, that means not all copper has been consumed to form the intermetallic phase. The observed bond thickness variations between the samples from different bonding parameters are caused by height variations during the electroplating process and squeeze-out.

EDS analysis results on the intermetallic layers are summarized in Table 3. The elemental compositions show that the intermetallic has approximately equal ratio of In and Sn, which indicates that the elements are intermixed properly during the bonding (or during the formation of the liquid phase). Furthermore, the observed Cu to (Sn,In) ratios are close to the Cu—Sn ratio observed in  $\text{Cu}_6\text{Sn}_5$  phase, which means that the phase formed is  $\text{Cu}_6(\text{Sn,In})_5$ . The results agree with the report that In has a higher solubility and larger stabilizing effect on  $\text{Cu}_6\text{Sn}_5$  compared to  $\text{Cu}_3\text{Sn}$  phase, causing a smaller driving force for copper to diffuse into the intermetallic to form  $\text{Cu}_3\text{Sn}$  [25]. Hence, making  $\text{Cu}_6(\text{Sn,In})_5$  more stable phase compared to  $\text{Cu}_6\text{Sn}_5$  in the conventional Cu—Sn system. The formation of  $\text{Cu}_6(\text{Sn,In})_5$  does not consume as much copper as  $\text{Cu}_3(\text{Sn,In})$ , which explains the remaining copper thickness after the bonding process.

High-resolution cross-section of the bond area using FIB-SEM reveals that the black spots observed on the bond cross-section in Fig. 6(a), (b), and (c) as microvoids. The high-resolution image also shows a possible, crack-like, hairline defects in the center of the intermetallic layer. Despite the observed defects, cap-deflection measurements indicated that the seal-ring could maintain hermeticity. This means the microvoids



**Fig. 4.** The cap deflection measured in optical and contact profilometer for (a,b) Si—Si bonded at 200 °C, (c,d) Si—Si bonded at 170 °C, and (e,f) Si-Borofloat@33 bonded at 170 °C.

are forming locally, and the crack-like defects do not extend through the seal-ring. In another word, the hairline defects might represent locally formed non-bonded areas, which were analyzed further using EBSD characterization.

In addition, for the samples that are bonded at 200 °C, Kirkendall voids at the interface between Cu and intermetallic layers could be observed, which indicates the formation of a thin layer of  $\text{Cu}_3(\text{Sn},\text{In})$ . Furthermore, these voids suggest possible impurities existing in the electroplated copper that inhibit the copper diffusion to the intermetallic layer [34]. Nevertheless, based on the hermeticity measurements, it can be assumed that the Kirkendall voids also have minimal impact to the hermeticity.

Fig. 7 summarizes the EBSD and EDS analyses on the cross-section of bonded Si—Si at 170 °C. The grain contrast images from EBSD highlight that intermetallic consisted of two different grain structures. At the Cu-(Sn,In) interface, the grains was observed to have smaller size, causing areas with darker contrast. While at the center of the bond, the grains

have developed into a larger columnar structure, following the growth structure of hexagonal  $\text{Cu}_6(\text{Sn},\text{In})_5$ . The elemental mapping presented in Fig. 7(d) and (e) shows a homogenous distribution of Sn and In across the intermetallic, which means the intermetallic is composed of a single phase, despite the differences in grain size. One of the possible reasons for the duplex microstructure is the difference in the interdiffusion rate. The relatively slow diffusion rate of (Sn, In) through the  $\text{Cu}_6(\text{Sn},\text{In})_5$  to copper layer causes the grains at the interface to be smaller. While, a relatively faster Cu diffusion rate to the (Sn,In) melt through  $\text{Cu}_6(\text{Sn},\text{In})_5$  resulted in larger grain sizes [35].

Furthermore, the EBSD characterization highlights the grain structure differences in the areas with and without the crack-like defects observed at the cross-section. Grain contrast image at the bond without hairline defects shows a single columnar  $\text{Cu}_6(\text{Sn},\text{In})_5$ . This indicates that grains grow from both sides of the bond and merged into a single columnar grain [36]. On the other hand, the grain contrast of the cross-section containing crack-like defects shows the two grains that grow

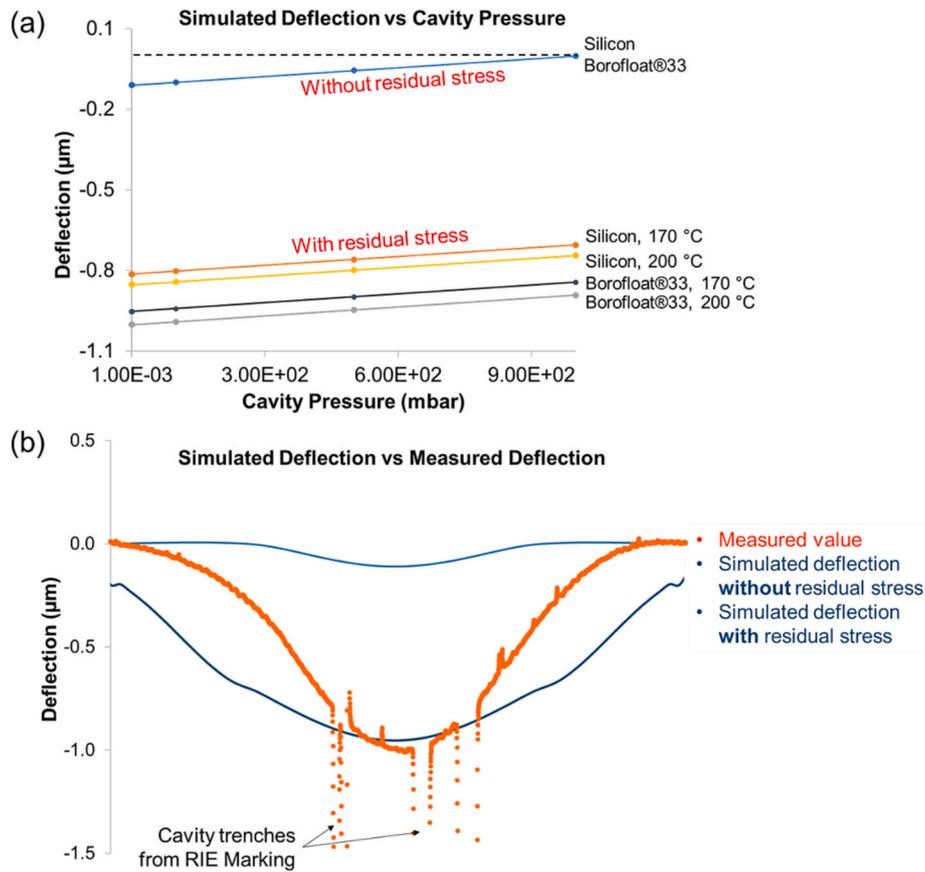


Fig. 5. (a) Simulated maximum cap deflection for two different cap materials as a function of pressure and effect of residual stresses, and (b) Measured cap deflection superimposed with simulated cap deflection for Si–Si bonded at 200 °C.

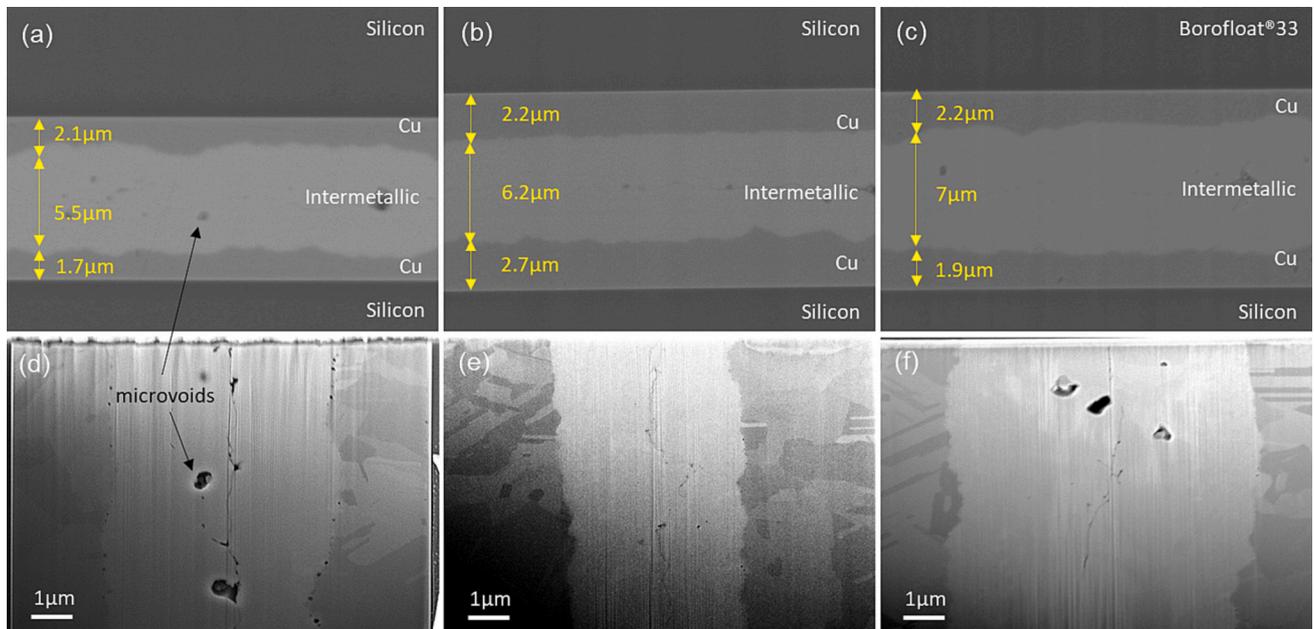


Fig. 6. SEM and FIB cross-section image for (a,b) Si–Si bonded at 200 °C, (c,d) Si–Si bonded at 170 °C, and (e,f) Si-Borofloat@33 bonded at 170 °C.

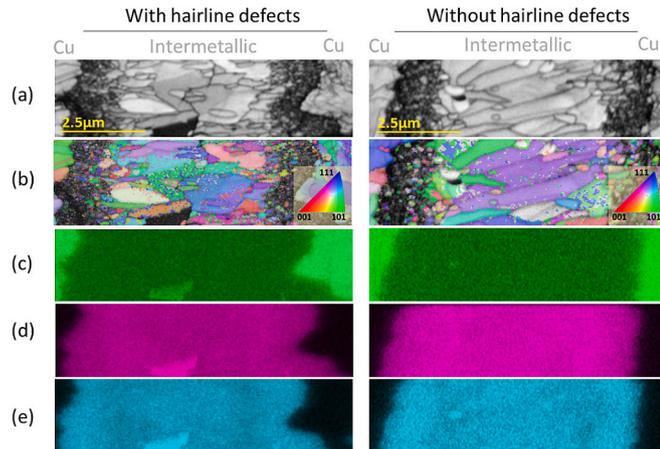
from both substrates did not merge. This confirms that there is a non-bonded area at the center of the bond.

Probably the reason for this crack-like defect is an oxide layer on the metal stack surface that is trapped when the substrates were brought into contact during the bonding process. Another possible explanation

could be a defect formation at the bond-interface grain boundaries. It has been reported that hexagonal close-packed (hcp) metals, which typically have a preferred growth direction along the c-axis, are susceptible to slip defects under compression loading [37,38]. Previous works has shown that the Cu<sub>6</sub>(Sn,In)<sub>5</sub> phase grows in an hcp P6<sub>3</sub>/mmc

**Table 3**  
Intermetallic layer elemental composition at different bonding temperature.

Bonding Parameter	Elemental Composition (at. %)		
	Cu	Sn	In
Si-Si bonded at 200 °C	56.23 ± 1,1	21.32 ± 0.5	22.44 ± 0.6
Si-Si bonded at 170 °C	54.8 ± 1.3	21.57 ± 1	23.64 ± 2.3
Si-Borofloat®33 bonded at 170 °C	56.15 ± 0.7	21.74 ± 0.4	22.11 ± 0.8

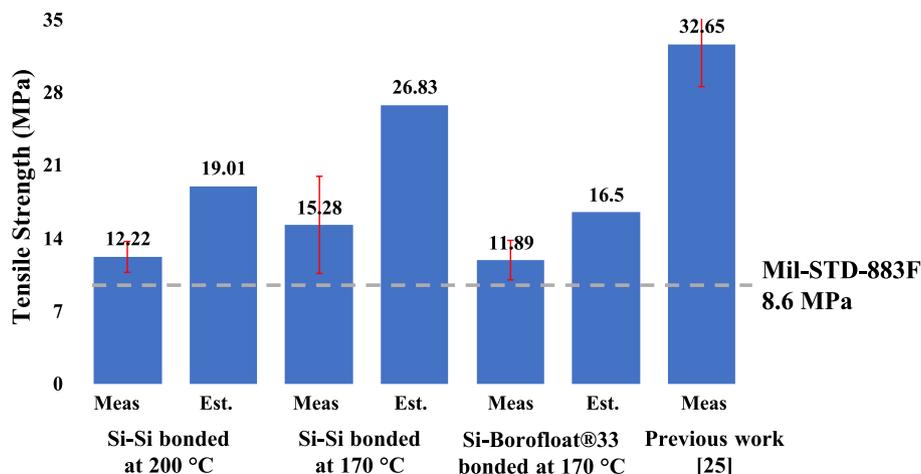


**Fig. 7.** EBSD Characterization for Si—Si bonded at 170 °C with and without hairline defects. (a) Grain contrast, (b) inverse pole figure (IPF-Z) maps (inset showing the grain orientations), (c) Cu, (d) Sn, and (e) In EDS elemental map.

orientation similar to Cu<sub>6</sub>Sn<sub>5</sub> [19,39], which is also confirmed through the EBSD characterization. The pole figure measurements presented in Fig. 7(b) and more detailed in supplementary fig. S3 show that the grains of the sample without defect grows at an angle close to the c-axis orientation, while the sample with hairline defect shows that the grains do not. This indicates that the growth could result in the grains either diffusing together if they are growing at a preferred angle or resulting in defects with clearly distinguished grain boundaries. Nevertheless, the possibility of a defect in the bond area could imply an effect on the bond strength.

**3.3. Mechanical tensile strength and fracture surfaces**

Fig. 8 summarizes the measured tensile strength of the Cu-Sn-In based SLID bonds. The measured results show values that are more than the minimum required strength of 8.6 MPa for substrate attach



**Fig. 8.** Measured (Meas.) and estimated (Est.) tensile strength of seal ring. Error bars show standard deviations of the measured tensile strength.

based on the Mil-STD-883 method 2027.2. However, the average values are much lower than Cu—Sn based SLID bonds with measured tensile strength of 90 MPa [15,40]. Mainly due to the mechanical strength of Cu<sub>6</sub>(Sn,In)<sub>5</sub> that are much lower than Cu<sub>3</sub>Sn. Interestingly, the reported strength of Cu<sub>6</sub>(Sn,In)<sub>5</sub> from this work was also smaller than results reported in [19]. Upon inspection of the fracture surfaces of the seal-ring after the mechanical tensile test, two types of failure mechanisms were identified, which are presented in Fig. 8.

One of the failure modes could be attributed to the intermetallic layer and occurs at most parts of the seal-ring, coloured in light grey in Fig. 9. A detailed SEM micrograph on the intermetallic fracture surface presented in Fig. 9(e) shows that the surface was inhomogeneous, which implies that the non-bonded interface might be the cause of this local effect. Additionally, the fracture surface also confirms that the microvoids observed in the SEM are forming locally and do not penetrate through the seal-ring.

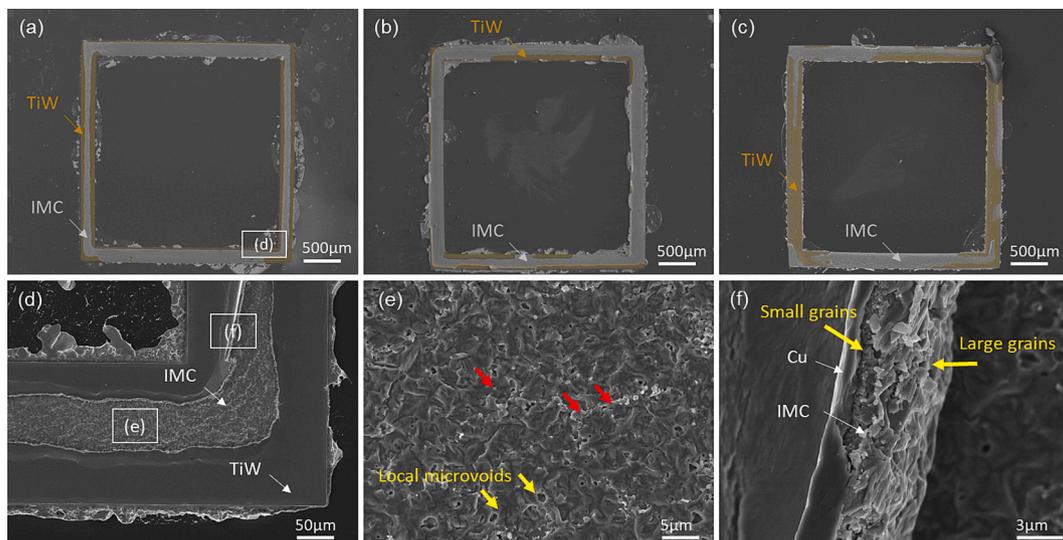
The other failure modes can be attributed to the adhesion failure between TiW and Si, marked in the micrograph at Fig. 9(a), (b) and (c) with yellow colour. Failures occurring at the adhesion layer might indicate that the bonds are fully formed at this location of the seal-ring, and the weakest link in the bond is located in the Si-TiW adhesion [41]. Moreover, all the support bump failures were observed to occur on the Si-TiW adhesion layer. Additionally, detailed fracture surface presented in Fig. 9(f) also confirms that the bond has a duplex microstructure where at the Cu-(Sn,In) interface small grain sizes of <100 nm were observed, hence confirming the region with darker contrast in EBSD. Additional fracture surface images and EDS characterization are presented in fig. S4 and table S5 in the supplementary files.

Based on the fracture surface micrographs and cross-sectional observations, a reconstruction of the seal-ring structure can be illustrated as shown in Fig. 10. The non-bonded area and squeeze out do not contribute to the bond strength.

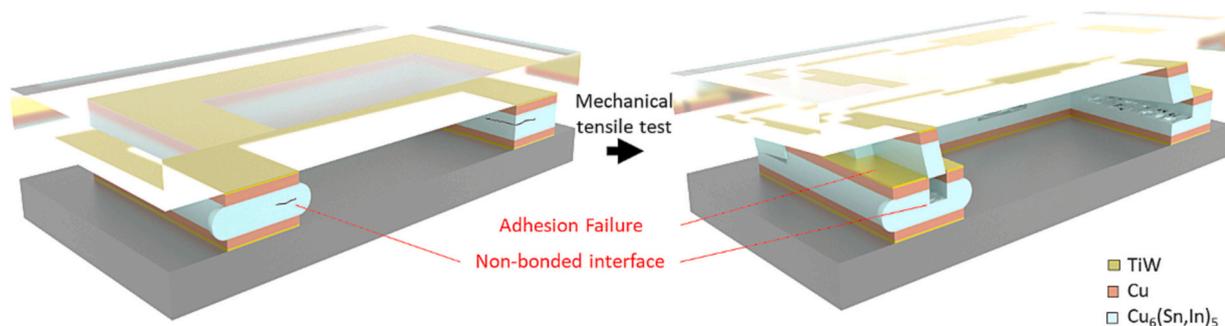
Therefore, a recalculation of the measured tensile strength based on the successfully bonded area was conducted to estimate the bond's strength if there were no non-bonded area (no hairline defects). The equation used to project the measured tensile strength was as follows:

$$\sigma_{est} = \frac{\sigma_{meas} \cdot A}{(A_{sup} + A_{bond})} \tag{1}$$

Where  $\sigma_{meas}$  represents the measured tensile strength, A is the total area of the sealing ring (4 mm<sup>2</sup>), A<sub>sup</sub> is the area of the supporting bump (1.76 mm<sup>2</sup>), and A<sub>bond</sub> represents the area failing at the adhesion layer. A<sub>bond</sub> values were obtained as a result of post-processing method on the backscattered electron image of the sealing ring using ImageJ software. The backscattered electron image was used as it shows better contrast by atomic weight used to differentiate silicon, intermetallic layer, and TiW



**Fig. 9.** SEM image on the fracture surface of (a) Si—Si bonded at 200 °C, (b) Si—Si bonded at 170 °C, and (c) Si-Borofloat®33 bonded at 170 °C. The area shaded in yellow marked the fracture occurring at the adhesion layer. (d,e,f) Detailed fracture surface SEM image (Area pointed out by red arrows shows the surface was inhomogeneous). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)



**Fig. 10.** Illustration of the SLID bond seal-ring structure and its failure mechanism after tensile testing. Non-bonded interfaces cause failures in the intermetallic layer, while successfully bonded areas fail at the adhesion layer.

adhesion layer. The highlighted area in yellow in Fig. 9 was obtained as a result of post-processing using the ImageJ software. The percentage of the area of the bond failing at adhesion are found as 49.19% for Si—Si bonded at 200 °C, 21.69% for Si—Si bonded at 170 °C, and 34.96% Si-Borofloat®33 bonded at 170 °C, respectively. Based on the calculation, the estimated strength was closer to the previously reported value, which strongly suggest that the non-bonded area was detrimental to the mechanical strength.

#### 4. Conclusions

In this study, low-temperature wafer-level SLID bonding based on Cu-Sn-In metallurgy has been successfully demonstrated using seal-ring structures. The bonding processes were conducted at temperatures as low as 170 °C to bond Si—Si wafer pairs and Si-Borofloat®33 wafer pairs. SAM characterization indicated that the as-bonded wafers were hermetic and have high bond quality.

The hermeticity of the bonds was further assessed by cap deflection measurements before and after the dicing process. Then, finite element modelling was used to supplement the measurement results. The simulation results support the conclusion of the bonds' being hermetic. However, residual stresses caused by CTE mismatch limits quantitative analysis of the package hermeticity.

Microstructural studies on the seal-ring cross-sections showed the bonds are composed of residual copper metallization and a single-phase intermetallic  $\text{Cu}_6(\text{Sn},\text{In})_5$  layers. Detailed analyses using FIB and EBSD

showed that the bonds contain some local microvoids that are not detrimental to the hermeticity but may influence on the mechanical strength. Minimal void formation and increased bond strength was observed from samples formed with lower bonding temperature of 170 °C.

This work presents a promising alternative for silicon-to-glass metal bonding for microsystem packaging. Further work should be done to further assess the package reliability, by considering several factors. First, utilizing even lower bonding temperature, given that the ternary metallurgy of Cu-Sn-In allows, to further reduce the residual stress effect. Second, utilizing larger cavities for quantitative measuring the hermeticity. Finally, implementing oxide cleaning step and improving metal stack deposition process to minimize the interface defects.

#### Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

#### Data availability

Data will be made available on request.

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## Appendix A. Supplementary data

Supplementary data to this article can be found online at <https://doi.org/10.1016/j.mee.2024.112140>.

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