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Investigative characterization of delamination at TiW-Cu interface in low-temperature bonded interconnects

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ABSTRACT

The trend for heterogeneous integration has driven the need for a low-temperature bonding process. Cu-Sn-In based solid-liquid interdiffusion (SLID) bonding technology has been presented as a viable option. However, previous studies have also reported that issues might exist in the interconnect interface towards the substrate, leading to the formation of intermetallic layers at undesired locations. This study carried out a series of characterization methods to determine the root cause of this issue. Cross-sectional observations showed that the problem occurs particularly at the TiW-Cu interface. Examination of the adhesion layer showed possible impurities existing in the layers, compromising its adhesion to copper. Residual stress analyses displayed opposing loading conditions at the interface. The interplay of the two factors resulted in the delamination of the TiW-Cu interface, leading to a pathway for Sn—In atoms. Furthermore, several methods are proposed to mitigate this issue.

1. Introduction

Heterogenous integration has become an established trend in microelectronics packaging. [1] The demands for functionalities and computing power are ever-increasing, while the need to scale down persists. Thus, microbumps technology becomes prominent as an integral part of forming connections between the devices. [2,3] Combined with through silicon vias (TSVs), microbumps can form high-density interconnects to maintain a small form factor. This gives the advantage of a shorter transmission distance, leading to faster signal transmission and low signal attenuation. [1,4] Furthermore, the technology allows vertical interconnects, prompting the use of a third dimension in device integration. [5,6]

Interconnects formed of copper and joined by a soldering approach have dominated the market for years. [3] Cu-based interconnects are attractive for the material's availability and good conductivity. These types of technology have been developed for interconnects with a pitch size as small as 10 μm. [2,7] However, fine pitch interconnects <10 μm are proven challenging to fabricate, which poses a problem for creating higher density interconnects. [7] Hybrid bonding technology was introduced as a solution for high-density interconnects. The process could be done at a relatively low temperature, which makes it very attractive. However, creating a very good surface quality (rms <0.5 nm) for the bonding process remains challenging and costly. [8,9] Alternatively, solid-liquid interdiffusion (SLID) bonding technology is a relatively more available bonding process. The process forms an interconnect from high-temperature melting material, typically Cu, and low-temperature melting material through intermetallic reactions. Several options of low melting materials, such as Sn ($T_m \sim 235$ °C) or In ($T_m \sim 157$ °C), allow varying bonding temperatures to fit different applications and do not have strict surface quality requirements. Furthermore, the resulting bond has a high remelting temperature (>400 °C), that allows SLID interconnects for consecutive higher processing temperatures. [10]

One feature that is commonly found in these high-density interconnects is the multi-layered structure. Various layers of different materials are often stacked to form the under-bump metallization (UBM) of the copper pillars or microbumps. Each layer functions as an electrical connection, adhesion, diffusion barrier, wear protection, and/or thermal insulation. [11] However, due to inherently different properties of each layer, the structures often face challenges due to materials compatibility. For instance, a diffusion barrier layer is employed to prevent interdiffusion of the copper-based bumps with silicon substrates or contact metallization layer. [12,13] However, copper's poor adhesion with the

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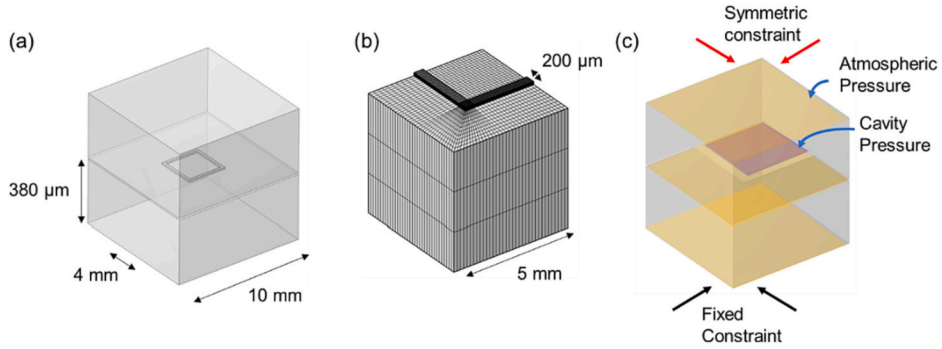

Fig. 1. (a) Illustration of square-shaped test structure contained in a single chip, (b) A quarter of the chip used as the model in finite element study (cap layer was removed for visualization), and (c) boundary conditions applied to the model. Yellow colored was area applied with atmospheric pressure, and purple colored area was applied with cavity pressure. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

barrier necessitates the use of an adhesion layer. [14]

Impurities and processing parameters are among the factors that affect the final layer quality. [15,16] Impurities during processing could affect the layer performance or induce defects that could lead to failure. [17] The deposition processes of thin films are known to cause intrinsic stress build-up due to various elements, such as lattice mismatch or final thickness. [18,19] Furthermore, varying coefficients of thermal expansion (CTE) induce temperature-related issues. [20] Potentially leading to structural failure, causing contact loss in microbumps or compromising hermeticity in a seal-ring-based application. [20,21]

In a recent study, the SLID bonding process based on Cu-Sn-In was demonstrated as a potential candidate for low-temperature wafer-level bonding. [22] Thermodynamic studies reported that Sn—In alloy has eutectic behavior that reduces the melting point of low-temperature metals to 112 °C. [10,23] Moreover, the addition of indium stabilizes the Cu_6Sn_5 phase, which has a remelting temperature > 500 °C, and also increases Cu solubility that can shorten bonding time. [22,24] This process has been successfully demonstrated for bonding temperatures down to 150 °C, which is lower than the melting point of In, and forms interconnect composed of a single $Cu_6(Sn,In)_5$ phase. [25] The process has also been demonstrated to bond silicon wafers with other substrates with dissimilar thermomechanical properties, such as borosilicate glass. [26,27] However, tensile tests conducted in resulting interconnects exhibited failures at the interconnect-to-substrate interfaces, particularly at the adhesion layer. [28] There have been some observations where intermetallic compounds have formed between copper and the substrate. [26] This strongly suggests that unresolved issues exist within the multi-layered interface.

Hence, in this work, an investigation was carried out to study the problems existing in the interface between the Cu-Sn-In SLID interconnect and the Si substrate. Wafer-level SLID bonding process using Cu-Sn-In metallurgy was utilized to fabricate test structures of bonded Si and glass wafers. Diffusion kinetic and thermodynamic analyses were utilized to build the initial hypothesis on the problem origin. Then, a series of characterization techniques were carried out to observe and determine the cause of the issues in the interconnect-to-substrate interface.

2. Experimental method

2.1. Test structure fabrication

In this study, two types of wafer pairs were bonded using Cu-Sn-In based SLID method: Si-Borofloat®33 and Si—Si. The interconnects' fabrication procedure follows the process that has been described in [26]. The manufacturing process started with patterning dicing mark on the backside of silicon wafers with lithography, followed with reactive ion etching for 2 min. Then, the photoresists were stripped in ultrasonic-agitated acetone bath for 10 min and IPA for 2 min. All wafers were then deposited with adhesion and seed layer in preparation of the metal stack deposition. MRC 903 Sputtering Deposition System was utilized as the deposition equipment. TiW (10 wt% Ti) adhesion layer with a thickness of 15 nm was deposited twice using RF magnetron sputter (0.3 kW) at room temperature. Subsequently, 100 nm Cu seed layer was deposited using DC magnetron sputter (1.1 kW) without breaking the vacuum conditions. During both deposition processes, Argon gas was injected into the deposition chamber and the pressure was kept roughly at 0.5 Pa.

Two seal-ring type structures, circular and square-shaped, as described in [27] were then patterned using standard lithography process. Fig. 1(a) depicts the dimensions of the square-shaped seal-ring. Next, the wafers were treated with oxygen plasma for 3 min to improve surface wettability. Metal layers stack for the bonding process were then electro-deposited with a thickness of 3.5 ± 0.2 µm for Cu, followed by Sn and In layers with a thickness of 1.8 ± 0.1 µm and 2.3 ± 0.4 µm, respectively.

Prior to the bonding process the photoresist was stripped in ultrasonic agitated stripping solution. Then, the unpatterned Cu seed layer was removed with wet etching process in NB tech Cu-etch-150 solution and rinsed with DI water afterwards. Subsequently, the unpatterned TiW layer was removed with H_2O_2 at 60 °C, and the wafers were cleaned with DI water. The wafers were then bonded under vacuum level of 0.1 Pa, contact force of 7.5 kN, and hold temperature of 170 °C for 1 h. The bonded wafers were then cooled down to 150 °C before the contact force was released. After the bonding process, the wafers were diced into 10 × 10 mm^2 chips for characterization. In addition, some of the chips were kept at high-temperature storage (T = 150 °C) to inspect the intermetallic phase stability.

2.2. Characterization methods

2.2.1. Microstructural characterization

Microstructural studies were carried out by scanning electron microscopy (SEM) imaging on the seal ring cross-section. The imaging was conducted on the as-bonded chips, and the chips that have been annealed/thermally aged at 150 °C for 6 h and 168 h. In preparation for the microstructural study, the chips were molded into epoxy resin, continued by mechanical grinding to expose area of interest. The samples were then polished with diamond polishing suspension and coated with chromium. Semi-quantitative elemental analysis was carried out using electron dispersive spectroscopy (EDS) within the SEM.

TEM lamella preparation was done using a JEOL JIB-4700F dual-beam system using an in-situ lift-out process from a molded cross-section. Transmission electron microscopy (TEM), scanning transmission electron microscopy (STEM), and select area electron diffraction (SAED) were conducted using the JEOL JEM-2200FS Cs-corrected microscopy. EDS was carried out using the JEOL JEM-2800. Both microscopes were operating at 200 kV.

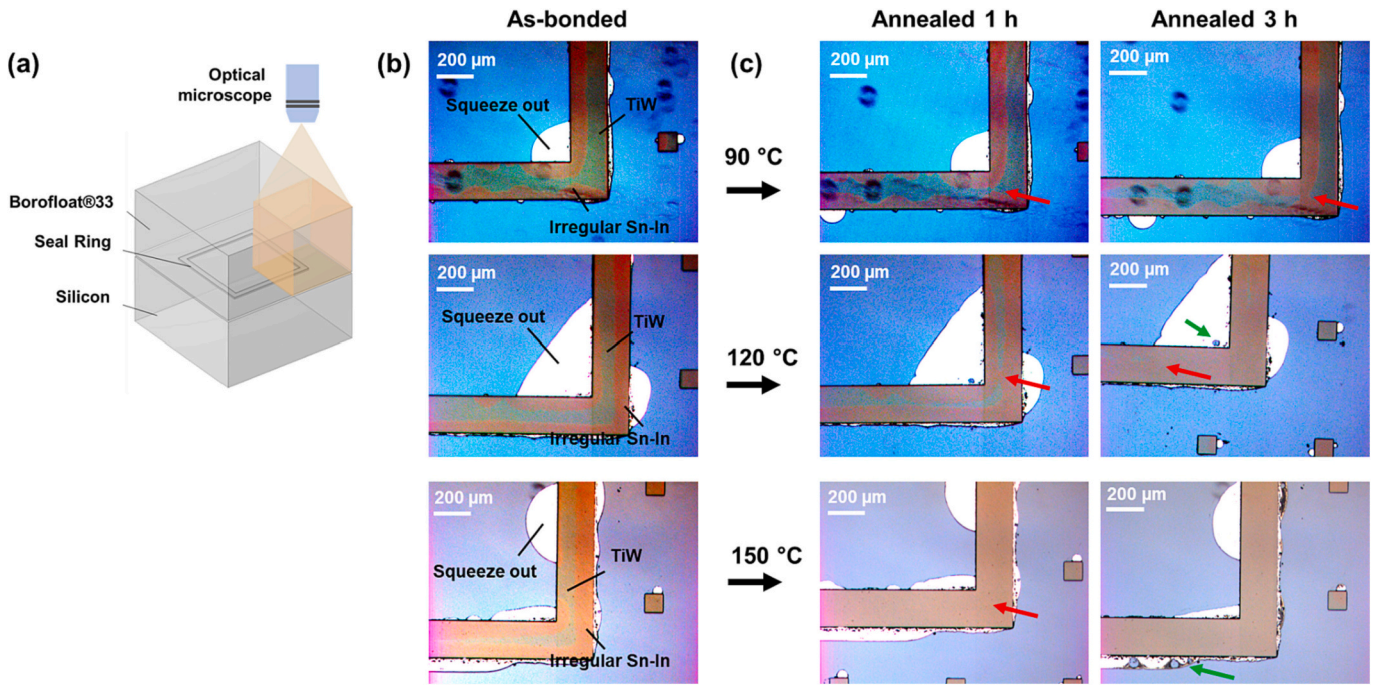

Fig. 2. (a) Illustration of optical microscopy observation for bonded Si-Borofloat®33, (b) the observed results of as-bonded samples and (c) the observed results after heat treatment at different temperatures and time. Dark orange-colored areas show the region where the Sn—In had diffused and formed Cu-Sn-In intermetallic. The red arrows marked the area where diffusion occurs prominently after annealing and green arrows marked the area where unreacted Sn—In are missing from squeeze-out region. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

2.2.2. Thin film characterization

Wafer-level residual stresses caused by the thin-film deposition were investigated using wafer curvature analysis. The curvature data was obtained using FLX-2320 equipped with laser of 670 nm wavelength. The measurements were conducted on the backside patterned silicon wafer: after the deposition of TiW adhesion layer, deposition of TiW-Cu seed layers, after seed layers removal and after the bonding process. The residual stress values were obtained through analytical calculation using Stoney's equation.

Time-of-flight elastic recoil detection analysis (TOF-ERDA) was used to study the elemental and impurity composition of adhesion and seed layers. It was performed with a 40 MeV beam at the 5 MV tandem accelerator of the University of Helsinki. The experiment was conducted in a horizontal geometry with an incident angle on the sample surface at 16° and a forward scattering angle at 40°. The system consists of a time-of-flight telescope with two timing gates and an energy detector. The length of the telescope was 684 mm, apertures of timing gates were 12 and 18 mm in diameter, and time resolution was 150 ps. The energy detector with a resolution of 18 keV was placed at a distance of 1243 mm from the sample and used for particle mass separation. Absolute error due to statistical uncertainty in the measurements was <1%. The reader is addressed to [29] for a more detailed description of the setup.

2.2.3. Finite element study for local residual stress

Local residual stresses as a result of cooling down process were studied by finite element analysis using COMSOL 6.1. The model uses a quarter of the single chip structure containing SLID bond with a ring width of 220 µm and side length of 4 mm, as illustrated in Fig. 1(b). The seal ring layered structure is composed of 30 nm TiW, 2 µm Cu, 6 µm $Cu_6(Sn,In)_5$, 2 µm Cu, and 30 nm TiW. To mimic the original structure, the seal ring was sandwiched between 380 µm silicon wafers that act as device (bottom) and cap (top) layer. The material properties used in the simulation were obtained through the COMSOL Multiphysics® library and listed in supplementary table 1. $Cu_6(Sn,In)_5$ Young's Modulus, in particular, were not presented in the library and was obtained from [30].

The boundary conditions for the first study were as follows: First, a symmetry function was applied to the two-quadrant surfaces containing seal-ring cross-sections. Fixed constraints were applied to the sidewalls of the substrate since the modelled chip was assumed to be constrained by the neighboring chips in the wafers. Then atmospheric pressure of 1.01×10^5 Pa was applied to the cap substrate, while the cavity internal pressure was 0.1 to Pa, which simulates vacuum encapsulation. Residual stresses were incorporated by adding a thermal expansion node to the model based on the work presented in [31]. The cooling down process, the test-structure was set to be initially stress-free at bonding temperature of 170 °C, and the final temperature was set to room temperature of 20 °C. Additionally, to account for copper plastic behavior, initial yield stress of 250 MPa and isotropic tangent modulus of 2 GPa was assigned to the material, and the plastic material domain was applied to the copper layers. [31,32] Fig. 1(c) illustrates the boundary conditions applied to the model.

3. Results

3.1. Preliminary observation of irregular Sn—In penetration

After the bonding process, optical microscope inspection on the interconnects was carried out on Si-Borofloat®33 wafer-pair as illustrated in Fig. 2(a). The squeeze-out at the seal ring edges indicates that the Sn—In had melted during the bonding process. Intriguingly, the as-bonded samples show areas with darker shade, which represent a possible undercut or irregular penetration of squeeze-out between the copper and substrate. Observations on the same samples after the heat treatments showed that the shaded areas grow towards the center of the sealing ring, as marked with red arrows at Fig. 2(c). Additionally, these irregularities were also observed after annealing below the Sn—In eutectic point (~112 °C), pointing out towards solid-state diffusion mechanism. While above the melting point, voids could be observed in the squeeze-out region, that indicate liquid penetration or diffusion

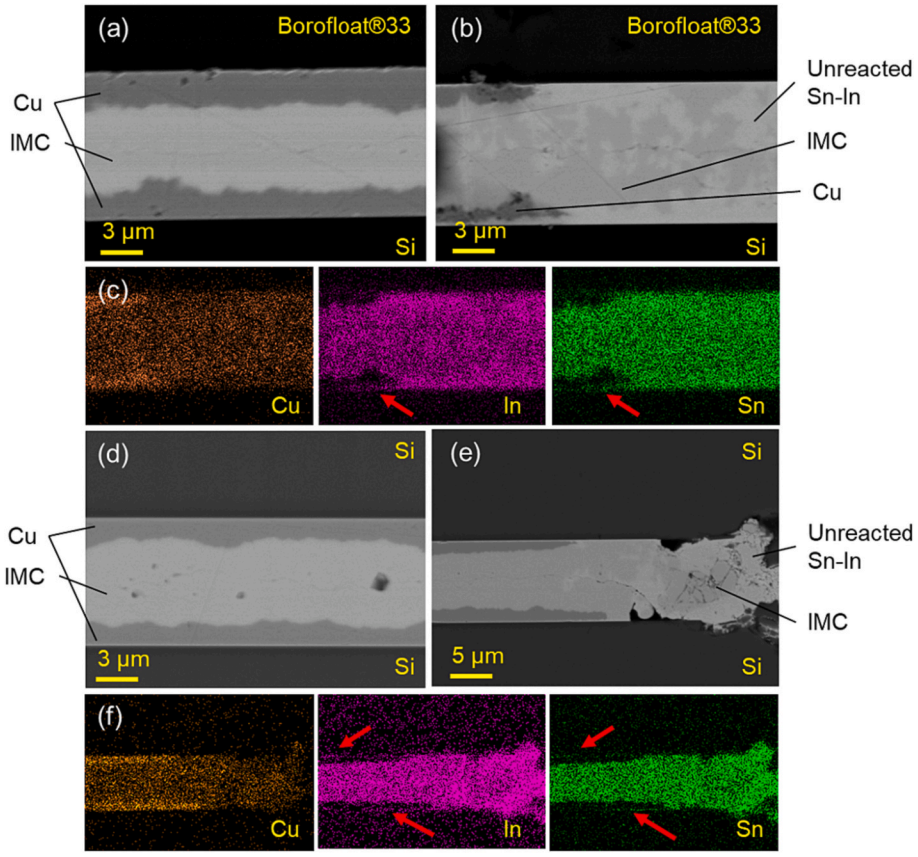

Fig. 3. Cross-section SEM images of (a) the bond center area, (b) squeeze-out area, and (c) Cu, In and Sn EDS elemental maps of the squeeze-out area of bonded Si-Borofloat®33 and (d,e,f) bonded Si—Si, respectively. Red arrows marked where Sn—In starts to penetrate under the copper layer. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

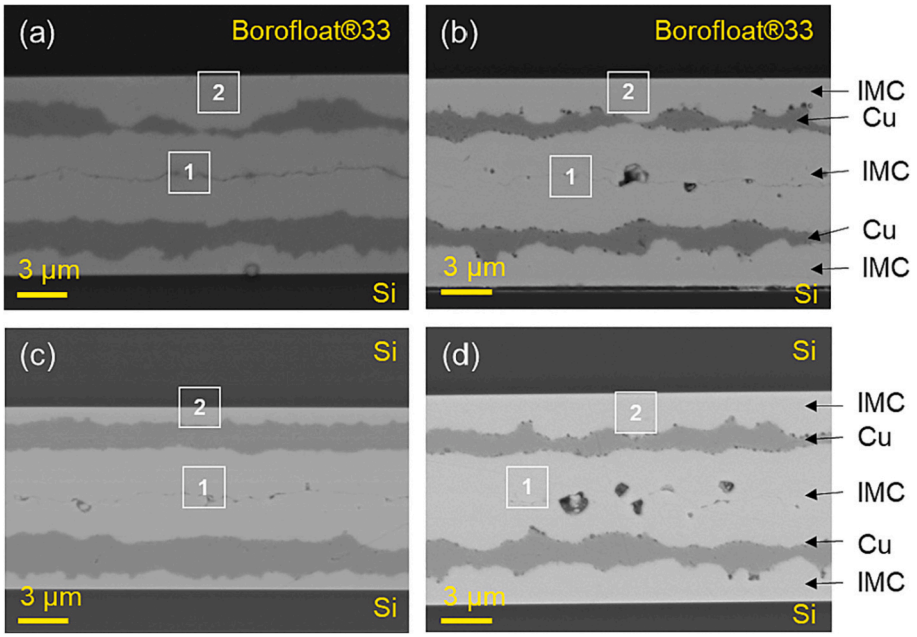

Fig. 4. SEM Cross-sections of the bond center area of (a,b) bonded Si-Borofloat®33 and (c,d) bonded Si—Si, after high-temperature storage at 150 °C for 6 h and 168 h, respectively.

occurs at copper-substrate interface.

Figure 3 shows micrographs of the seal-ring cross-section for bonded Si-Borofloat®33 and Si—Si. The bonds center area showed a structure of intermetallic layer sandwiched between unreacted copper layers. EDS semi-quantitative analyses show the intermetallic has an average composition of 55.5 ± 1.2 at.% Cu, 22.9 ± 1.8 at.% In, and 21.66 ±

Table 1
Elemental composition by EDS characterization on the area marked at Fig. 4.

Elemental composition (at. %)				
Sample	Area	Cu	In	Sn
Si- Borofloat®33	a.1	58.79 ± 0.28	21.33 ± 0.77	19.88 ± 0.81
	a.2	60.12 ± 0.02	27.93 ± 0.13	12.26 ± 0.46
	b.1	57.92 ± 0.19	24 ± 0.12	18.08 ± 0.07
	b.2	58.95 ± 0.56	28.29 ± 0.16	12.77 ± 0.4
Si-Si	c.1	57.28 ± 0.61	21.43 ± 0.77	21.29 ± 0.17
	c.2	58.76 ± 0.06	27.46 ± 0.26	13.79 ± 0.32
	d.1	57.81 ± 0	20.43 ± 0.5	21.76 ± 0.5
	d.2	61.26 ± 0.58	22.77 ± 4.08	15.97 ± 3.5

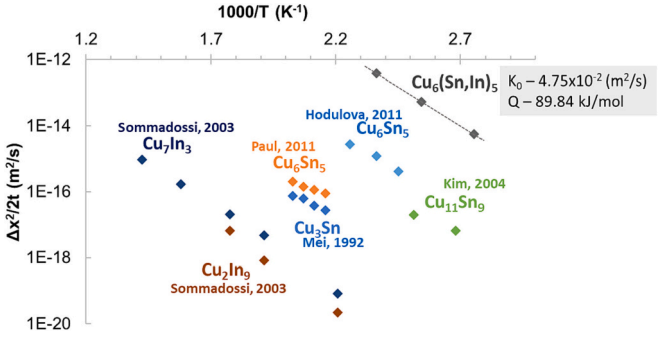

Fig. 5. Comparison of growth rate constant of various intermetallics ([33–36,38]) as a function of temperature.

0.77 at.% Sn, which can be attributed to the $Cu_6(Sn,In)_5$ phase. Meanwhile, micrographs of the squeeze-out region showed in Fig. 3(b) exhibited areas with brighter contrast than the intermetallic, representing unreacted Sn—In, which were confirmed with the EDS elemental maps presented in Fig. 3(c) and (f). The Sn—In maps also show that the intermetallic has started to form between copper-substrate interface at locations marked by red arrows. This reveals a possibility that Cu starts to delaminate, creating a pathway for Sn—In diffusion or penetration. Intriguingly, the results also do not show significant differences between bonded Si—Si and Si-Borofloat®33 samples. This indicates that the global CTE mismatch between the bonded wafers was not the roots cause of the observed issue.

Figure 4 summarizes the cross-section micrographs of the samples that were kept at high-temperature storage for 6 h and 168 h, and Table 1 summarizes the EDS characterization of the areas marked in the figures. The results show that the bonds consisted of a single phase $Cu_6(Sn,In)_5$, with a slightly higher copper content than the as-bonded samples that could lead into nucleation of $Cu_3(Sn,In)$ after a longer annealing time. This observation agrees with the previous studies that In has stabilizing effect of the Cu_6Sn_5 phase [22,23]. But, more importantly, all the figures also show that new intermetallic layers had formed between the electrodeposited copper and silicon. These features seem to grow towards the copper layers, implying the formation initiated from the interface, which conform with the optical microscopy observations that Sn—In alloy had penetrated the interface between the bond and the substrate. A higher In content than Sn was present in the newly formed intermetallic layer, that presumably caused by excess Indium thickness from the electroplating process.

3.2. Diffusion kinetics and driving force analysis

Diffusion kinetics analysis was utilized to examine the possibilities that caused Sn—In penetration. Based on the cross-sectional and topside observations, no further intermetallic growth was observed between samples that were stored at 150 °C for 6 and 168 h. Hence, the Cu-Sn-In intermetallic growth rate constant, can be deduced by using the parabolic equation and the effect of temperature can be evaluated through Arrhenius equation. [33] The intermetallic length after heat treatment process was obtained by post-processing of the optical microscopy image discussed on section 3.1, and the results were summarized in supplementary Table 2. Fig. 5 shows a summary of the growth rate constant of Cu—Sn and Cu—In based intermetallic from various references, superimposed with data obtained from this study. Understanding the intermetallic growth rate constant is directly proportional to diffusion rate implies an extremely rapid diffusion process occurred.

Below the eutectic point of Sn—In alloy the growth rate constant was estimated to be 5.6×10^{-15} m^2/s. However, above the eutectic point the diffusion mechanism increases significantly by several orders of magnitude reaching 3.8×10^{-13} m^2/s at 150 °C. These values are few order of magnitudes higher than the reported kinetics for Cu—Sn (Cu_6Sn_5) [34,35] and Cu—In (Cu_7In_3) [36–38] intermetallic. Unfortunately, there is limited information available on Cu-Sn-In kinetics [39], especially regarding the diffusion kinetics at low temperatures. Nevertheless, these studies point out mass transport along grain boundary and changes in the driving force are the factors that could affect the diffusion processes. [40]

Based on the test structure, grain boundary diffusion of Sn—In could only occur in two ways. The first one would be grain boundary diffusion through the bulk electrodeposited copper. However, this would also mean that intermetallic formation should also occur at the bulk copper grain boundaries, which had not been observed in the cross-sections. Furthermore, grain boundary diffusion typically occurs slower than what was estimated by several orders of magnitude (10^{-17}–10^{-18} m^2/s), owing to the large size of Sn—In atom to the Cu. [37,41] A more likely possibility is mass transport through the polycrystalline copper seed layer.

The driving force for Cu—Sn or Cu—In interdiffusion are represented by their chemical potential differences. [42,43] A thermodynamic study on the Cu-Sn-In ternary system shows that the addition of Indium stabilizes the phase in $Cu_6(Sn,In)_5$, hence reduces the driving force for copper diffusion. [22,23] This also confirms that Sn—In diffusion is a dominating factor for the irregular intermetallic formation. Additionally, the study also shows Gibbs energy of formation of $Cu_6(Sn,In)_5$ increased by ~50%. [22] However, this increase could not justify the increase of diffusion rate by several orders of magnitude, which implies there is another factor that increases Sn—In mobility.

Alternatively, irregular Sn—In penetration may arise due to issues that lie within the Cu-substrate interface. The optical microscope observations presented in section 3.1 reveals instances where Sn—In squeeze-out remelted and penetrates through the Sn—In interface, particularly on samples heat-treated above the eutectic point. This strongly suggests that delamination had occurred, thereby providing pathway for the melt to penetrate. Thus, investigating factors that could affect interface adhesion, such as impurities and defects become critical. [14,17]

Lastly, residual stresses are a known factor that affect the reliability of interconnect, particularly at interfaces where CTE mismatch are the largest. [32,44] Buckling or cracking due to thin-films deposition may result with delamination of the interface. [45] Additionally, accumulation of the thermomechanical stresses from different processing stages may surpass the individual strength of the materials involved, which result in structural failure as well. [20] It is worth noting that such structural failures potentially serve as a pathway for Sn—In penetration.

To summarize, the potential factors that causes Sn—In irregular penetration can be listed as: (1) extremely high grain boundary diffusion of Sn—In through polycrystalline Cu seed layer, Interface delamination due to (2) defects or (3) impurities, and lastly (4) residual stresses. The next few sections are dedicated to present and discuss the results series of characterization methods to study the root cause of irregular Sn—In penetration.

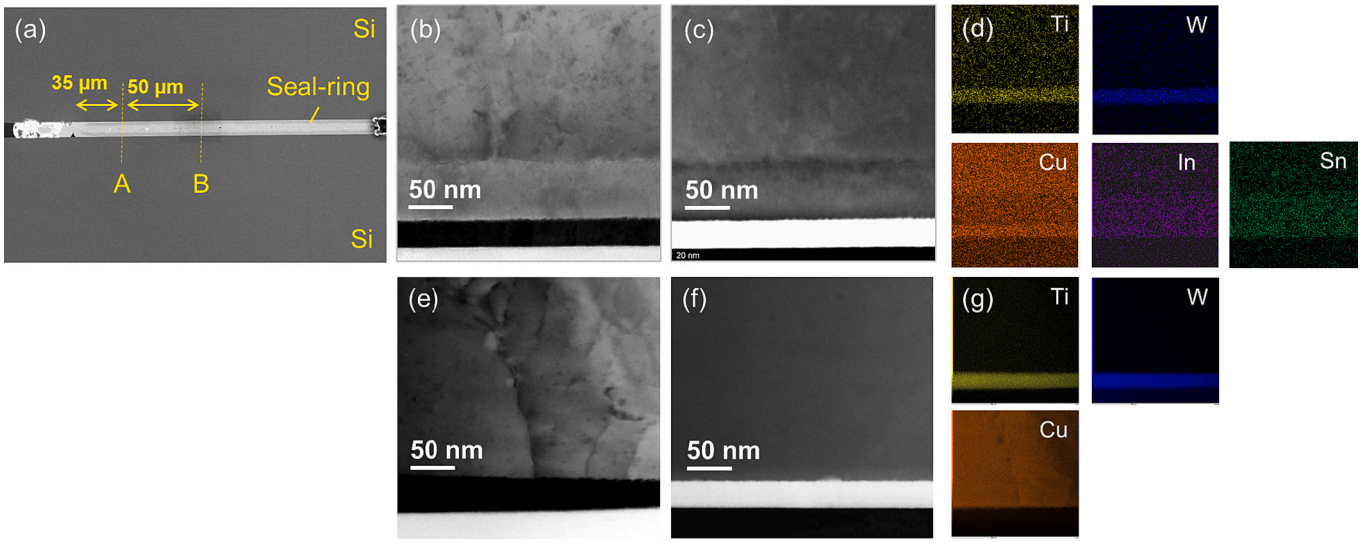

Fig. 6. (a) SEM image of seal ring cross section for as bonded Si—Si, A and B are the areas used for TEM observation; Respectively, brightfield STEM, darkfield STEM, and EDS mapping for region (b,c,d) A and (e,f,g) B.

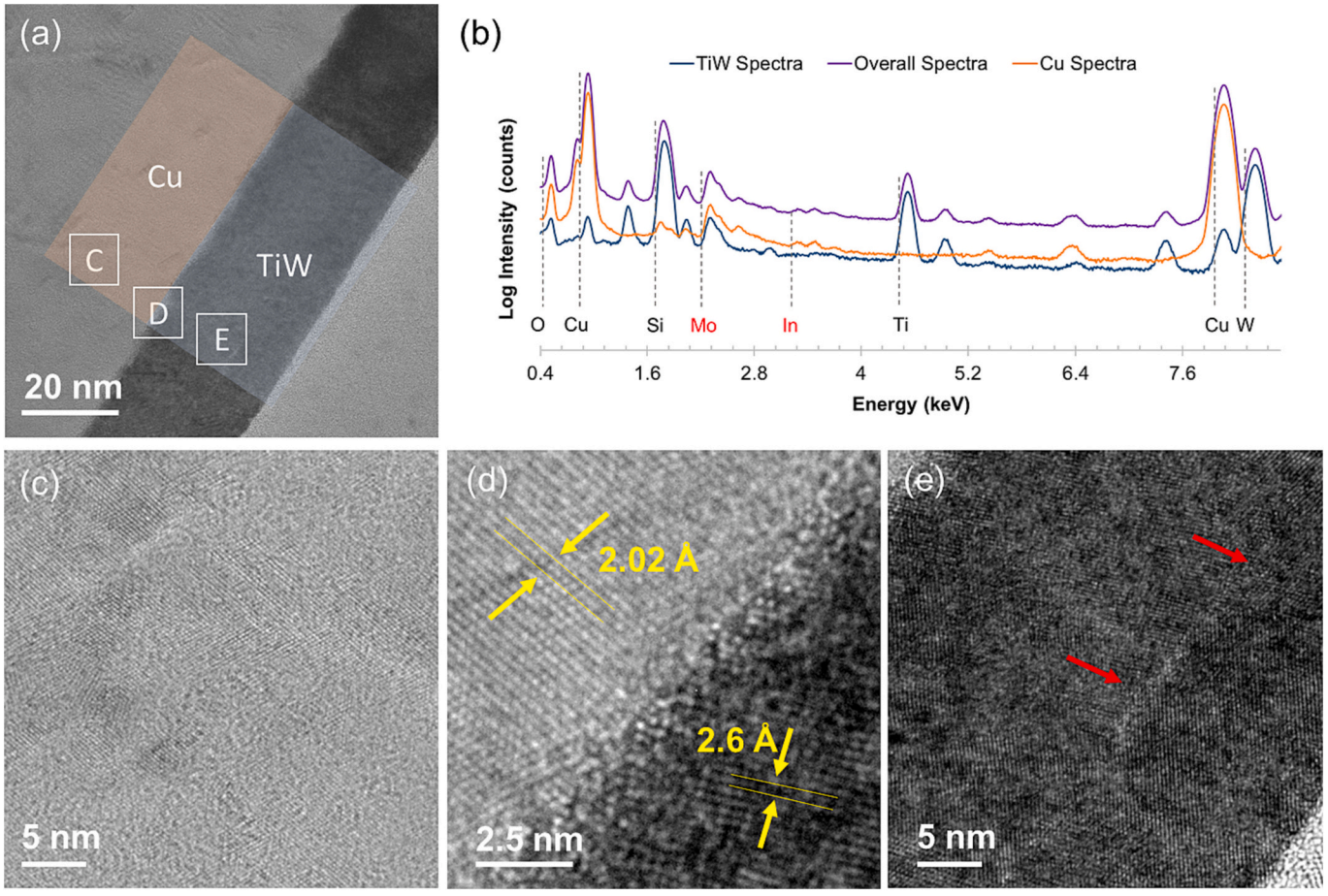

Fig. 7. HRTEM image of as bonded Si—Si at (a) 500 k magnification, (b) EDS line spectra of the marked area; 800 k magnification image of the area marked in (a): (c) Cu layer, (d) TiW-Cu interface, and (e) TiW layer (red arrow mark indicate possible impurities). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

3.3. High-resolution interface imaging

Grain boundary diffusion or defects that promote Sn—In penetration were examined using high resolution imaging with TEM on the copper-substrate interface. Fig. 6(a) shows a micrograph of the as-bonded Si—Si interconnects, from which two lamellas were fabricated for the interface investigation. The first lamella was fabricated 35 µm from the edge, namely location A, where Sn—In penetration is expected to be minimal.

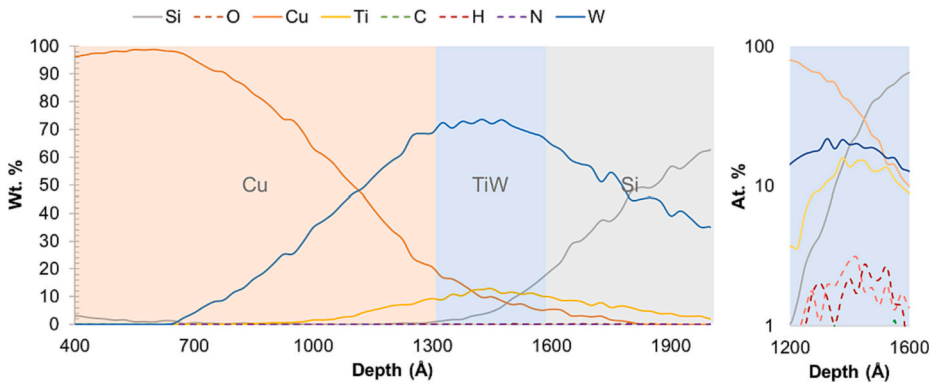

Fig. 8. Elemental and impurity concentration of unpatterned TiW-Cu adhesion and seed layers obtained by ERDA. Inset on right shows atomic percentage in the TiW area.

The second lamella were fabricated 85 μm from the edge, marked as location B, where no Sn—In penetration was observed.

Figure 6 (b) and (c) show a STEM image of the interfaces at location A. The micrographs show that Sn—In had penetrated between the TiW adhesion layer and copper. This highlighted weak adhesion energy between TiW-Cu or presence of impurities as a possible cause for Sn—In penetration. EDS elemental maps at Fig. 6 (d) indicate Sn—In had reacted with copper to form intermetallic. However, phase identification from semi-quantitative analysis was limited due to interferences from Cu-based TEM grid. This effect was more evident on the TiW layer where electrons are more likely to scatter due to heavy element presence (in this case W). Furthermore, no copper and titanium, diffusion towards silicon were observed, confirming excellent barrier properties of TiW.

STEM observation of the Si—Cu interface close to the center of the interconnect, namely location B, were presented at Fig. 6 (e), (f), and (g). STEM images confirm that no Sn—In penetration had occurred at this location. The observed copper microstructure from brightfield micrograph implies that copper seed layer had been incorporated to the electrodeposited copper throughout the bonding process. Consequently, this fact eliminates the possibility of grain boundary diffusion occurring through the copper seed layer.

Possible cause of defects and impurities at the TiW-Cu interface were inspected by HRTEM imaging and interface EDS analysis of location B. Fig. 7 (a) shows a general overview of the interface and the highlighted areas represent locations used for EDS characterization. In Fig. 7 (b) individual EDS spectra obtained from the TiW and Cu layers are illustrated, along with an overall spectrum that represents summation of both. The copper layers spectrum shows slight Sn—In content, which is contrary to the findings presented at Fig. 6. So, it is most likely the peak is a result of measurement artifact. On the other hand, spectrum of the TiW layers shows additional peaks that suggest impurities or measurement artifacts due to electron scattering.

Higher magnification micrographs presented in Fig. 7 (d) reaffirms the copper seed layer had been incorporated to the electrodeposited copper. Furthermore, no unwanted interfacial layer was observed between the TiW-Cu interface micrograph, suggesting a good metallic bond locally. More importantly, micrographs of the TiW layer in Fig. 7, shows area with brighter contrast (marked with the red arrows). This further implies the presence of impurities within the TiW layer, which most likely originate from the two-step deposition process, potentially compromising its adhesion to the copper layer.

3.4. TiW-Cu interface impurities

ToF-ERDA measurements on unprocessed TiW-Cu adhesion and seed layers were conducted to investigate the elemental and impurity concentration of the layer stack. Fig. 8 shows the depth profiles of [Si], [O], [Cu], [Ti], [C], [H], [N] and [W] in the adhesion and seed layers obtained from ERDA measurements. Based on the result, the thickness of the TiW can be estimated as 30 nm, which agrees with the observed thickness in TEM image at Fig. 7. The impurity content on TiW adhesion layer derived from the measurements is presented in supplementary

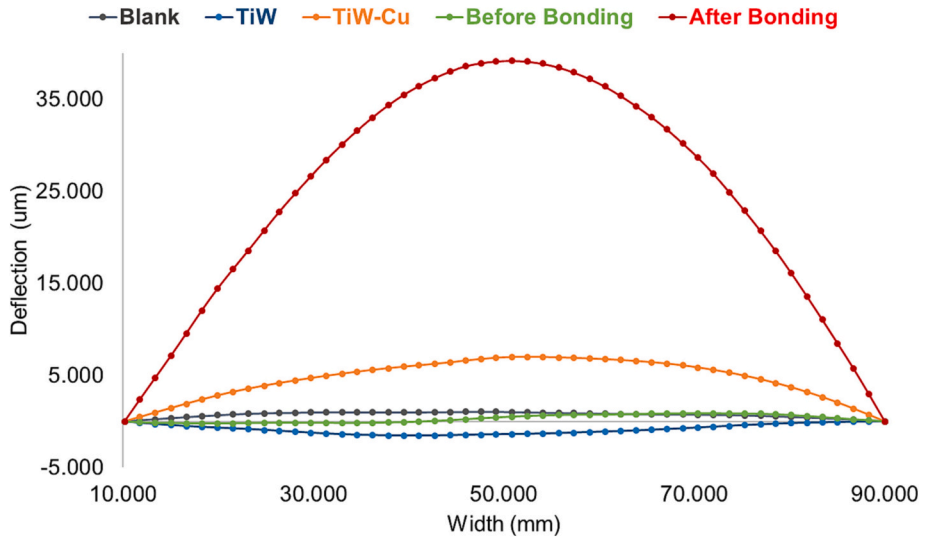

Fig. 9. Wafer deflection measurements of bonded Si—Si at different stage of processing.

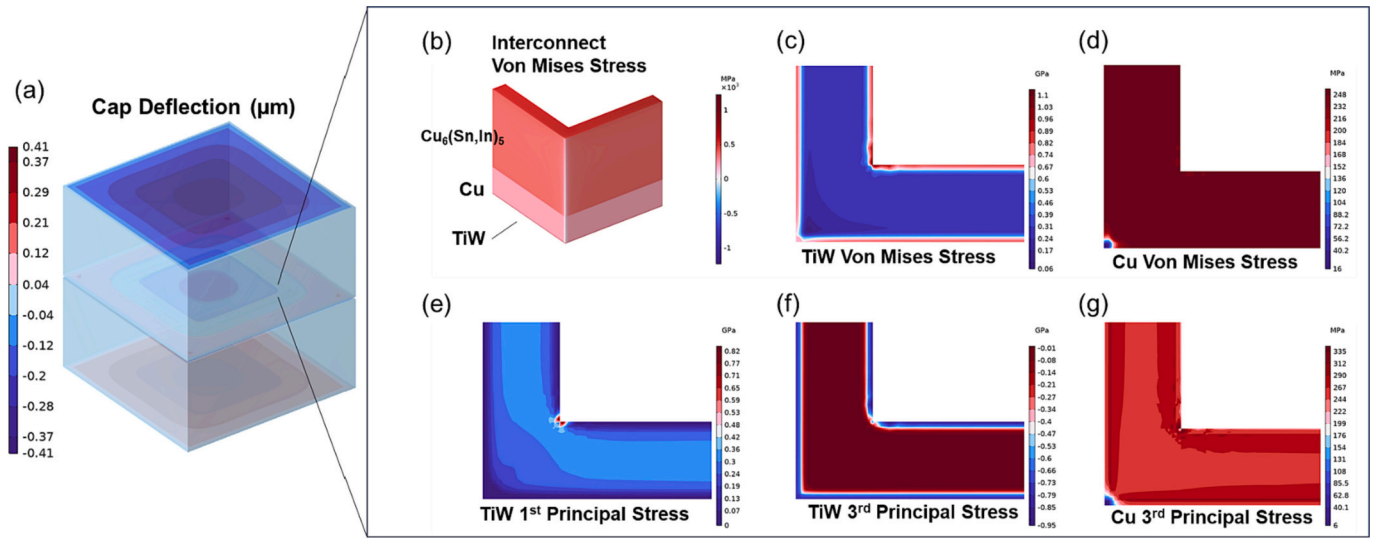

Fig. 10. Finite element modelling results on bonded Si—Si showing (a) Cap deflection, (b) Von Mises Stress of TiW-Cu-Cu_6Sn_5 layer stack; Von Mises Stress of (c) TiW layer, and (d) Cu layer; 1st principal stress and (f) 3rd principal stress of TiW layer; (g) 3rd principal stress of Cu layer.

Table 3. Altogether with the inset presented in Fig. 8, the measurement showed that oxygen had accumulated within the TiW layer. This means that during the deposition process, Ti acts as a getter in the deposition chamber leading to oxygen incorporation into the deposited layer. [46] Furthermore, the result also indicate formation of TiO_2 that could promote barrier like properties but lowers adhesion energy between TiW and Cu. [14,17]

3.5. Residual stress analysis

Delamination of TiW-Cu interface is another possibility that could promote the irregular Sn—In penetration. The defects are typically caused by residual stresses due to CTE mismatch. Global residual stress resulting from thin film deposition could be studied by measuring the curvature as shown in Fig. 9. Then, residual stress as a result of thin film deposition could be estimated from the measured deflection using Stoney's Eq. [47]:

$$\sigma_f = \frac{h^2}{6t_f\left(S_{11}^{Si} + S_{12}^{Si}\right)R} \tag{1}$$

Where h is the substrate thickness, t_f is the thin film thickness R is the radius of curvature, and $1/(S_{11} + S_{12})$ is silicon compliance tensor of 1.803×10^{11} N/m^2. For the known TiW adhesion layer thickness of 30 nm, residual stress could be estimated to be -242.83 ± 28.01 MPa, which indicates compressive stress. On the other hand, after subsequent deposition of TiW and Cu, the stresses could be estimated to be 273.70 $\pm$ 74.91 MPa, which indicate that Cu deposition induces a high tensile stress. After the metal bonding layer deposition and removal of unpatterned seed layer, the curvature returned close to its initial state, implying the global stress was minimal. However, after the bonding process the curvature rose significantly, indicating very high residual stress formed during the bonding process. It is imperative to note, the curvature might not represent the global stresses since there are no CTE mismatch between the bonded silicon substrates. Instead, the curvature is most likely caused by the accumulation of local residual stresses. [48] Unfortunately, the residual stress from before and after the bonding process could not be quantitatively determined since the film thickness information is no longer applicable.

Finite element modelling results to estimate the local residual stresses acting on the interface were summarized in Fig. 10. The model simulates the stress at the interface of the as-bonded sample. As a result of forming hermetic encapsulation, the pressure difference between cap and formed cavity, 410 nm inward deflections were observed both in bottom and cap wafers. It is critical to note that singularity effect limits quantitative determination of stresses at sharp corner of the geometries. [31] Nevertheless, qualitative assessment of the stress distribution is true. The modelling results show the Von Mises stresses across the TiW, Cu, and $Cu_6(Sn,In)_5$ could be estimated as 397 MPa, 250 MPa, and 600 MPa, respectively.

Based on the values, it is understandable that the copper layer undergoes plastic deformation, while TiW, $Cu_6(Sn,In)_5$ layers, and Si substrate still behave elastically. Consequently, during the heat treatment process the copper layer could not revert into its initial state, resulting in defects to pile-up. [49,50] Alfreider et al. studied defect formation in TiW-Cu interface using a specialized test structure, which demonstrated that tensile stress resulted in ductile failure at the copper layer. Furthermore, shear stresses introduced crack initiation at the TiW-Cu interface. [11,21,51] Another study also discussed that copper plastic deformation started from the TiW-Cu interface, due to the high CTE mismatch, during heating and cooling down process. [32] These studies explain the likelihood of failure occurring in the interface, enabling pathway for Sn—In penetration.

Another potential reason for the delamination can be revealed by analyzing the principal stresses. Fig. 10 (e), (f), and (g) illustrates the principal stresses acting on TiW and Cu layers. The first principal stress denotes tensile stress, while the third principal stress represents compression stress. It is noteworthy that, although most layers undergo tensile loading, the TiW layer's edge experiences high compression stress. This strongly implies the opposing loading condition as a cause for TiW-Cu delamination, particularly at the edges. This finding also aligns with the previous observations presented in Fig. 3, where delamination identified at the interconnect edge.

4. Discussion

To summarize, SLID bond on Cu-Sn-In metallurgy was employed to bond Si—Si wafers, as well as Si-Borofloat®33 wafers. Observation on both wafer pairs, shows irregular presence of Sn—In between copper and substrate after the bonding process. After high-temperature storage at 150 °C up to 168 h, additional Cu-Sn-In intermetallic layer was observed between copper and substrate. This indicates that penetration of Sn—In has occurred at the interface between the copper and the substrate. Diffusion kinetics study estimates the intermetallic growth rate constant reaches $\sim 4 \times 10^{-13}$ m^2/s, which is several orders of

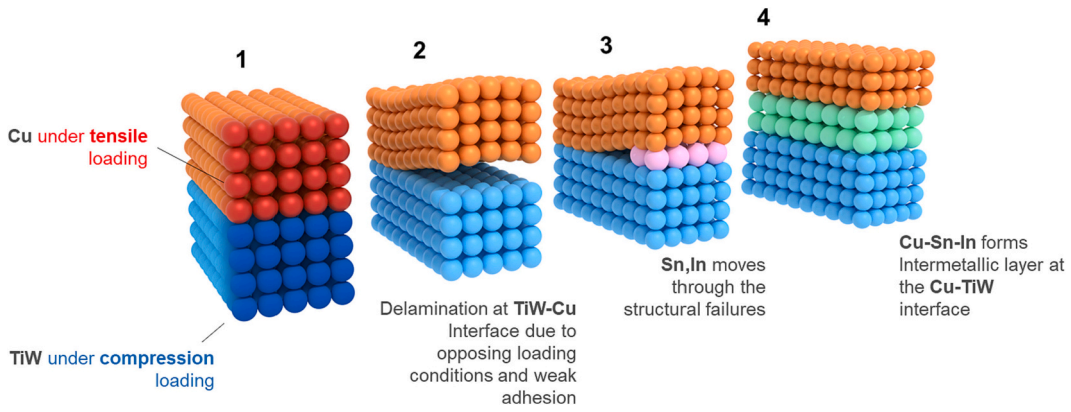

Fig. 11. Illustration for defect formation that promotes In—Sn diffusion: (1) Opposing residual stress due to CTE mismatch, (2) Cu layer delaminates from TiW due to the stress conditions and weak adhesion, (3) the structural failures creating pathway for In and Sn atoms, and (4) Cu-Sn-In intermetallic are formed at the TiW-Cu interface.

magnitudes higher than that in the Cu—Sn and Cu—In based systems. Furthermore, the driving force for Cu-Sn-In intermetallic formation could not justify the extremely high growth rate constant. Thus, a series of investigations have been carried out to investigate the root cause for Sn—In penetration between copper and the substrate.

High resolution TEM characterization excluded the possibility of grain boundary diffusion or TiW undercut. The result also highlights impurities that might cause poor adhesion between the TiW layer and electrodeposited copper. The ERDA measurements then confirmed the impurities, particularly oxygen, existed in the TiW layer. This reaffirms that the adhesion between TiW and Cu is compromised.

Residual stress analyses using finite element modelling showed that the copper layer has undergone plastic deformation during the bonding process, which compromises its structural integrity. Additionally, opposing loading conditions were observed at the interconnect edges. Combined with the results from other characterization methods, it is more likely that copper delaminated from the TiW adhesion layer. Fig. 11 illustrates the proposed failure mechanism that leads to the formation of pathway for Sn—In atoms.

Based on the results, several methods to prevent such failure mechanism can be proposed. First, to address the weak adhesion between TiW and copper, the deposition processes need to be optimized. Several studies have proposed improving adhesion by adjusting the TiW layer thickness and increasing Ti concentration. [14,52] Furthermore, impurities could be prevented by using single-step deposition process or running an oxygen gettering process prior to TiW deposition. Second, Sn—In squeeze-out was identified as the source for irregular Sn—In penetration from the interconnect edge. Consequently, minimizing squeeze-out is an obvious approach, that could be achieved by: (1) optimizing the bonding conditions (pressure and temperature), (2) reducing low-melting metal stack thickness, and (3) modifying the interconnect geometry. [53,54] The last proposal is to minimize the residual stresses caused by the CTE mismatch. The curvature measurements showed that curvature still occurs between bonded Si—Si wafers, that does not have a global CTE mismatch between the bonded substrates. Consequently, the defining factor for the interface problem could be attributed to the local CTE mismatch, particularly at the interface between TiW and Cu. One possible solution to this issue is by introducing another layer of materials with similar thermomechanical properties, for instance TiW-Cr-Cu. Alternatively, a rather simpler solution for residual stresses would be to reduce the bonding temperature even further. Given the eutectic point for Sn—In alloy at 110 °C, the bonding process could be done at even lower temperatures. [22,23]

5. Conclusion

In this work, the failure mechanism at the interface of low-temperature bonded interconnects were investigated. Si—Si and Si-Borofloat®33 wafer pairs were bonded using SLID bond based on Cu-Sn-In metallurgy at temperatures as low as 170 °C to form the test structure. Initial observation of the as-bonded samples displayed the interconnect formed of a single phase $Cu_6(Sn{\cdot}In)_5$. However, penetration at copper-to-substrate interface from squeeze-out region were also observed. This resulted in the formation of unwanted Cu-Sn-In intermetallic layer between the copper and the substrate after kept at high-temperature storage up to 168 h.

A series of characterization were carried out using TEM, ERDA, and residual stresses simulation to find the root cause. The results concluded interplay between weak adhesion caused by impurities and residual stresses delaminates Cu from TiW adhesion layer. Furthermore, the issue resulted in a pathway for remelting Sn,In to move in from squeeze-out region. The findings emphasized that local residual stress, where CTE mismatch is largest, possess a critical risk, even at lower processing temperature.

To mitigate the issues found in this study, heterogenous integration process based on TiW-Cu architecture are proposed by paying important aspect to: improving adhesion of TiW-Cu layers, mitigate of squeeze-out formation, and reduce residual stress by utilizing lower bonding temperature.

CRediT authorship contribution statement

Obert Golim: Writing – review & editing, Writing – original draft, Visualization, Investigation, Formal analysis, Conceptualization. **Vesa Vuorinen:** Writing – review & editing, Validation, Formal analysis, Conceptualization. **Glenn Ross:** Writing – review & editing, Investigation, Formal analysis. **Sami Suihkonen:** Writing – review & editing, Investigation, Formal analysis. **Mervi Paulasto-Kröckel:** Writing – review & editing, Validation, Supervision, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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Appendix A. Supplementary data

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