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Bergman, Jan H.S.; Ryynänen, Kaisa; Ala-Laurinaho, Juha; Stadius, Kari; Ryynänen, Jussi; Viikari, Ville Crack Stop as a Coupling Element Between an IC Chip and Antenna

Published in: 18th European Conference on Antennas and Propagation, EuCAP 2024

DOI: 10.23919/EuCAP60739.2024.10501186

Published: 01/01/2024

Document Version Publisher's PDF, also known as Version of record

Please cite the original version:

Bergman, J. H. S., Ryynänen, K., Ala-Laurinaho, J., Stadius, K., Ryynänen, J., & Viikari, V. (2024). Crack Stop as a Coupling Element Between an IC Chip and Antenna. In *18th European Conference on Antennas and Propagation, EuCAP 2024* IEEE. https://doi.org/10.23919/EuCAP60739.2024.10501186

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Crack Stop as a Coupling Element Between an IC Chip and Antenna

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Abstract—Millimeter-wave antenna arrays place integrated transceiver chips and antennas in close proximity to each other. As a result, the presence of the chip will affect the performance of the system significantly, with the metallic structures within the chip being a source for structural resonances. A transition which utilizes one of these metallic structures, the crack stop, as a coupling element is presented. The proposed design allows a non-galvanic connection between the IC chip and the antenna. The performance of the transition is analyzed through simulations, and is shown to reach above-70-percent power transmission between 42.3 GHz and 62 GHz, covering the majority of V-band.

Index Terms—antenna arrays, integrated circuits, simulations, millimeter wave devices, aperture coupled antennas

I. INTRODUCTION

The increase in the operating frequency of wireless devices brings new challenges to the design of each component in the system. For example, the higher level of integration in antenna arrays at millimeter-wave frequencies has led to integratedcircuit (IC) components being closer to the antenna elements. This will become more pronounced with the upcoming sixth generation (6G) of mobile communications, which places high importance on antenna arrays in both mobile terminals and base stations [1].

A typical antenna array can require separate vector modulators for every antenna element in the array. In the worst case, using single-channel chips such as [2], an antenna array can include as many or more IC chips as antenna elements. Moreover, while the elements in an antenna array typically scale linearly with frequency, the IC chips do not necessarily follow a similar trend [3]. This can lead to a situation, where a significant number of electrically large ICs are in the immediate vicinity of antennas, which has been observed to have significant effects on the performance of the system [4].

Thus far, antenna designers have not required any extensive knowledge about what an IC chip consists of. The main effects the chip causes for the system have been included by modeling the chip as a dielectric slab with the same dimensions as the chip [5]. However, as the chips are becoming electrically larger, the effects of the metallic structures within the chip, such as transmission lines, capacitors, and crack stops, can no longer be neglected.

Some studies have been made on the importance of modeling an IC chip correctly and on the negative effects it might



Fig. 1. Illustrative view of the (a) top and (b) side of an IC-chip simulation model. $h_{\rm b}=30\,\mu{\rm m}$ refers to the height of the flip-chip bumps. The silicon die, flip-chip bumps, and crack stop are drawn in dark gray, yellow, and light gray, respectively. Units in $\mu{\rm m}$.

have on the system [4], [6]. In this work, we approach the problem of having metallic structures near an antenna–IC transition with the following question: Could we utilize them for our benefit? Specifically, we look into the possibility of using a metallic crack stop as a part of an antenna–IC transition at the V-band. The crack stop is a metallic structure on the edge of the chip that makes the chip more robust against cracks, which might damage the chip.

Section II introduces the simulation model of an IC chip, the crack-stop coupling structure, and the antenna-transition printed circuit board (PCB) together with a proposed nongalvanic antenna–IC transition. In Section III, the performance of the proposed transition and its sensitivity to structural uncertainties is showcased through simulations in CST Studio Suite [7].

II. SIMULATIONS

A. Initial IC-chip model

For the purposes of this work, a simplified model of a baredie IC chip will be used. Fig. 1 shows a visualization of the 4-mm-by-2.6-mm-by-0.25-mm chip used in the simulations, including a silicon die with a crack stop and copper flipchip bumps, the last of which being the galvanic interconnects between the IC chip and a PCB.

Integrated circuits are fabricated into a wafer that may include hundreds or even thousands of individual circuits, often called dies. Scribe line is an area in a wafer that defines the cutting region that is used during wafer dicing to separate individual dies at the end of the manufacturing process. The cutting process itself may damage the edges of a die [8]. These defects result in a lower yield or issues in reliability, such as penetration of moisture into the IC stack [9], [10]. Crack stops are added to dies to avoid crack propagation towards the active chip area after the dicing process. Crack stop contains several metal layers and in some processes, it forms a continuous metallic rim, also called a seal ring, around the chip as is shown in Fig. 1(a). This type of continuous crack stop will be used in this work.

In practice, the metallic rim is manufactured during the back-end-of-line (BEOL) portion of the IC-fabrication process on the metallic layers of the BEOL stack [11]. This gives the order of magnitude for the size of the metallic rim crack stop, which is manufactured only on a thin section on the top of the chip as is shown in Fig. 1(b). For this work, a 15- μ m-by-15- μ m square-profile rim is selected.

The presence of such a crack stop is equal to having an electrically conductive loop in the vicinity of radio frequency (RF) transmission lines. Therefore, the RF signal might couple to the crack stop and start to resonate at frequencies, at which the electrical length of the loop is appropriate.

B. Adding electrical discontinuities to the crack stop

To alleviate the problematic resonances caused by the crack stop, electrical discontinuities can be introduced in the rim. This means that the crack stop will no longer be continuous but will consist of multiple shorter sections. Methods for creating electrical discontinuities without undermining the structural integrity of the crack stop have been published [12].

Using gaps in the crack stop to mitigate structural resonances has already been done in the past [13], [14]. However, an excitation is placed in one of the gaps, a part of the crack stop can be used as a component in the transition from the IC to the PCB. Furthermore, this component of the transition can realize a non-galvanic connection between the IC chip and the PCB by utilizing aperture coupling. This could, for example, enable coupling to the bottom of the chip, i.e., the opposite side from the contact pads, through the chip substrate. However, in this work we will focus on a same-side transition as a proof of concept.

In Fig. 2, a chip with the proposed crack-stop coupling structure is shown. The gaps have three purposes: excitation, separating the coupling structure from the rest of the crack stop, and reducing structural resonances. The coupling structure resembles a dipole, consisting of two metallic strips extending in opposite directions from a central gap, and its key dimensions are shown in Fig. 2(b). In the simulations, a 100- Ω discrete-port excitation is placed in the gap between



Fig. 2. (a) Illustration of the chip with a discontinuous crack stop. Gaps used for reducing structural resonances, separating the coupling structure, and placing the excitation are highlighted with blue, orange, and red arrows, respectively. (b) Closeup of the area marked with green, showing the key dimensions of the coupling structure and the location of Port 1. Note that the pictures are not to scale. Units in μ m.

the two metallic strips and is later referred to as Port 1. In practice, this excitation could be done through galvanic or non-galvanic connections from the on-chip transmission lines to the crack stop. However, the detailed IC design required for this transition is beyond the scope of this work.

C. The antenna-transition PCB

The PCB consists of a 200- μ m thick two-sided Panasonic MEGTRON 7 substrate with material parameters $\epsilon_r = 3.31$ and $\tan \delta = 0.003$. The chip is attached on one side of the PCB using the flip-chip bumps, such that all the bumps are connected to the ground plane, as is shown in Fig. 3(a).

The crack-stop coupling structure on the chip is placed across two slots in the ground plane on the IC-chip-facing side of the PCB. The distance from the coupling structure to the PCB is equal to the height of the flip-chip bumps, $h_b = 30 \,\mu\text{m}$. On the opposite side of the PCB, one microstrip line (MS) runs symmetrically across the centers of the slots and is terminated at both ends in waveguide ports, as is shown in Fig. 3(b). These ports are handled as the two terminals of a differential port, effectively forming Port 2. A via from the MS to the ground plane is added in between the two slots in order to isolate the positive and negative terminals of Port 2.

Terminating both ends of the transition in ports is done for a more efficient analysis of the transition. However, the MS on the back side of the PCB could be replaced with, or connected to a differentially-fed antenna.



Fig. 3. (a) Overview of the transition structure showing the placement of the chip on the top side of the PCB and the location of Port 1 on the chip. (b) Back-side of the PCB with the microstrip line, the terminals of Port 2, and outlines of the chip and the coupling slots. Units in μ m.

III. RESULTS

The performance of the transition is analyzed through simulations in CST Studio Suite [7]. Both ends of the structure are terminated into $100-\Omega$ differential ports, with Port 1 being on the chip and Port 2 on the PCB.

Fig. 4 shows the S-parameters of this two-port system. The transmission parameter $S_{21} = S_{12}$ reaches a peak value of -0.91 dB at 49 GHz, and a band of above-70-% power transmission, corresponding to $S_{21} = S_{12} \ge -1.5 \text{ dB}$, with a nearly 20-GHz bandwidth between 42.3 and 62.0 GHz. The rest of the power is either radiated (up to 20%), dissipated (up to 6%), or reflected.

The height of the flip-chip bumps might not be exactly known during the IC-design process. The bump height defines the distance between the PCB and the IC chip and is therefore an important parameter for the non-galvanic connection between the two. Therefore, Fig. 5 displays the effect that varying the height of the flip-chip bumps $h_{\rm b}$ has on the performance of the transition.

The most significant effect of varying the bump height is the decrease in the frequency range where the transmission is sufficient. Increasing the height from $30 \,\mu\text{m}$ to $70 \,\mu\text{m}$ results in the $S_{21} \geq -1.5 \,\text{dB}$ bandwidth decreasing from 19.7 GHz



Fig. 4. Performance of the transition with $h_b = 30 \,\mu\text{m}$. The frequency range with above-70-% power transmission is highlighted with the gray region.



Fig. 5. Effect of varying the flip-chip bump height $h_{\rm b}$ on the performance of the transition.

to 9.1 GHz, whereas the peak value only decreased from -0.91 dB to -1.31 dB. Additionally, a local minimum in the coupling coefficient becomes more prominent and shifts to lower frequencies with larger $h_{\rm b}$. This stems from a structural resonance within the rest of the crack stop and could be mitigated by changing the number and location of the gaps in the crack stop, highlighted with blue arrows in Fig. 2(a).

IV. CONCLUSION

A non-galvanic antenna–IC transition has been designed for V-band applications. The transition utilizes the crack stop as a coupling element, simultaneously reducing structural resonances and realizing a connection between the chip and a PCB without the need for traditional interconnects. The transition reaches above-70-% power transmission between 42.3 GHz and 62 GHz, with a peak value of -0.91 dB at 49 GHz.

ACKNOWLEDGMENT

This work was supported by Business Finland through the ENTRY100GHz CELTIC-NEXT project, as well as Walter Ahlström Foundation and HPY Research Foundation. Research infrastructure provided by Aalto Electronics-ICT was utilized for this work.

REFERENCES

- [1] A. Pärssinen, M.-S. Alouini, M. Berg, T. Kürner, P. Kyösti, M. E. Leinonen, M. Matinmikko-Blue, E. McCune, U. Pfeiffer, and P. Wambacq. *White paper on RF enabling 6G : opportunities and challenges from technology to spectrum.* [Online]. Available: http://urn.fi/urn.isbn:9789526228419
- [2] K. E. Drenkhahn, A. Gadallah, A. Franzese, C. Wagner, and A. Malignaggi, "A V-band vector modulator based phase shifter in BiCMOS 0.13 µm SiGe technology," in 2020 15th Eur. Microw. Integr. Circuits Conf. (EuMIC), 2021, pp. 65–68.
- [3] B. Sadhu, X. Gu, and A. Valdes-Garcia, "The more (antennas), the merrier: A survey of silicon-based mm-wave phased arrays using multi-IC scaling," *IEEE Microw. Mag.*, vol. 20, no. 12, pp. 32–50, 2019.
- [4] J. H. S. Bergman, K. Ryynänen, J. Ala-Laurinaho, K. Stadius, J. Ryynänen, and V. Viikari, "Effects of an IC chip on an antenna-IC transition at 100 GHz," in *Proc. 17th Eur. Conf. Antennas Propag.* (EUCAP), 2023, pp. 1–5.
- [5] J. Haarla, J. Ala-Laurinaho, and V. Viikari, "Scalable 3-D-printable antenna array with liquid cooling for 28 GHz," *IEEE Trans. Antennas Propag.*, vol. 71, no. 6, pp. 5067–5078, 2023.
- [6] A. Jentzsch and W. Heinrich, "Theory and measurements of flip-chip interconnects for frequencies up to 100 GHz," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 5, pp. 871–878, 2001.
- [7] Dassault Systèmes, the 3DEXPERIENCE[®] Company.
 (2023) CST Studio Suite[®] (Version 2023.05). [Online]. Available: https://www.3ds.com/products-services/simulia/products/cststudio-suite/
- [8] H.-H. Lee, M.-J. Lii, S.-p. Jeng, and S.-Y. Hou, "Scribe line layout design," U.S. Patent US7 952 167B2, Apr. 27, 2007.
- [9] F. Khatkhatay, L. Popova, C.-C. Huang, H. J. Lee, Y. Zang, K. C. Ahn, C. Tsao, T. H. Lee, T. Mahalingam, H. Wang, A. Gupta, J. Lee, T. Ali, and J. M. Kaule, "Scribe line defect-induced yield loss in FINFET technology," *IEEE Trans. Semicond. Manuf.*, vol. 32, no. 4, pp. 387– 392, 2019.
- [10] S.-O. Kim and O. S. Park, "Crack stop and moisture barrier," U.S. Patent US7 741 715B2, Mar. 14, 2005.
- [11] M. Rabie, N. A. Polomoff, M. K. Hassan, V. L. Calero-DdelC, D. Degraw, M. Hecker, M. Thiele, and E. M. Bazizi, "Innovative design of crackstop wall for 14nm technology node and beyond," in 2018 IEEE 68th Electron. Compon. Technol. Conf. (ECTC), 2018, pp. 460–466.
- [12] D. Bang and T. A. Myers, "Electrically broken, but mechanically continuous die seal for integrated circuits," World Patent WO2011146755A1, May 19, 2011.
- [13] M. Keramat, S. S. Islam, and M. Heshami, "Seal ring for reducing noise coupling within a system-on-a-chip (SoC)," U.S. Patent US7 898 056B1, Dec. 9, 2008.
- [14] N. Frederick, Jr. and T. Myers, "Double broken seal ring," World Patent WO2 010 039 981A2, Oct. 1, 2009.