Kauppinen, Christoffer; Khan, Sabbir Ahmed; Sundqvist, Jonas; Suyatin, Dmitry B.; Suihkonen, Sami; Kauppinen, Esko I.; Sopanen, Markku

Atomic layer etching of gallium nitride (0001)

Published in:
Journal of Vacuum Science and Technology A

DOI:
10.1116/1.4993996

Published: 01/11/2017

Document Version
Publisher's PDF, also known as Version of record

Please cite the original version:
Kauppinen, C., Khan, S. A., Sundqvist, J., Suyatin, D. B., Suihkonen, S., Kauppinen, E. I., & Sopanen, M. (2017). Atomic layer etching of gallium nitride (0001). *Journal of Vacuum Science and Technology A*, *35*(6), 1-5. Article 060603. https://doi.org/10.1116/1.4993996

Atomic layer etching of gallium nitride (0001)

Christoffer Kauppinen, Sabbir Ahmed Khan, Jonas Sundqvist, Dmitry B. Suyatin, Sami Suihkonen, Esko I. Kauppinen, and Markku Sopanen

Citation: Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films **35**, 060603 (2017); doi: 10.1116/1.4993996

View online: http://dx.doi.org/10.1116/1.4993996

View Table of Contents: http://avs.scitation.org/toc/jva/35/6

Published by the American Vacuum Society

Atomic layer etching of gallium nitride (0001)

Christoffer Kauppinen[a),b)]
Department of Electronics and Nanoengineering, Micronova, Aalto University, P.O. Box 13500, FI-00076 Aalto, Finland

Sabbir Ahmed Khan[c)]
Department of Applied Physics, Aalto University School of Science, P.O. Box 15100, FI-00076 Aalto, Finland

Jonas Sundqvist
Fraunhofer Institute for Ceramic Technologies and Systems IKTS, Winterbergstr. 28, 01277 Dresden, Germany

Dmitry B. Suyatin
Division of Solid State Physics and NanoLund, Lund University, P.O. Box 118, SE-22100 Lund, Sweden

Sami Suihkonen
Department of Electronics and Nanoengineering, Micronova, Aalto University, P.O. Box 13500, FI-00076 Aalto, Finland

Esko I. Kauppinen
Department of Applied Physics, Aalto University School of Science, P.O. Box 15100, FI-00076 Aalto, Finland

Markku Sopanen
Department of Electronics and Nanoengineering, Micronova, Aalto University, P.O. Box 13500, FI-00076 Aalto, Finland

(Received 3 July 2017; accepted 7 August 2017; published 18 August 2017)

In this work, atomic layer etching (ALE) of thin film Ga-polar GaN(0001) is reported in detail using sequential surface modification by Cl_2 adsorption and removal of the modified surface layer by low energy Ar plasma exposure in a standard reactive ion etching system. The feasibility and reproducibility of the process are demonstrated by patterning GaN(0001) films by the ALE process using photoresist as an etch mask. The demonstrated ALE is deemed to be useful for the fabrication of nanoscale structures and high electron mobility transistors and expected to be adoptable for ALE of other materials. © *2017 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4993996]

With the recent development in 3D integration of nanoelectronics and continuous electronic device down-scaling, atomic scale process control becomes vital and very challenging. This recently triggered industrial interest in atomic layer etching (ALE) of traditional semiconductors.[1–3] ALE is a cyclic thin film etching process that uses self-limiting reactions,[4,5] in order to obtain a well defined etch per cycle. This can be a single atomic (or molecular, as in this work) layer etched in one etch cycle.[6–8] Historically, ALE was developed mostly using ion beam or neutral beam etching systems,[5] often custom built. Recently, it was suggested that conventional plasma etch tools can be used for ALE (Ref. 9), indeed ALE of Si in a close-to-conventional plasma etch tool has been reported by Goodyear and Cooke,[10] and the ALE of silicon oxide in a conventional tool has also been demonstrated.[11] Recent advances in III-N semiconductors also call for atomic scale control of etch processes and defect free nanofabrication. Metal organic vapor phase epitaxy (MOVPE) grown AlGaN/GaN heterostructure high electron mobility transistors (HEMTs) have a well-defined layered structure with the two-dimensional electron gas (2DEG)[12,13] and can benefit greatly from recessed gates which allow more powerful modulation of the 2DEG.[14–16] Etching of the gate recess is challenging as conventional reactive ion etching (RIE) does not provide sufficiently good control over the etch process, and high energy ions can cause damage to the 2DEG layer.[17,18] These problems can be avoided if GaN ALE is used in etching these recesses. In addition to GaN HEMTs, research in 2D GaN has been active,[19] but the techniques of growing a single monolayer or few monolayers of GaN are challenging. GaN ALE could provide an alternative method to the 2D material community by a controlled thinning of high quality films of GaN down to a few atomic layers. There have been reports on directional GaN ALE,[12,20,21] but a detailed description of the process including crystal orientation and polarity has not been presented until now. In this letter, we demonstrate and characterize the ALE of monocrystalline Ga-polar GaN(0001) thin films, using a standard RIE system.

GaN samples were grown on 2 in. sapphire substrates using a vertical reactor MOVPE system (Thomas-Swan 3×2 in.). Trimethylgallium and ammonia were used as the sources of Ga and N, respectively. The c-plane sapphire substrates were preheated in a H_2 ambient at 1100 °C for 300 s, after which the substrate was nitridated under ammonia flow at 535 °C. This was followed by the growth of a GaN nucleation layer at 535 °C and subsequent annealing at 1050 °C, after which a 3.06 μm-thick GaN buffer layer was grown at 1025 °C. Then, a 1.46 μm-thick "device" GaN layer was grown. The growth utilized a nucleation layer optimized

[a)]C. Kauppinen and S. A. Khan contributed equally to this work.
[b)]Electronic mail: christoffer.kauppinen@aalto.fi
[c)]Electronic mail: sabbir.khan@aalto.fi

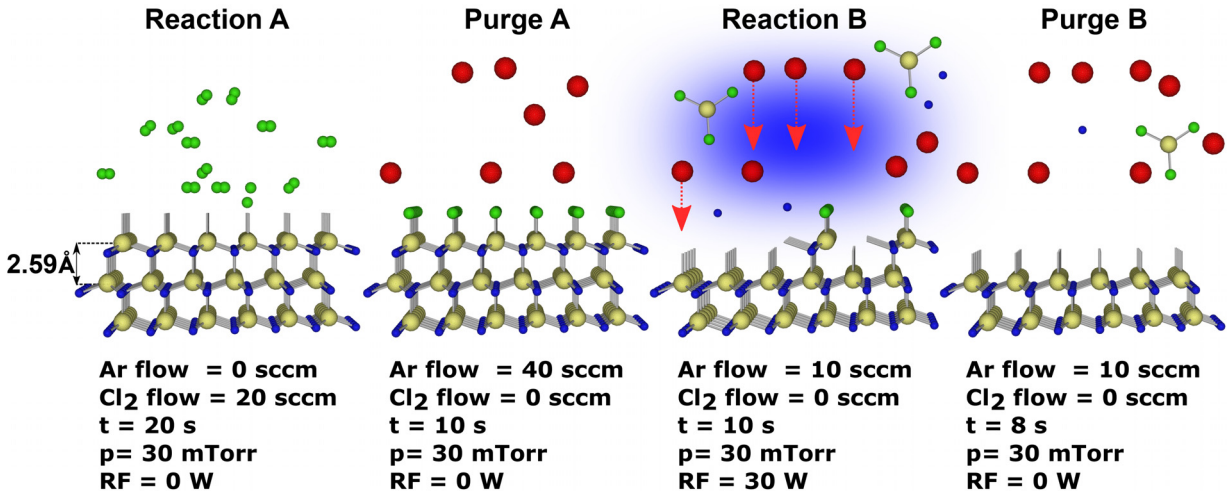

FIG. 1. (Color online) GaN atomic layer etching process and initial parameters. In reaction (A), the GaN surface (Ga-atoms larger and N-atoms smaller) is modified with Cl_2 (small diatoms), forming a chlorinated surface, and later in reaction (B), energetic Ar ions (Ar atoms represented by large individual spheres and Ar ions spheres with arrows) remove this modified surface. One full cycle also consists of two purges after each reaction, which are crucial for self-limited reactions. The molecular layer thickness is shown in the leftmost schematic.

two-step growth.[22,23] After growth, etch masks were fabricated on the wafers. A standard 1.5 μm photoresist (AZ5214e) layer was spin-coated on all wafers and photolithographically patterned resulting in an array of 100 μm $\times$ 1 cm stripes with macroscopic spacings.

An inductively coupled plasma (ICP)-RIE system (Oxford Instruments Plasmalab 100) was used for developing the GaN ALE process. A similar system has been recently used to demonstrate Si and SiO_2 ALE.[10] The samples were analyzed using atomic force microscopy (AFM). The GaN samples were treated with hydrochloric acid before ALE in order to selectively remove the native oxide.

Figure 1 shows schematically the GaN ALE process, consisting of surface chlorination [reaction (A)], purging excess chlorine (purge A), removing chlorinated surface with Ar ions [reaction (B)], and finally purging the byproducts (purge B). After preliminary experiments, ALE was observed in GaN with the process parameters presented in Fig. 1. We observed that the ALE energy window for GaN is between RF powers of 10 W (DC bias 5 V, negligible etch rate) and 50 W (DC bias 24 V, RIE-like etch process behavior, high rate with surface roughness visible with an optical microscope). The ALE process with a RF power of 30 W (DC bias 16 V) is presented in Fig. 1, as this process provided repeatable ALE. The etch rate as a function of the DC bias is presented in Fig. 2. The ICP power was kept zero at all times, which means that the ALE process was effectively realized in a RIE tool. The ICP-RIE substrate electrode was set to a constant temperature of 23 °C in all samples.

Figure 3(a) shows the etch depth and the etch rate corresponding to the ALE parameters in Fig. 1 as a function of the number of cycles. The etch rate does not depend on the number of cycles performed, and correspondingly, the etch depth increases linearly with the number of cycles. The etch depth and etch rate were measured by AFM from the difference in the height between unmasked areas and masked areas after photoresist removal. The photoresist was removed by immersing the wafers into acetone for 10 min and then rinsing with 2-propanol and deionized water.

In order to confirm ALE, we performed a synergy test,[4,24] with the initial ALE parameters shown in Fig. 1. The results of the synergy test are shown in Fig. 3(b). In the synergy test, the samples were processed with only one of the major steps [reactions (A) or (B)] with purging. Ideally, neither step should individually cause etching. In the synergy test, the GaN samples were exposed first to just Cl_2 [reaction (A)] for 200 cycles [reaction (B), the removal step was excluded]. Careful examination by AFM disclosed no measurable etching after exposure to just gaseous chlorine pulses, confirming the ideal ALE behavior of reaction (A). A similar experiment was performed with just Ar plasma exposure [reaction (B)] for 200 cycles [reaction (A), the surface modification was excluded], which leads to an etch rate of 0.58 Å/cycle, seen in Fig. 3(b). The observed etching is due to Ar ions sputtering the sample surface. This small etch rate indicates a nonideal ALE process, which is common when using Ar ions in the removal step as the ion energy distribution can be wider than the ALE window.[4] The undesired sputtering can

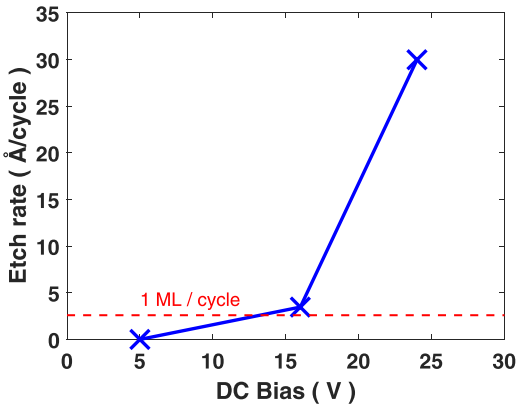

FIG. 2. (Color online) Etch rate as a function of the DC bias. DC bias varied with RF power. Other parameters are from Fig. 1.

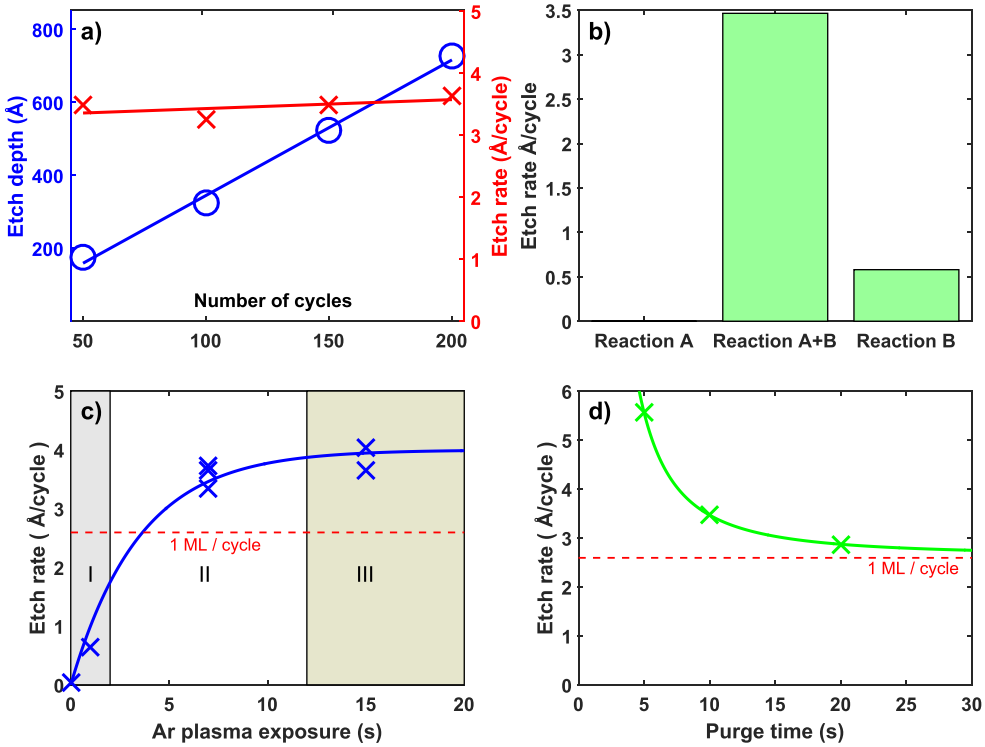

FIG. 3. (Color online) (a) Etch depth (circles) and etch rate (crosses) of GaN as a function of the number of ALE cycles, using the parameters in Fig. 1. (b) Etch rate of GaN after exposure to only Cl_2 [reaction (A)] and only Ar plasma [reaction (B)] for 200 cycles. In the middle bar, both reactions are combined [reaction (A) + reaction (B), 200 cycles], which leads to a significantly higher etch rate than the individual reactions. (c) Etch rate as a function of the Ar plasma exposure time. (d) Etch rate as a function of the purge A time. Figure 1 shows the used parameters excluding the parameter which is varied.

also cause other unwanted phenomena such as micromasking, as the mask material can also be sputtered on the unmasked area.[4] The combined etch rate of sequential Cl_2 and Ar^+ exposure is also shown in Fig. 3(b). It can be seen that combining both reactions into the ALE sequence produces synergy and the combined etch rate is much higher than the sum of the individual etch rates.

Figure 3(c) shows the etch rate as a function of the Ar ion exposure time (ion dose), with the other parameters kept the same as in Fig. 1. The dashed line shows the etch rate for one molecular layer (ML) per cycle.[25] Figure 3(c) is divided into three regions. In region I, the etch rate increases strongly and almost linearly with respect to the Ar ion dose since the surface is highly chlorinated and ion bombardment can easily knock out parts of the modified layer. In region II, less chlorine modified surface is left after initial Ar ion bombardment, which leads to a bowed slope. Finally, in region III, only the pristine GaN surface is left for interaction with Ar ions, and accordingly, very little additional etching can occur. This confirms that GaN ALE is achieved. Ideally, region III should be completely saturated.[4] However, region III of Fig. 3(c) is expected to exhibit a very slight upward slope indicating quasisaturation[4] due to the sputtering component, see Fig. 3(b). Quasisaturation means that small additional etching can be obtained with a longer Ar bombardment time. In addition to sputtering, chlorine remaining in the chamber or on the chamber walls can also contribute to RIE-like parasitic etching, which can explain significantly larger than 1 ML per cycle etch rate in region III.

To study the possible effect of residual chlorine, the purge A time was varied and corresponding etch rates were measured. Figure 3(d) shows the etch per cycle as a function of Cl_2 purging time (purge A). From Fig. 3(d), we deduce that a significant amount of chlorine remains in the chamber after reaction (A). With insufficient purging time, remaining chlorine molecules contribute to higher etch rates during reaction (B). As shown in Fig. 3(d), it takes approximately 20 s of purging for the chamber with Ar after chlorination for the etch rate to saturate approximately to 1 ML of GaN. This etch per cycle is 2.87 Å/cycle, compared to the ML thickness of 2.59 Å.[25] Similar behavior of 1 ML etching has been reported before for GaAs using the same chemistry.[7] Purge B time is less critical since very little Cl_2 remains in the chamber after purge A and reaction (B). We determine that this 20 s purge time is optimal for obtaining close to 1 ML etch per cycle. Goodyear and Cooke reported on significantly shorter purge times using a modified version of the same reactor that was used in this work.[10] This modified reactor allowed ultrashort (40 ms) chlorine doses, and it is not surprising that this allowed shorter (2–5 s) chlorine purge times to be used.

The etch mechanism of GaN ALE is surprisingly complex. When exposing wurtzite GaN(0001) surfaces to chlorine gas, chlorine preferentially reacts with Ga to form different gallium chlorides on the surface.[26] Gallium chlorides are known to have low boiling points[27] and are easily removed by the Ar ions. Recent molecular dynamic simulations of Ar ion bombardment on chlorinated wurtzite

GaN(0001) surfaces reveal that the sputtering yield of chlorinated Ga on the GaN surface is much higher than that of chlorinated N on the GaN surface.[28] On nonchlorinated surfaces, there is experimental evidence that high energy (1 keV) Ar ions preferentially sputter N over Ga,[26] and Harafuji and Kawamura[28,29] also pointed out that this effect is more profound at low energies. The simulated sputtering energy threshold is 100 eV for N and 250–400 eV for Ga.[29] This is reasonable just by looking at the crystal structure (see Fig. 1), as N-atoms have just one covalent bond to the bulk of the crystal below, but surface Ga-atoms have three, which makes kinetic removal of surface-N easier than that of surface-Ga. In this experiment with low DC bias (DC bias 16 V), sputtering of N is far more likely than sputtering of Ga as even the N sputtering is energy limited. Thus, the sputtering of nonchlorinated Ga-surface atoms is small, compared to the sputtering of chlorinated Ga. In fact, sputtering of nonchlorinated surface-Ga cannot be observed in simulations with low energies.[29] Sputtering occurs as a Ga-N pair and not as a single Ga-atom in these simulations.[29] This leads us to conclude that the etch mechanism of our GaN ALE is ion assisted removal of chlorinated surface Ga and Ar ion sputtering of singly bonded surface N-atoms. Surface Ga-atoms are chlorinated in reaction (A) (see Fig. 1), and then in purge A, excess chlorine is removed with longer purges [see Fig. 3(d)]. After that, in reaction (B), the chlorinated Ga-atoms are removed by the Ar ions, the underlying weakly bonded N-atoms are sputtered away in the same Ar ion pulse, and finally, in purge B, byproducts are purged away. This results in the removal of approximately 1 ML of GaN, when purge A is sufficiently long, see Fig. 3(d). It must be noted that these findings hold only for GaN(0001). A nitrogen-polar material can behave very differently as the number of bonds for surface-Ga and surface-N is switched.

An AFM image of an ALE fabricated GaN stripe using parameters from Fig. 1 is shown in Fig. 4. An ideal ALE process should not damage the etched structures, and the sample surface should be smooth and clean after etching.[4,5] In Fig. 4, small additional roughness is induced on the sample as the root mean square (RMS) surface roughness increases from 1.9 to 2.5 nm on the etched surface. The increase in roughness can partially be attributed to nonidealities of the ALE and partly to photoresist residues left after acetone immersion. A clear fencing (also known as veil) effect[30,31] is also observed on the stripe due to residual photoresist. The sidewall edge roughness in Fig. 4 is due to the initial edge of the photomask.

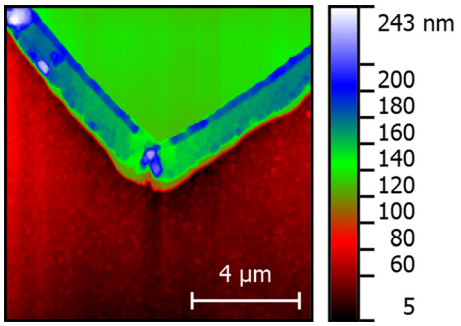

FIG. 4. (Color online) Etched GaN surface (200 cycles) after photoresist removal, measured using AFM. The etched stripe height is 72 nm in this case. The corner of the 1 cm-long stripe is in the image. The RMS surface roughness is 1.9 nm on the masked area after photoresist removal and 2.5 nm on the etched area. Major fencing (Refs. 30 and 31) is seen on the edge of the masked (flat green) area.

In conclusion, ALE of Ga-polar GaN(0001) using a standard RIE system is achieved in this work and reported in detail, including all process parameters. The GaN ALE process is demonstrated by etching mesa structures masked with photoresist, thus demonstrating the suitability of the process for nanofabrication of GaN devices. The etch rate is shown to be constant with the number of ALE cycles, and the etch rate saturates when increasing the Ar ion dose. Almost exactly (0.28 Å error) 1 ML etch per cycle is achieved with longer purge times. All in all, the GaN ALE demonstrated in this work provides a new method for atomic precision nanofabrication of Ga-polar GaN(0001) devices using widely available RIE systems and can be potentially adopted for ALE of various materials.

ALE experiments in this research project were carried out at the Micronova Nanofabrication Centre (Aalto Nanofab) of Aalto University. The authors would like to thank all the users of the ICP-RIE for patience while the authors were developing the GaN ALE process. This work was supported by the MOPPI project of Aalto University AEF research program.

[1]C. M. Huard, Y. Zhang, S. Sriraman, A. Paterson, K. J. Kanarik, and M. J. Kushner, J. Vac. Sci. Technol., A **35**, 031306 (2017).
[2]D. Hisamoto *et al.*, IEEE Trans. Electron Devices **47**, 2320 (2000).
[3]K. T. Park *et al.*, IEEE J. Solid-State Circuits **50**, 204 (2015).
[4]K. J. Kanarik, T. Lill, E. A. Hudson, S. Sriraman, S. Tan, J. Marks, V. Vahedi, and R. A. Gottscho, J. Vac. Sci. Technol., A **33**, 020802 (2015).
[5]T. Faraz, F. Roozeboom, H. Knoops, and W. Kessels, ECS J. Solid State Sci. Technol. **4**, N5023 (2015).
[6]M. N. Yoder, U.S. patent 4756794 A (12 July 1988).
[7]Y. Aoyagi, K. Shinmura, K. Kawasaki, T. Tanaka, K. Gamo, S. Namba, and I. Nakamoto, Appl. Phys. Lett. **60**, 968 (1992).
[8]G. S. Oehrlein, D. Metzler, and C. Li, ECS J. Solid State Sci. Technol. **4**, N5041 (2015).
[9]M. J. Cooke, ECS J. Solid State Sci. Technol. **4**, N5001 (2015).
[10]A. Goodyear and M. Cooke, J. Vac. Sci. Technol., A **35**, 01A105 (2017).
[11]D. Metzler *et al.*, J. Vac. Sci. Technol., A **34**, 01B102 (2016).
[12]W. Yang, T. Ohba, S. Tan, K. J. Kanarik, J. Marks, and K. Nojiri, U.S. patent 15/173,358 (8 December 2016).
[13]J. Lemettinen, C. Kauppinen, M. Rudzinski, A. Haapalinna, T. Tuomi, and S. Suihkonen, Semicond. Sci. Technol. **32**, 045003 (2017).
[14]W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, IEEE Trans. Electron Devices **53**, 356 (2006).
[15]T. Egawa, G.-Y. Zhao, H. Ishikawa, H. Umeno, and T. Jimbo, IEEE Trans. Electron Devices **48**, 603 (2001).
[16]W. Lanford, T. Tanaka, Y. Otoki, and I. Adesida, Electron. Lett. **41**, 449 (2005).
[17]F. Khan, V. Kumar, and I. Adesida, Electrochem. Solid-State Lett. **5**, G8 (2002).
[18]W.-K. Wang, Y.-J. Li, C.-K. Lin, Y.-J. Chan, G.-T. Chen, and J.-I. Chyi, IEEE Electron Device Lett. **25**, 52 (2004).
[19]Z. Y. Al Balushi *et al.*, Nat. Mater. **15**, 1166 (2016).
[20]K. J. Kanarik *et al.*, J. Vac. Sci. Technol., A **35**, 05C302 (2017).
[21]T. Ohba, W. Yang, S. Tan, K. Kanarik, and K. Nojiri, Jpn. J. Appl. Phys., Part 1 **56**, 06HB06 (2017).
[22]T. Lang, M. Odnoblyudov, V. Bougrov, S. Suihkonen, M. Sopanen, and H. Lipsanen, J. Cryst. Growth **292**, 26 (2006).

[23]H. Amano, N. Sawaki, I. Akasaki, and Y. Toyoda, Appl. Phys. Lett. **48**, 353 (1986).
[24]G. D. Sherpa and A. Ranjan, J. Vac. Sci. Technol., A **35**, 01A102 (2017).
[25]M. Leszczynski *et al*., Appl. Phys. Lett. **69**, 73 (1996).
[26]Y.-H. Lai, C.-T. Yeh, J.-M. Hwang, H.-L. Hwang, C.-T. Chen, and W.-H. Hung, J. Phys. Chem. B **105**, 10029 (2001).
[27]S. Pearton, R. Shul, and F. Ren, MRS Internet J. Nitride Semicond. Res. **5**, e11 (2000).
[28]K. Harafuji and K. Kawamura, Jpn. J. Appl. Phys. **49**, 08JE03 (2010).
[29]K. Harafuji and K. Kawamura, Jpn. J. Appl. Phys., Part 1 **47**, 1536 (2008).
[30]M. Sandberg, M. R. Vissers, J. S. Kline, M. Weides, J. Gao, D. S. Wisbey, and D. P. Pappas, Appl. Phys. Lett. **100**, 262605 (2012).
[31]A. Aydemir and T. Akin, J. Micromech. Microeng. **22**, 074004 (2012).