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A Sub-nW Temperature Invariant Voltage Reference in a Unipolar TFT-based Flexible IC Technology

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***Abstract*—Voltage reference circuits are crucial for any mixed-signal circuits, providing PVT (Process, Voltage, Temperature) robust output for the system's stability and accuracy. This paper presents a novel voltage reference circuit implemented in an indium gallium zinc oxide (IGZO) based thin film transistors (TFT) technology, proposing for the first time a sub-nanowatt, area-efficient circuit realized with only a single N-type TFT in a 600 nm technology. The design occupies a minimal area of 27x37 µm², operates across a broad supply voltage range from 0.5 V to 3 V, and maintains functionality from 0 °C to 100 °C. The circuit has an ultra-low power consumption between 0.75 nW to 1.2 nW while achieving an output voltage of 454 mV with a temperature coefficient (TC) as low as 28.9 ppm/°C. The simulated results, which include process variation, temperature dependence, line sensitivity and power supply rejection ratio measurements, underline the circuit's potential for high-efficiency, low-power applications in next-generation flexible electronics.**

***Index Terms*—Voltage reference, flexible integrated circuits, IGZO, TFT, thermal compensation, ultra-low power.**

I. Introduction

The emergence of flexible electronics has paved the way for a number of applications, enabling the development of innovative applications. The properties of flexible substrates offer versatility and low production costs. This integration not only advances wireless sensing and biomedical fields but also opens the door to a diverse array of applications. Flexible integrated circuits made by IGZO based TFTs have been recently gaining a lot of attention in diverse applications such as 32-bit microcontrollers [1], radio-frequency identification (RFID) tags [2] and even machine learning processing engines [3]. For the past few decades, many analog TFT-based circuits have been developed, including operational transconductance amplifiers (OTA) [4], [5], oscillators [5], rectifiers [6], analog to digital converters (ADC) [7], etc. Although much development has been going on in designing digital and analog TFT-based circuits, there remains a critical gap in the development of reference generator circuits, which are essential components for any mixed-signal circuit architecture. One such work [8] that discusses voltage reference in TFT technology uses a traditional beta-multiplier current reference and is developed on a glass substrate, consuming power of 89.7 µW and an area of 400x380 µm^2, another work [9] realizes a reference generator in an ADC by using resistors consuming a high power of 17.7 mW. These approaches often require multiple device types or high power consumption, underscoring the challenge of achieving PVT robust, ultra-low power voltage references with the unipolar device in TFT technology.

Although there exist circuits which can consume sub nW of power with a very small area using NMOS only devices [10]–[15], these work uses bulk complementary metal-oxide-semiconductor (CMOS) technology and are implemented by more than one type of NMOS-device. The commonly used transistors by these circuits are zero threshold native transistors stacked with a thick oxide device [10], [13], [14], and thin oxide devices [12]. Due to the choice of using various types of transistors in the CMOS technology, it is possible to realise these types of references. However, the presence of one single type of unipolar device in TFT makes it challenging to obtain a PVT robust sub-nW voltage reference.

Addressing this critical gap in mixed-signal circuit design, this paper introduces an ultra-low power (sub-nW) and area, voltage reference circuit employing a single N-type TFT. By leveraging a singular N-type TFT, the design removes the traditional dependence on multiple device types, setting a new standard for low area and simplicity in voltage reference circuits. The circuit achieves temperature invariant voltage output of achieving comparable performance with the state-of-the-art CMOS circuit. The post-layout simulations of the ready-to-be-fabricated circuit verify the functionality of the proposed design.

II. Flexible circuit design description

The schematic of the proposed circuit is shown in Figure 1. The circuit consists of five stacked NMOS based TFTs. M_{1A} and M_{1B} provide the required regulation to the output voltage. Since the V_{GS} of M_{1B} is zero, the drain-source resistance of this device is connected to the impedance of diode-connected series transistors $M_{2\text{-}4}$. According to [15], the output voltage of this circuit (neglecting the body effect) can be denoted by:

$$V_{\text{TEMP}} = \underbrace{V_{\text{TH}_1} - V_{\text{TH}_{2,3,4}}}_{\text{CTAT}} + \underbrace{mV_T \ln \frac{C_{\text{OX}_1}\left(\frac{W_1}{L_1}\right)}{C_{\text{OX}_{2,3,4}}\left(\frac{W_{2,3,4}}{L_{2,3,4}}\right)}}_{\text{PTAT}} \quad (1)$$

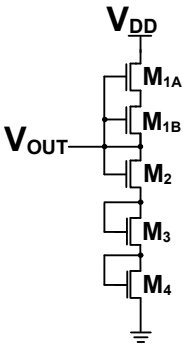

Fig. 1. Schematic description of the proposed voltage reference using a single type of NMOS.

where W and L are the width and length of the device, C_{OX} is the gate oxide thickness, m is the subthreshold slope, V_T is the thermal voltage, V_{TH} is the threshold voltage. Since the threshold voltages are complementary to absolute temperature (CTAT) [16] and, therefore, by proper sizing or transistors, the proportional to absolute temperature (PTAT) behaviour of the circuit can be optimized to obtain a temperature invariant circuit. By using the same type of device, the dependence of the circuit on process variations is minimised as well, the results of which are discussed in the next section.

III. Post-Layout Simulation Results and Comparison

The circuit has been implemented in a 600 nm IGZO TFT-based technology (Pragmatic FlexIC [17]) on an insulating substrate hence, there is no physical connection between the bulk and the devices. The post-layout verification of the circuit was done across various supply voltage, temperature and process corners. The evaluation of the circuit was thoroughly done only across process corners, including fast, slow, and typical, to ensure a robust analysis under the given constraints. Given the technology's evolving nature, Monte Carlo distribution simulation was not performed because of the models unavailability at the time of this research.

Figure 2 shows the layout of the implemented design. As shown in the layout, the circuit occupies an area of 27x37 μm^2. The circuit operates for a wide supply voltage (V_{DD}) range of 0.5 V to 3 V and a temperature range of 0°C to 100°C. The

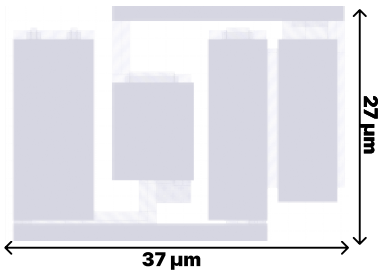

Fig. 2. Layout of the proposed voltage reference circuit in TFT-based IGZO technology.

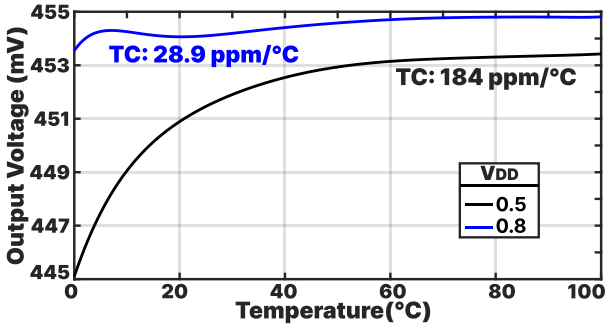

Fig. 3. Simulated thermal dependence of the output voltage w.r.t. 0.5 V and 0.8 V supply voltages.

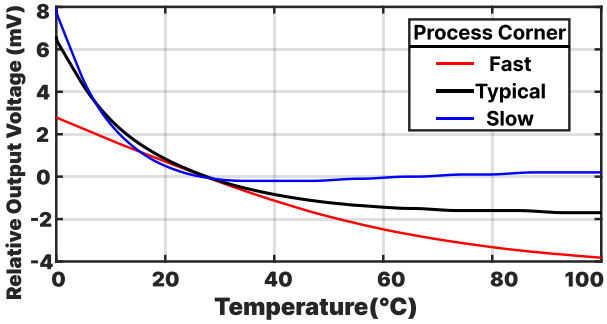

Fig. 4. Output voltage error relative to room temperature of 27°C across various process corners.

circuit has an ultra-low power consumption of 0.75 nW at 0.5 V of V_{DD} and 1.2 nW at 0.8 V. The circuit generates an output voltage of 454 mV at TC of 184 ppm/°C at V_{DD} of 0.5 V, and the lowest TC this reference generator can achieve is 28.9 ppm/°C at V_{DD} of 0.8 V as shown in Figure 3.

To evaluate the robustness of the circuit, Figure 4 shows the post-layout simulation plot illustrating the relative output voltage w.r.t. room temperature and its error for various process corners at an operating voltage of 0.5 V. A maximum error of 12 mV is obtained in this simulation result, showing the feasibility of the circuit for fabrication.

Line sensitivity of the output voltage w.r.t to the supply voltage is shown in Figure 5, the circuit can operate at a

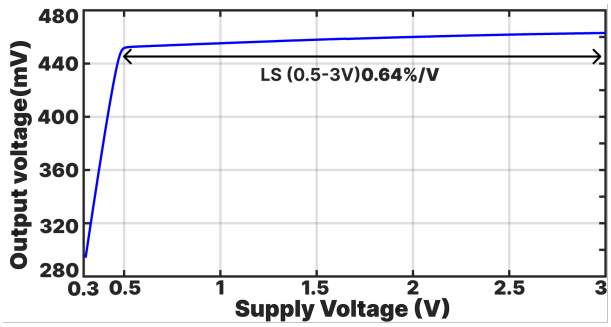

Fig. 5. Simulated output voltage dependence of the circuit on the input supply voltage at room temperature.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE OF THE ART

	This Work	[8]	[10]	[11]	[12]	[13]	[14]
Technology	IGZO-TFT 600nm	LTPS-TFT 3µm	CMOS 130nm	CMOS 180nm	CMOS 180nm	CMOS 180nm	CMOS 180nm
Flexible	Yes	No	No	No	No	No	No
Number of devices/components used	1	4	2	3	3	5	3
Supply range (V)	0.5-3	10	0.5-3	1-1.8	0.6-1.8	1.6-2.8	0.6-2
Output Voltage (mV) @27°C	454	6870	174.9	692.6	431	704	350
Temperature range (°C)	0 to 100	25 to 125	-20 to 80	-20 to 100	0 to 85	0 to 125	-40 to 80
Minimum TC (ppm/°C)	28.9	195	16.9	25	52	92.2	35.9
Power (nW)@VDD	0.75@0.5V	89700@10V	0.0044@0.5V	0.192@1V	0.023@0.6V	0.2789@1.6V	0.15@0.6V
Area (μm^2)	999	152000	1350	4500	3000	13900	5400
LS (%/V)	0.64	-	0.033	0.02	0.03	0.004	0.093
PSRR (dB) @100 Hz	-45	-	-53	-55	-47	-69.6	-39

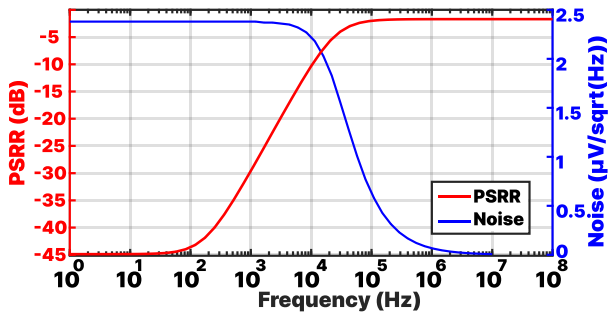

Fig. 6. PSRR of the output reference voltage and noise of the circuit

minimum voltage of 0.5 V and can be powered upto V_{DD} of 3 V. For this V_{DD} range, the circuit shows a line sensitivity of 0.64 %/V. Additionally, the power supply rejection ratio of -45 dB is observed for frequencies up to 100 Hz as shown in Figure 6. This figure also shows that the circuit has a low noise of 2.5 $\mu V/\sqrt{Hz}$, which is lower than the state of the art [14].

Table I compares this work with the related state-of-the-art work based on TFT as well as circuits using CMOS technology. It can be seen that this circuit obtains comparable power consumption of 0.75 nW, markedly lower than the values reported in TFT-based technology, [8]. The design's simplicity, using just one device, greatly reduces the circuit's area to 999 μm^2, contrasting sharply with the larger areas required by all other works. A temperature coefficient (TC) of 28.9 ppm/°C shows the circuit achieving better performance in some cases when compared to other TFT [8] and CMOS technology [12]–[14]. Thus demonstrating a balanced performance between power efficiency and temperature dependence.

IV. CONCLUSION

This work presents an ultra-low power, compact, PVT robust voltage reference circuit for flexible ICs. The simple design of the circuit using only a single N-type TFT makes the circuit compact, occupying an area of 27x37 µm². This low area is achieved within the constraints of a 600 nm technology, which is inherently larger in size compared to CMOS processes like 130 nm or 180 nm technologies. The circuit achieves an ultra low power consumption between 0.75 nW and 1.2 nW while maintaining a consistent output voltage with a low-temperature coefficient of 28.9 ppm/°C. The comparison with state-of-the-art works further highlights the circuit's performance comparable with CMOS circuits w.r.t power consumption, line sensitivity, PSRR and temperature stability, positioning it as a promising solution for flexible ultra-low-power applications.

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