Liu, Shenyi; Vuorinen, Vesa; Liu, Xing; Fredrikson, Olli; Brand, Sebastian; Tiwary, Nikhilendu; Lutz, Josef; Paulasto-Krockel, Mervi

Fatigue Crack Networks in Die-Attach Layers of IGBT Modules Under a Power Cycling Test

Published in:
IEEE Transactions on Power Electronics

DOI:
10.1109/TPEL.2024.3447909

Published: 01/01/2024

Document Version
Publisher's PDF, also known as Version of record

Fatigue Crack Networks in Die-Attach Layers of IGBT Modules Under a Power Cycling Test

Shenyi Liu, Vesa Vuorinen, Xing Liu, Olli Fredrikson, Sebastian Brand, Nikhilendu Tiwary, *Member, IEEE*, Josef Lutz, *Senior Member, IEEE*, and Mervi Paulasto-Kröckel, *Member, IEEE*

***Abstract*—The die-attach layer is a vulnerable structure that is important to the reliability of an insulated-gate bipolar transistor (IGBT) module. A new failure mechanism named fatigue crack network (FCN) has been identified in the central area of the IGBT modules' solder layer. In this article, to investigate the formation mechanism of the FCN, a fast power cycling test (PCT) (current on 0.2 s and current off 0.4 s) was designed and performed on a commercial IGBT module. Subsequently, scanning acoustic microscopy and X-ray imaging were used for nondestructive inspection of the defects of the solder layer. The cross section was based on the nondestructive inspection results. Then, electron backscattered diffraction analysis was carried out on both observed vertical and horizontal cracks. As a result, both networked vertical cracks at the center and horizontal cracks at the edge of the solder layer were detected. The recrystallization occurred during the PCT. The voids and cracks emerged at high-angle grain boundaries. A finite element simulation was performed to understand the driving force of FCN qualitatively. The stress simulation results indicate that under time-dependent multiaxial stress at the center of the solder, the defects nucleated, expanded, and connected vertically to form the FCNs.**

***Index Terms*—Die-attach, fast power cycling test (PCT), fatigue crack network (FCN), insulated-gate bipolar transistor (IGBT), Sn-Ag-Cu (SAC) solder.**

I. Introduction

POWER semiconductors are widely employed in various fields, including electric vehicles, photovoltaic systems, and wireless power transfer [1], [2], [3]. These applications require high switching frequencies combined with high current densities and operating temperatures, leading to new reliability challenges for power devices [4]. Given that power semiconductors play a crucial role as one of the most critical components in power electronics systems, it is imperative to study the reliability of these devices, such as insulated-gate bipolar transistors (IGBTs).The power cycling test (PCT) is one of the most important methods for investigating the reliability of IGBT modules [5]. This testing approach not only accelerates the testing process but also facilitates active control of power modules. The failures observed under actual operating conditions, including degradation of the die-attach layer and bond wires, can be simulated during the PCT [6]. Schwabe et al. [7] applied a fast PCT to an IGBT module, with load and cooling times in each cycle less than 1 s. During testing, a large number of voids were exclusively detected within the central region of the solder layer. Notably, the solder at the chip's periphery remained intact, which distinguishes this from the horizontal cracks typically observed during thermal cycling tests (TCTs) [8] and standard PCTs [9]. However, a comprehensive explanation for the failure mechanism was not provided in [7]. Sugimoto et al. [10] found similar small vertical cracks that emerged at the center of the solder layer in a Si/Sn-Ag-Cu (SAC) solder/Si joint specimen after performing a TCT. A subsequent study by the same authors concluded that with more cycles applied, these individual vertical cracks merged and formed a fatigue crack network (FCN) [11]. FCNs have been observed to occur in high-lead and SAC solder layers and sintered Ag joints in the center of the die-attach layer of samples after applying PCTs [12], [13]. In [13], the horizontal cracks at the edge of the solder and the FCN were found in cross-sectional results. Considering that FCN occupied 70% or more of the die-attach area and the length of horizontal cracks is relatively short, it was concluded in [13] that only FCN has a significant impact on the reliability of IGBT modules.

FCNs were detected in various solder materials and sample structures under different testing conditions by X-ray imaging [11], [12], [13]. The X-ray imaging results of the solder layer of IGBT modules after standard PCT were compared with the results obtained using scanning acoustic microscopy (SAM) [14]. X-ray imaging can observe the density variation of vertical cracks, while horizontal cracks are only visible through SAM. Therefore, Hartmann et al. [14] concluded that it is not feasible to confirm the presence of both horizontal and vertical

Received 28 December 2023; revised 22 April 2024 and 28 June 2024; accepted 7 August 2024. Date of publication 22 August 2024; date of current version 7 October 2024. This work was supported by the PowerizeD project. The project is supported by the Chips Joint Undertaking and its members, including the top-up funding by the national Authorities of Germany, Belgium, Spain, Sweden, Netherlands, Austria, Italy, Greece, Latvia, Finland, Hungary, Romania, and Switzerland, under grant agreement number 101096387. Co-funded by European Union. Recommended for publication by Associate Editor K. Sheng. *(Corresponding author: Shenyi Liu.)*

Shenyi Liu, Vesa Vuorinen, Nikhilendu Tiwary, and Mervi Paulasto-Kröckel are with the Department of Electrical Engineering and Automation, School of Electrical Engineering, Aalto University, FI-00076 Aalto, Finland (e-mail: shenyi.liu@aalto.fi; vesa.vuorinen@aalto.fi; nikhilendu.tiwary@aalto.fi; mervi.paulasto@aalto.fi).

Xing Liu and Josef Lutz are with the Chair of Power Electronics, Chemnitz University of Technology, 09126 Chemnitz, Germany (e-mail: xing.liu@etit.tu-chemnitz.de; josef.lutz@etit.tu-chemnitz.de).

Olli Fredrikson is with the ABB Drives, Q&R Laboratory, 00170 Helsinki, Finland (e-mail: olli.fredrikson@fi.abb.com).

Sebastian Brand is with the Fraunhofer Institute for Microstructure of Materials and Systems IMWS, 06120 Halle, Germany (e-mail: sebastian.brand@imws.fraunhofer.de).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3447909.

Digital Object Identifier 10.1109/TPEL.2024.3447909

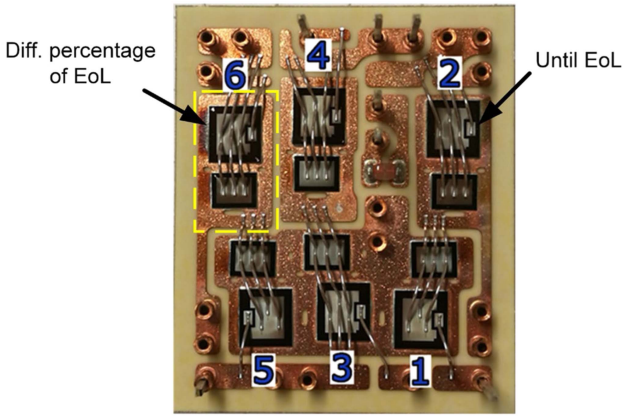


Fig. 1. Internal layout of the IGBT module with six subsystems.

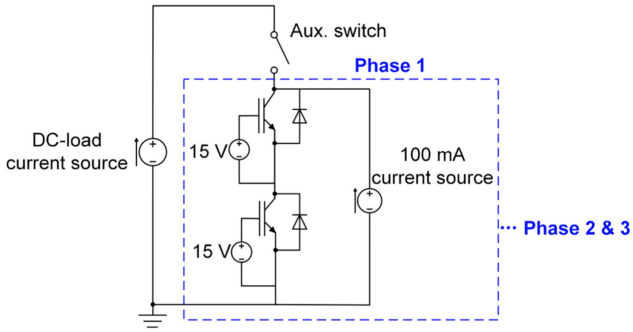


Fig. 2. Simplified power cycling test circuit.

cracks in the solder layer solely by employing X-ray imaging. Moreover, advanced computed tomography scanning has been used to detect the voids and measure the voids' size in the solder layer of the IGBT module [15]. Therefore, a comprehensive comparison of the typical methods and their correlation with failure mechanisms is essential. Furthermore, it is necessary to conduct further research to accurately characterize the propagation and microstructure evolution of FCN and its dissimilarity from horizontal cracks in an IGBT module during the PCT.

In this study, a fast PCT is designed and applied to commercial IGBT modules. A finite element (FE) simulation is constructed to demonstrate the temperature and stress distribution in the solder layer during the PCT. Then, the inspections using SAM and X-ray methods were employed to investigate the degradation mechanisms in the die-attach solder layer. The combined use of SAM and X-ray methods confirmed both vertical and horizontal cracks before resorting to any destructive inspection on the IGBT samples. Finally, a comprehensive cross-sectional analysis is performed using electron backscattered diffraction (EBSD) analysis to elucidate the nucleation and propagation mechanisms of defects. This analysis also examines the evolution of microstructural features in both vertical and horizontal crack orientations by EBSD analysis.

II. Methods

A. Power Cycling Test

Commercially available IGBT modules were utilized in this study. Fig. 1 presents the layout of these modules. Each module contains six subsystems, each consisting of one IGBT and one diode chip. These subsystems are combined to operate as a three-phase full bridge. The PCT was carried out on IGBT chips 2 and 6 for each IGBT module. The die-attach layer between the IGBT chip and direct bonding copper (DBC) substrate is a Sn3.0Ag0.5Cu (SAC305) solder.

For all PCTs, the load current was applied solely to the IGBT chip. The simplified test principle is illustrated in Fig. 2. The circuitry for the three-phase branches of the module was identical. Each phase has two chips connected in series for testing. A 15 V bias voltage was constantly applied to the gate.

The load current for heating the device was switched with the auxiliary switch in each phase. Therefore, the cooling time t_{OFF} in each cycle was set to two times the duration ton for which the load current was applied. A 100 mA measurement current was applied continuously to obtain the junction temperature of the chip using the $V_{\mathrm{CE}}(T)$ method [16].

The temperature swings of the individual cycles were kept at approximately $\Delta T_j \approx 90$ K with $T_{j,\max} \approx 150$ °C. The load current duration was set to 0.2 s, and the cooling time was 0.4 s. Due to the short on-time and relatively high-temperature swing, the power density in the PCTs was also high. Therefore, it is easier to trigger the degradation of the die-attach in the central region. Six IGBT chips in three different IGBT modules were tested in total until the end of life (EoL) to obtain the power cycling lifetime. Afterward, chip 6 in the modules, according to the indication in Fig. 1, was cycled for a lifetime of 25%, 50%, and 75% EoL, respectively.

The gate voltage for all modules in the tests was kept at 15 V, which is higher than the temperature compensation point; the IGBT voltage drop has a positive relationship with temperature. Hence, the occurrence of current crowding during the tests was avoided. To determine $T_{j,\max}$, a 150 μs measurement delay time was set after the load current was switched OFF.

B. Finite Element Simulation

In the fast PCT, the failure emerged at the central area in the solder layer, which is different from the standard horizontal detachment starting at the edge. Therefore, simulating the stress state in the solder layer is necessary for understanding the driving force of the FCN. Thus, after the fast PCT, FE simulations were performed to qualitatively study the temperature and thermo-mechanical stress distribution in the solder layer during the PCT. The defects and time-dependent degradation of the solder layer are not considered in the simulations. In [17] and [18], FE simulations without including the aging failures were also employed to only analyze the temperature and stress state in the solder layer of the power modules. The FE simulations were carried out in COMSOL Multiphysics utilizing the solid mechanics physics interface and heat transfer in solid from the heat transfer module. The viscoplasticity was assigned to the SAC solder domain and all other domains were assigned as linear elastic material. Fig. 3 shows the schematic of the model.

TABLE I
MATERIALS PHYSICAL PROPERTIES

Materials	Density (kg/m^3)	Thermal conductivity (W/mK)	Coefficient of thermal expansion (1/K)	Poisson's ratio	Young's modulus (GPa)
Cu	8960	401	16.5×10^{-6}	0.34	120
Al_2O_3	2700	25	6.4×10^{-6}	0.22	300
Si	2329	130	2.6×10^{-6}	0.28	170
SAC305	7370 [20]	60 [19]	2.2×10^{-5} [20]	0.36 [20]	50 [20]

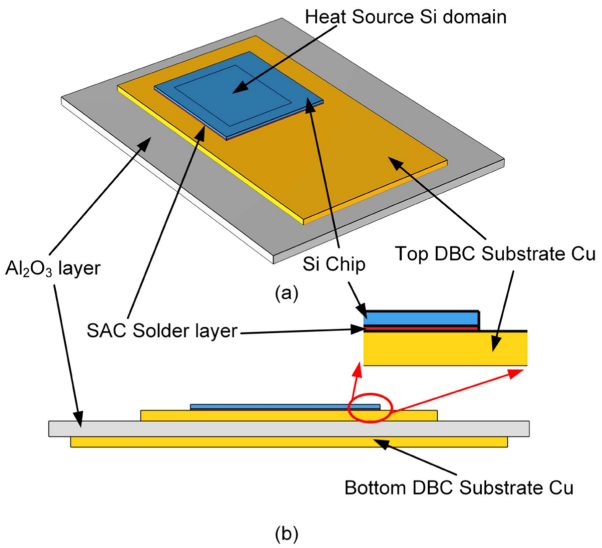


Fig. 3. Schematic of FE model of IGBT module (a) in 3-D, pure Si domain as the heat source, (b) in cross-section, with Si (5.2 mm × 5 mm × 0.114 mm), SAC solder layer (5.2 mm × 5 mm × 0.068 mm), top DBC Cu layer (13 mm × 7.3 mm × 0.26 mm), Al_2O_3 (15 mm × 11.7 mm × 0.38 mm), and bottom DBC Cu layer (14 mm × 10.7 mm × 0.26 mm).

The thickness and dimensions of each layer in the model were consistent with the IGBT modules used in the experiments. During the PCT, the IGBT chip only acts as the heat source. The pure Si domain in the FE model can simulate heat generation, as well as the heat transfer between chip and solder. Thus, the internal structure of the IGBT chip was not considered in this model. In the simulations, it was assumed that the guard rings and the gate pad of the IGBT chip do not generate heat during the PCT. To simulate the heat generation area in the IGBT chip more accurately, a 3 mm × 4 mm Si domain was defined as the heat source. The IGBT chip is also asymmetrical as can be seen from Fig. 1, which implies asymmetrical heat generation. The peripheral Si domain aimed to simulate the gate pad and guard rings of the IGBT chip to incorporate this asymmetry in the model to mimic the actual conditions as closely as possible. The models without the IGBT internal structure have been used to study the thermomechanical stress in IGBT power modules in [19] and [20]. The power dissipation assigned in the heat source was approximately the same as in the PCT. The bottom surface boundary of the DBC substrate was set as 24 °C to simulate the cooling condition in the PCT. Finer mesh elements were assigned to the SAC solder domain, while normal mesh elements were assigned to the other domains.

TABLE II
ANAND PARAMETERS OF SAC305 SOLDER [21]

Parameters	Value
Initial value of deformation resistance (MPa)	45.9
Activation energy/Boltzmann's constant (K)	7460
Pre-exponential factor (1/s)	5.87×10^6
Stress multiplier (dimensionless)	2
Strain rate sensitivity of stress (dimensionless)	0.0942
Hardening constant (MPa)	9350
Deformation resistance saturation coefficient (MPa)	58.3
Deformation resistance sensitivity (dimensionless)	0.015
Hardening sensitivity (dimensionless)	1.5

The material physical parameters for Al_2O_3, Cu, and Si domains were taken as the default values available in the COMSOL library. The parameters for the SAC305 solder domain were gathered from the literature [21], [22]. The material parameters employed are shown in Table I. The viscoplastic Anand model was used in the solder domain to represent the SAC305 solder behavior, and the related Anand's viscoplastic parameters are given in Table II [23].

C. SAM and X-Ray Analysis

After PCT, SAM, and X-ray analyses were performed on the IGBT samples. In SAM, elastic waves focused by an acoustic lens are emitted into the sample, while the transducer is scanned across the sample surface. The contrast mechanism in acoustic analyses is based on the gradients in the mechanical properties of mass density and of the elastic tensor between adjacent materials, which cause alterations in the acoustic impedance and thus lead to reflection and scattering of incident acoustic waves [24]. In a practical sense, acoustic waves are reflected in different materials, with the reflection amplitude increasing with the gradient of the elastic properties across the material boundary. Thus, it is a highly sensitive technique for the detection and localization of delamination, which can be understood as a horizontal crack; however, as a nondestructive technique, the lateral resolution is substantially lower than that of physical techniques that have direct access to the site of inspection. On the other hand, in X-ray imaging, the density variations accompanying cracks can be detected only when the cracks are parallel to the X-ray beam. Consequently, X-ray analysis exhibits high sensitivity toward the detection of cracks that are vertical to the solder plane [14]. Therefore, SAM analysis was employed here to assess the degradation and the presence of defects in the solder layer at the chip–solder and solder–board interfaces. The X-ray

analysis aims to detect the networked vertical cracks at a higher resolution. The results of the two methods are complementary and will, thus, be combined to serve as the basis for subsequent cross-sectional analyses.

The SAM analysis was conducted using a commercial acoustic microscope consisting of a three-axis scanner (PT15-A, ITK Dr. Kassen GmbH, Lahnau, Germany), a pulser receiver (DPR 500, JSR Ultrasonics, New York, NY, USA), and an 1 GS/s, 8Bit AD-Converter (M4i.21xx, Spectrum Instrumentation GmbH, Grosshansdorf, Germany), alongside a Sonoscan Gen6 operating at a frequency of 50 MHz and a focal length of 0.75 in. X-ray was performed in the Nanomex 180 DXR with voltage at 160 kV and current at 100 μA. ImageJ software was utilized for measuring the length of the cracks in the X-ray image.

D. Cross Section and EBSD Analysis

The cross-sectional analysis was conducted subsequent to the nondestructive inspections by SAM and X-ray. The position for preparing the cross-sectional aligned with the results of the SAM and X-ray analyses. Samples representing 25%, 75%, and 100% EoL conditions were prepared by standard metallographic methods and broad ion beam polishing using a JEOL Ion Beam Cryo Cross Section Polisher. Following these preparation steps, all samples were analyzed using a JSM-6330F field emission scanning electron microscope (SEM; JEOL Ltd.) and INCA X-sight energy-dispersive X-ray spectroscopy system (Oxford Instruments).

EBSD analysis was applied to the cross-sectioned samples to study the recrystallization of the β-Sn phase in the solder. The EBSD maps were obtained using a SEM equipped with EBSD (JIB 4700 F). The EBSD maps were scanned with a step size of 0.24 μm and 0.36 μm for 25% EoL and 75% EoL samples, respectively. For the 100% EoL sample, the central part is scanned with 0.38 μm step size and the middle part with 0.75 μm.

III. Results and Discussion

A. Power Cycling Test Results

The trends in ON-state voltage drop V_{CE} and junction to heatsink thermal resistance $R_{\mathrm{th,js}}$ for the EoL test on chip 2 are shown in Fig. 4. The EoL criterion is denoted by either a 5% increase in the forward voltage at the load current, signifying bond wire failure, or a 20% increase in $R_{\mathrm{th,js}}$, revealing solder layer degradation [25]. The V_{CE} curves in Fig. 4 show increasing trend and abrupt drop during the PCT. The increasing trend of the V_{CE} is caused by higher junction temperatures in the power module. During the PCT, thermal grease was attached between the power module and the heatsink for heat spreading. The aging of the thermal grease can also lead to an increase in the V_{CE}, which indicates junction temperature increasing. Therefore, when the increasing trend of V_{CE} was observed, the thermal grease was changed. Once an abrupt drop of the V_{CE} was observed after the renewal of the thermal grease (as shown in Fig. 4), then it can be concluded that the increased V_{CE} is caused by the aged thermal grease instead of bond wires degradation.

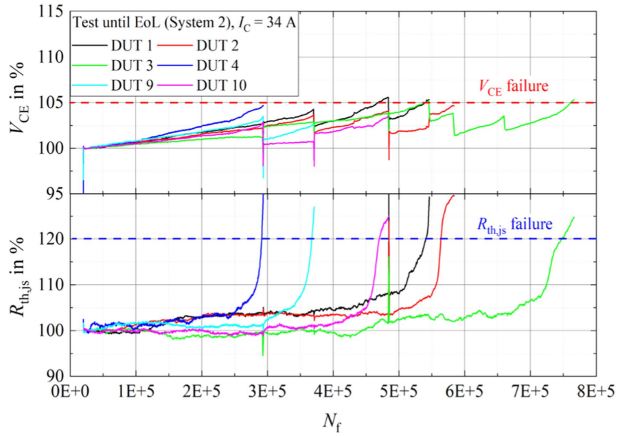


Fig. 4. V_{CE} and $R_{\mathrm{th,js}}$ trends of the EoL power cycling test on chip 2 (DUT represents the IGBT module under testing).

As shown in Fig. 4, all IGBT modules failed due to die-attach degradation causing an increase in $R_{\mathrm{th,js}}$. The load current of the power cycling was 34 A, which was 136% of the rated current. This higher current density is intended to induce the aging of the bond wires. Nevertheless, solder layer degradation is expected to be the dominant failure mode, a conclusion further supported by subsequent failure analysis.

There are 6 IGBT modules tested, one chip in each module was aged to 100% EoL in total. The average lifetime was calculated based on the 6 chips. The average value is about 480 k cycles and is considered as 100% lifetime. Then, the 25% and 75% EoL cycles were based on the average lifetime cycles, which means the 120 k cycles were applied to 25% EoL chips and 360 k cycles to 75% EoL chips. Afterward, modules 1 and 2 and modules 3 and 4 were aged to 25% and 50% EoL, respectively. Modules 9 and 10 were aged to 75% EoL. All different EoL percentage tests were performed on chip 6.

B. Nondestructive Inspection Results

This section compares the results of nondestructive inspection (SAM and X-ray imaging) of different EoL percentage samples. The differences between the observations of the two methods are discussed.

Fig. 5 illustrates the simplified IGBT structure, direction, and amplitude of the SAM signal and the nondestructive inspection results of different EoL percentage samples. The direction and route of SAM scanning are shown in Fig. 5(a). Fig. 5(b) shows the amplitude of the SAM signal and its corresponding interfaces. Based on the amplitude of the signal, the target of the SAM was determined with three different depths: the DBC–solder interface, the entire solder layer, and the solder–Si chip interface.

The SAM results illustrate the defects with bright spots and reveal clear distinctions in the central regions of the three depths. In the 25% EoL sample, the defects in the center of the DBC–solder interface [see Fig. 5(c)] and the entire solder layer [see Fig. 5(d)] are less clear than those in the solder–Si chip interface [see Fig. 5(e)], as marked in the red box in the image. Therefore, the defects can be located in the solder–Si

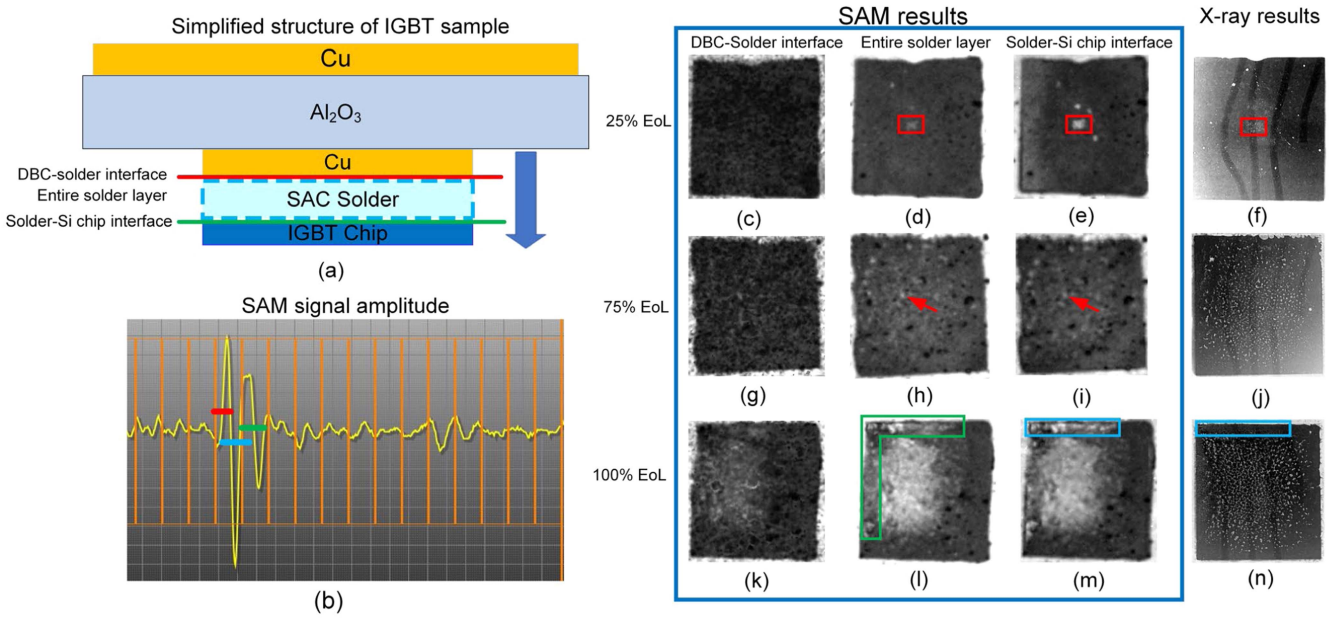


Fig. 5. Nondestructive inspections. (a) Simplified IGBT structure and (b) SAM signal amplitude; SAM and X-ray results of Module2Chip6 (M2C6) 25% EoL: (c) DBC–solder interface, (d) entire solder layer, (e) solder–Si chip interface, and (f) X-ray; (g)–(j) M10C6 75% EoL; (k)–(n) M10C2 100% EoL.

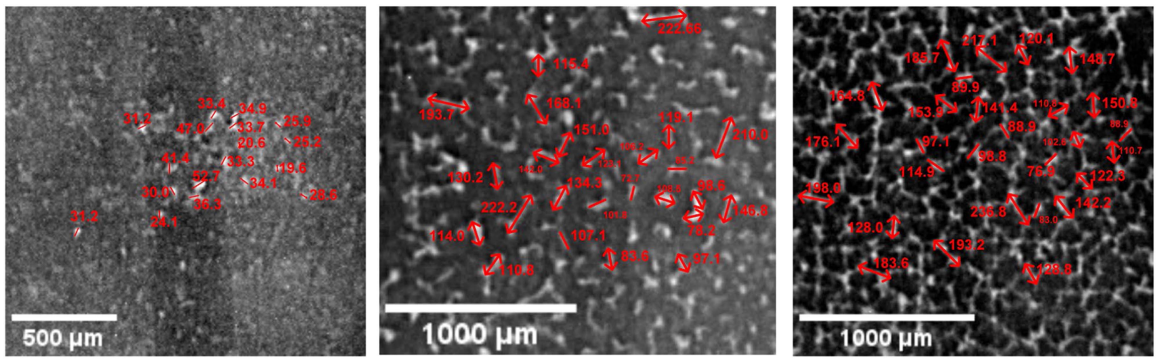


Fig. 6. Higher magnification of the central area of X-ray results and measurement of crack length: (a) 25% EoL, (b) 75% EoL, and (c) 100% EoL.

chip interface. Compared to the 25% EoL sample, an increased number of defects are evident at the solder–Si chip interface [see Fig. 5(i)] in the 75% EoL sample. Notably, when examining the solder–Si chip interface [see Fig. 5(i)] in contrast to Fig. 5(h), distinctive differences are observable in the positioning of bright spots. One of these differences is specifically highlighted by red arrows. The observed differences indicate that defects do not solely emerge at the solder–Si chip interface. There is a growing number of voids across the entire solder layer. The SAM results from the 100% EoL sample shown in Fig. 5(l) and (m) highlight the large horizontal fatigue cracks propagating in the bright area.

Fig. 6 shows a higher magnification of the central region within the X-ray imaging results for the 25%, 75%, and 100% EoL samples. In the 25% EoL sample, only a few cracks emerged at the center. With more power cycles applied to the IGBT module, the X-ray imaging result of the 75% EoL sample revealed a greater quantity of cracks and an increase in their length. However, most of the cracks remained unconnected. In the case of the 100% EoL samples, the cracks continued to extend, and a large number of them started to connect, forming a typical crack network, as shown in Fig. 6(c).

As shown in Fig. 6(a), the average length of the cracks in the 25% EoL sample was 32.4 ± 8.5 μm. In the 75% EoL sample, the average value increased to 129.7 ± 43.5 μm, and even >220 μm long cracks were measured. When the sample reached 100% EoL, the average value increased slightly due to the emergence of small new cracks. However, most cracks exceeded 150 μm, and the maximum value, as shown in Fig. 6(c), was 236.8 μm.

The comparison between the SAM and X-ray imaging results can provide a more comprehensive understanding of solder layer failure. In the 25% EoL sample, the SAM image shows clear defects in the center of the solder layer, but the X-ray imaging only detects small cracks in the same area, as marked in the red box in Fig. 5(e) and (f). The crack networks and large area defects

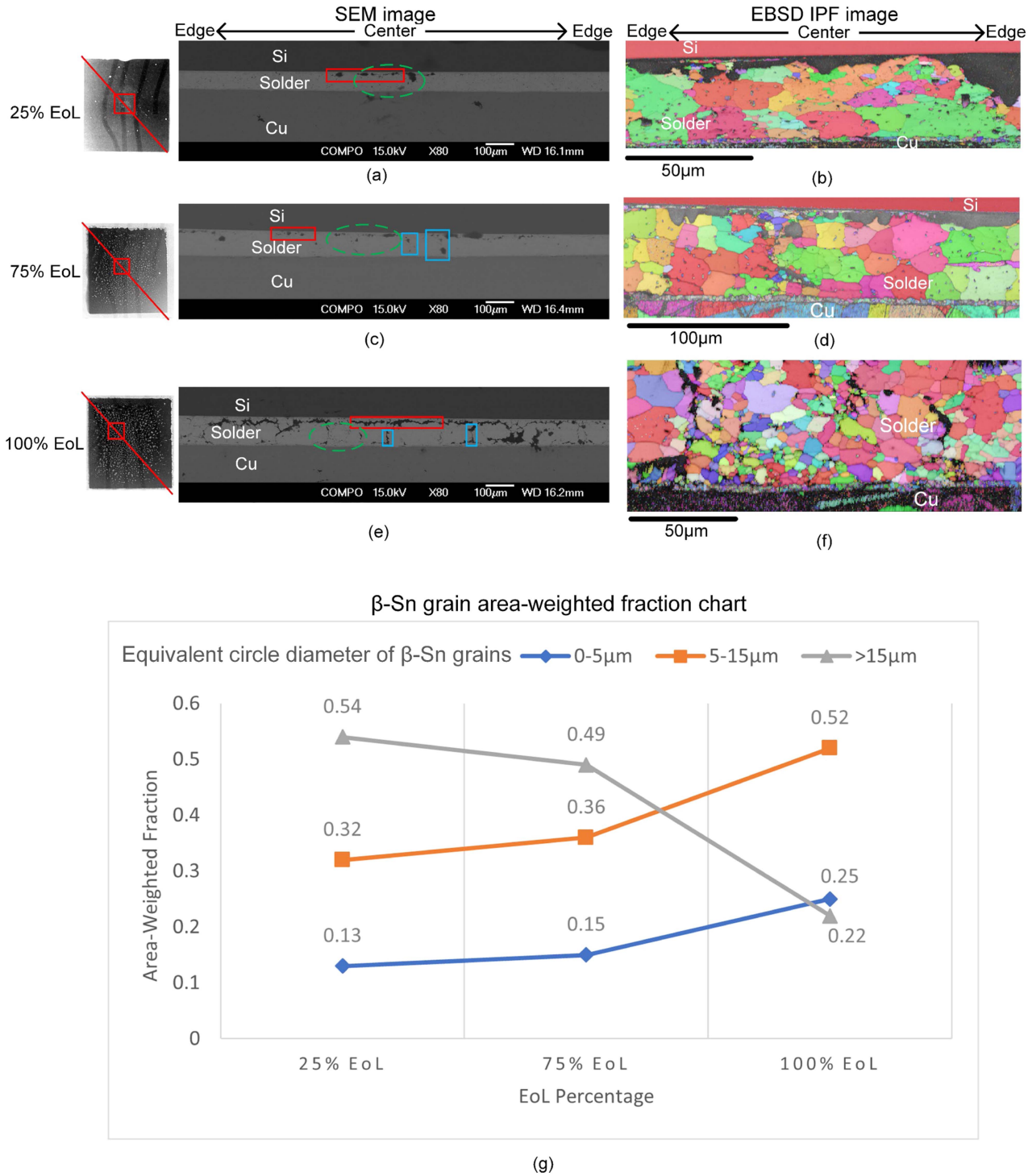


Fig. 7. Cross-section and EBSD inverse pole figure (IPF) maps of the 25% EoL sample. (a) Cross-sectional BSE-SEM image and (b) IPF map. (c) and (d) 75% EoL. (e) and (f) 100% EoL; (g) β-Sn grain area-weighted fraction chart.

in the X-ray imaging and SAM results of the 100% EoL sample indicate the possible existence of both vertical and horizontal cracks in the center of the solder layer.

In the 100% EoL sample, the edge of the solder layer near the top left corner in X-ray imaging [see Fig. 5(n)] is nearly identical to the intact area. However, in the SAM result [see Fig. 5(m)], some defects are detected in this area, as marked in the blue boxes. The difference indicates that the edge of the solder layer only has horizontal detachment.

In conclusion, SAM was able to locate voids in 25% and 75% EoL samples. In the 100% EoL sample, SAM can detect two types of failure: detachment at the edge and large defects in the center area. X-ray imaging results can only show crack network formation when the EoL percentage increases from a lower to

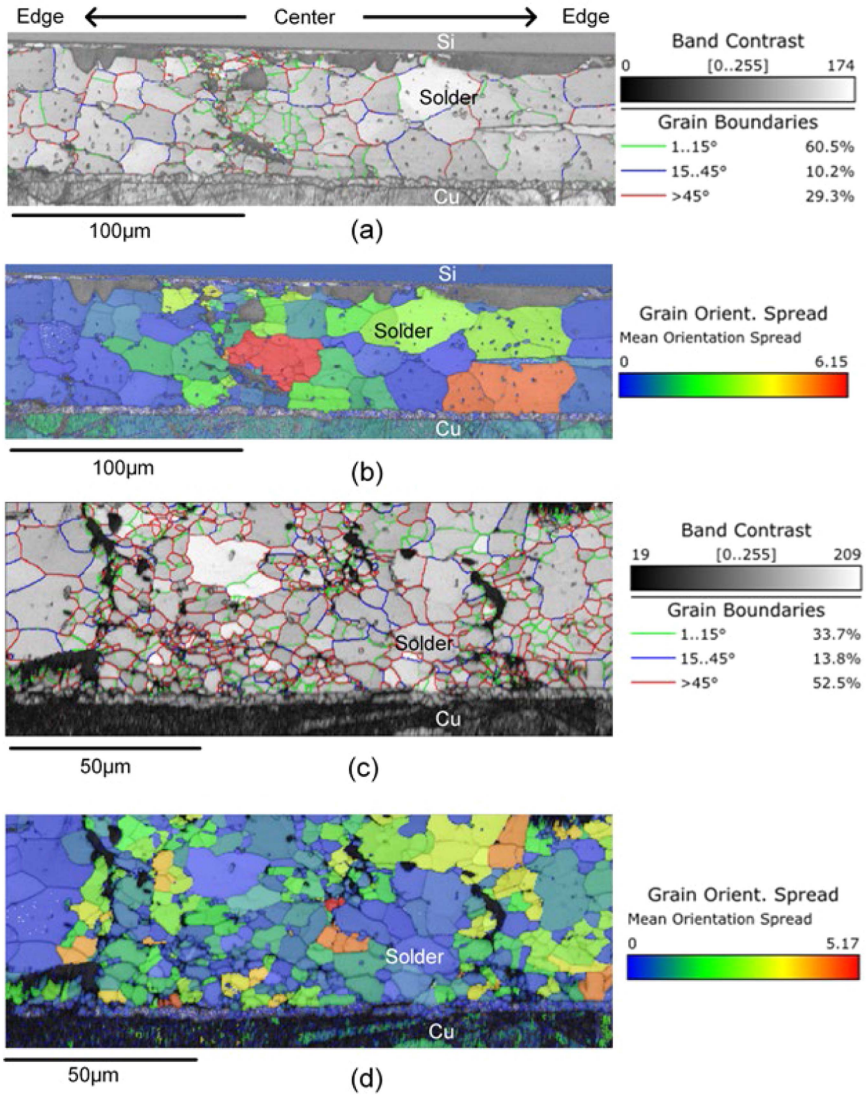


Fig. 8. GBA map and GOS map of (a) and (b) 75% EoL and (c) and (d) 100% EoL.

a higher value. To obtain more detailed information on solder layer failure, a combination of these two methods is required.

C. Destructive Inspection and Microstructural Analysis Results

Based on the SAM and X-ray imaging results, to observe the horizontal detachment and more vertical cracks in the cross-sectional analysis, the cross-sectional position was determined from the top left to the bottom right corner of the solder layer, as marked with the red line in the small X-ray image in Fig. 7. Fig. 7 presents the cross-sectional BSE-SEM and EBSD analysis results of different EoL percentage samples. The cross-sectional image is from the center area, marked as the red box in the small X-ray image in Fig. 7.

Fig. 7(a) shows the BSE-SEM image of the 25% EoL sample, with voids located at the solder–Si chip interface. In the 75% EoL sample, as shown in Fig. 7(c), most of the voids were observed to be located close to the Si chip, and some voids' size increased in the vertical direction compared to the 25% EoL sample, which is reflected in the X-ray imaging. As demonstrated in Fig. 7(e), two different types of cracks can be found in the 100% EoL sample. The voids and cracks found in the cross-sectional analysis confirm the difference between the X-ray imaging and SAM results discussed in Section III-B.

The EBSD analysis in this study focused primarily on the voids and cracks at the center of the solder layer. The occurrence of cracks has been related to the recrystallization of the β-Sn phase [26]. Cracks or voids typically occur in the high-strain region of β-Sn, coinciding with the recrystallization process and the formation of smaller grains [27]. The main microstructure features include grain size, grain crystallographic orientation, and grain boundary misorientation.

Fig. 7(b), (d), and (f) shows the inverse pole figure (IPF) maps of different EoL percentage samples. The IPF maps correspond to the delineated green dashed regions, as indicated within the SEM images. The color variations in the IPF maps correspond to a unique crystal orientation and delineate the boundaries

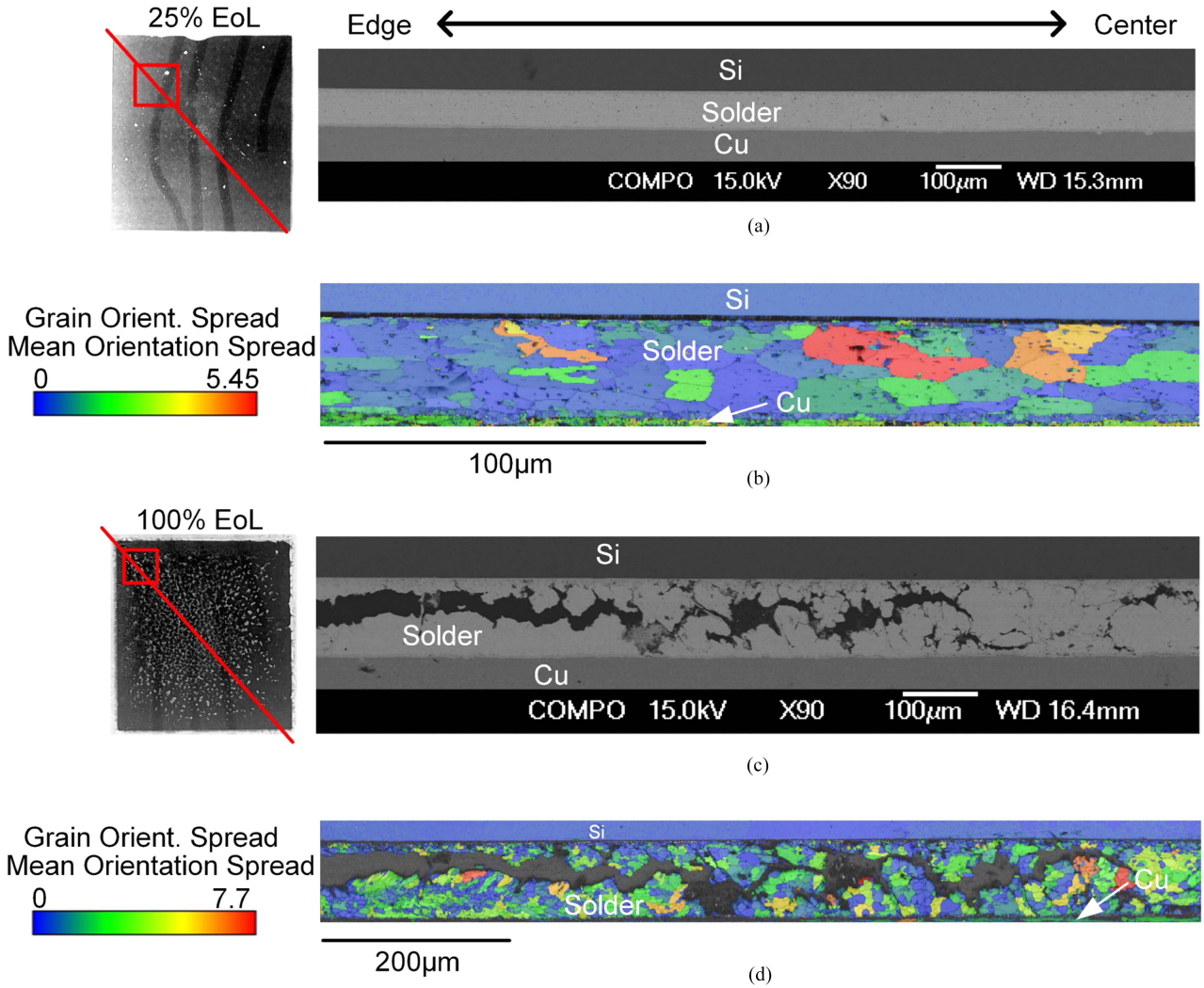


Fig. 9. Cross-sectional figure and EBSD GOS map of the solder between center and edge in (a), (b) 25% EoL and (c), (d) 100% EoL.

between different grains. The grain orientation reflects the rotation of the grains during the recrystallization. As evident from the IPF maps, the 25% EoL sample exhibits less misorientation and larger grain size. The misorientation increases and the average grain size decreases with a higher EoL percentage. The changes in β-Sn grain size and misorientation illustrate the recrystallization that occurs during the power cycling. In each sample, there are smaller grains near the voids and cracks. During crack propagation, a high-stress concentration at the crack tip can trigger localized recrystallization and then lead to small β-Sn grain generation. In order to demonstrate the grain size variation in different samples directly, Fig. 7(g) shows the grain area-weighted fraction curves. The equivalent circle diameter serves as a metric to represent the size of individual grains by approximating their irregular shapes to circles of the equivalent area [28]. There is an increase in the fraction of smaller grains with higher EoL percentage, especially in grain diameters under 5 μm and 5–15 μm. In the 25% and 75% EoL samples, there are large fractions of bigger-size grains with diameters exceeding 15 μm. The fraction is 0.54 and 0.49 in the 25% and 75% EoL samples, respectively, while it decreases to 0.22 in the 100% EoL sample.

Fig. 8 shows the grain boundary angle (GBA) and grain orientation spread (GOS) maps of the 75% and 100% EoL samples. In Fig. 8(a) and (c), the GBAs lower than 15° are demonstrated in green color. The high-angle boundaries (higher than 45°) are marked with red color. In both samples, most of the high-angle boundaries are close to the voids and cracks. The high-angle grain boundaries indicate more recrystallization close to voids and cracks. The GOS maps represent the average misorientation of all pixels in a grain relative to the grain's average orientation [29]. A higher GOS value corresponds to high strain inside the grain [30]. In Fig. 8(b) and (d), the grains close to the cracks and voids have more deformations and higher strains.

In Fig. 8(a), low-angle boundaries (lower than 15°) are also detected near the vertical connection voids. The low-angle boundaries close to cracks are caused by the β-Sn subgrains [27]. β-Sn subgrains are generated in the initial stage of the recrystallization, which has a low GBA [31]. This feature

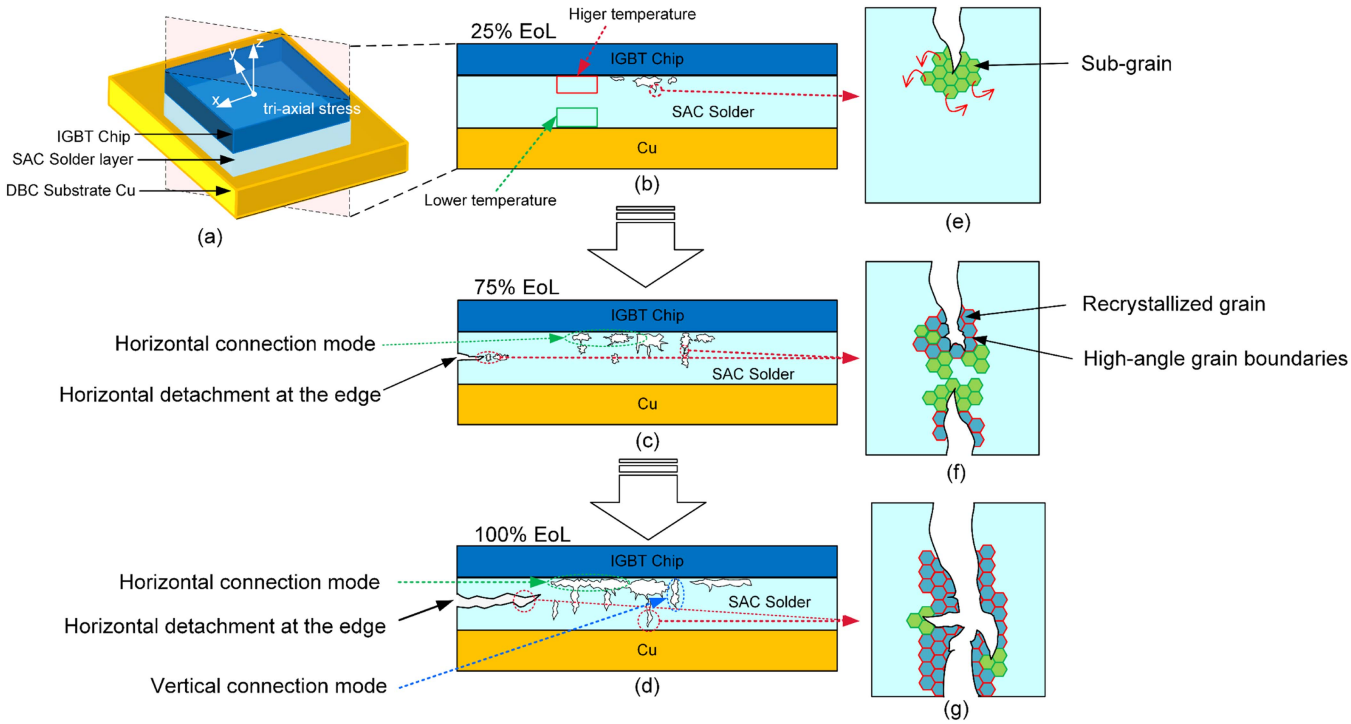


Fig. 10. Schematic diagram of failure formation and microstructure evolution: (a) compounded stresses state in solder layer, (b)–(d) voids connection modes and cracks formation, (e)–(g) microstructure evolution of β-Sn phase.

means that the voids and cracks keep growing in the 75% EoL sample.

Due to the presence of horizontal detachment, analyzing the microstructure evolution of the solder between the center and the edge is crucial for a comprehensive understanding of the failure mechanism of the entire solder layer.

Fig. 9 shows the cross section and EBSD results of the solder between the center and edge in different EoL percentage samples. Fig. 9(c) demonstrates the typical CTE horizontal detachment that emerged at the edge of the sample, which is also detected by SAM, as shown in Fig. 5(m) in Section III-B. As discussed in [32], shear stress caused by the mismatch of the different materials during power cycling is the reason for this detachment at the edge.

Fig. 9(b) and (d) demonstrates the GOS maps of the two samples. In the 100% EoL sample, the number of small-size grains increases, along with more grains that have higher misorientation angles, particularly close to the detachment and crack propagation paths. The grain size and misorientation both indicate that there is more recrystallization in the 100% EoL sample. Thus, the microstructure evolution of the horizontal detachment at the edge of the solder layer is similar to vertical cracks.

In order to combine the experimental results and summarize the failure mechanism, Fig. 10 illustrates a schematic diagram of the failure formation mechanism. As depicted in Fig. 10(a), power cycling generates biaxial (x- and y-directions, parallel to the solder layer) tensile and compressive stress in the central region of the solder layer [13]. Based on the EBSD analysis, the xy-direction stress first generates the β-Sn subgrains, and the rotation of these subgrains leads to the formation of high-angle grain boundaries, resulting in recrystallized grains [33], as shown in Fig. 10(e) and (f). Voids and cracks are more prone to emerge and propagate at the high-angle grain boundaries. As shown in Fig. 10(b), small voids first form in the center area close to the solder–Si chip interface. The voids are initially detected by SAM and confirmed with cross-sectional analysis in the 25% EoL sample. The recrystallization continues with more power cycles applied to the IGBT module, reflected in the reduction of grain size. With higher angle grain boundaries created, the volume of voids increases. New voids emerge both at the solder–Si chip interface and in the solder layer. The voids in the solder layer connect to form vertical cracks, and those close to the interface connect horizontally, as depicted in Fig. 10(c) and (d). In the 75%EoL sample, a large number of vertical connections are detected in the center of the solder, and the X-ray imaging result [see Fig. 5(j)] shows that the vertical cracks already exist in a larger area in the solder layer. The obvious horizontal connections and edge horizontal detachment are only found in 100%EoL samples. Thus, the vertical connections mode is the dominant factor of the main formation process of the FCN. The clues to the two connection modes in the cross-sectional results are demonstrated in Fig. 7(a), (c), and (e). The horizontal and vertical connection modes are marked as red and blue boxes, respectively. After the power cycles reach 100% lifetime, the connections of the voids form large vertical and horizontal cracks in the center of the solder layer. The vertical cracks connect and are detected by X-ray imaging as the FCN. The horizontal cracks appear as bright areas in the SAM results.

In both the standard and fast PCT, the center of the IGBT chip has a higher temperature [7], [34]. The FE simulation in

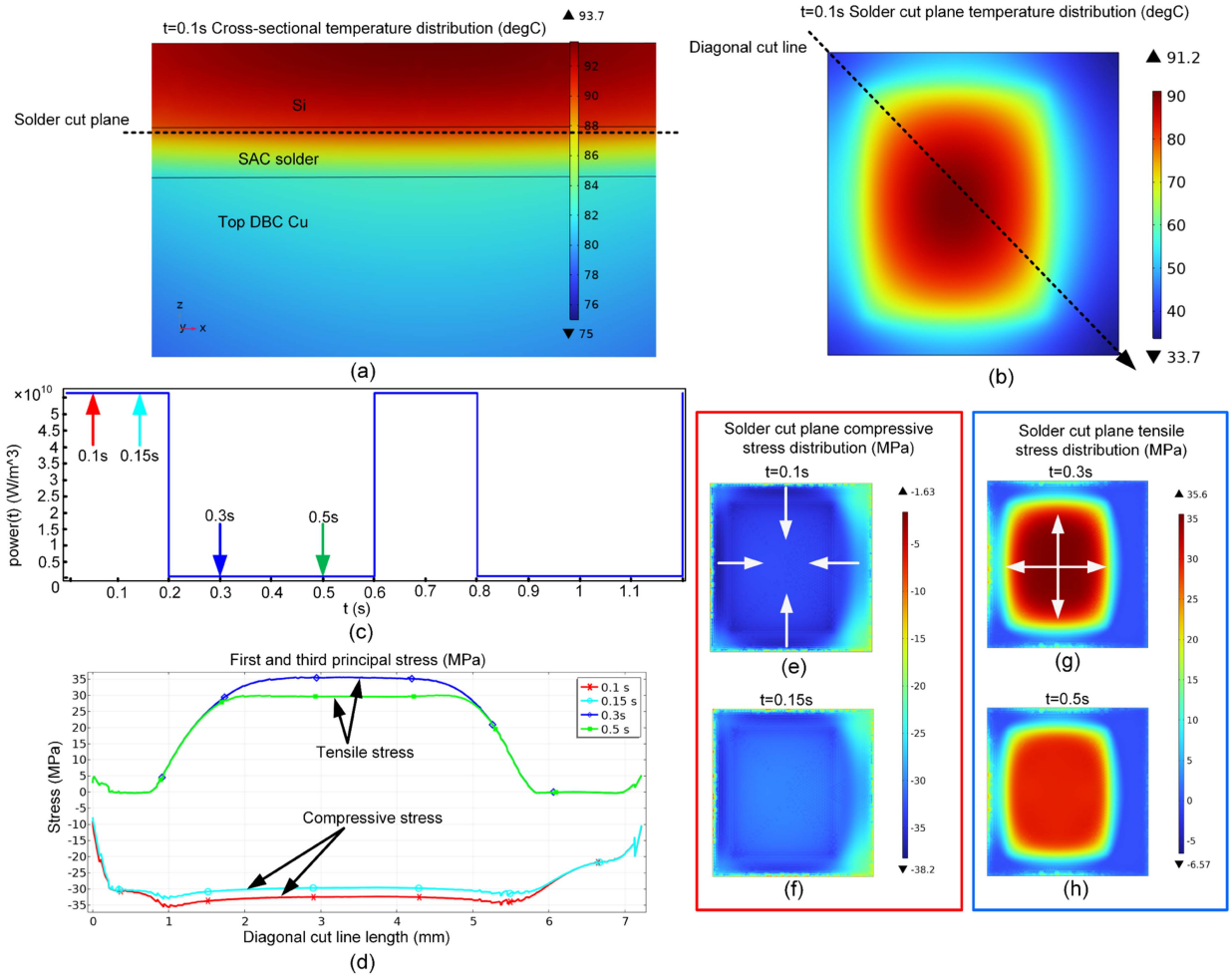


Fig. 11. Simulation results of temperature and stress distribution in the solder layer. (a) Cross-sectional temperature distribution, in diagonal cut line. (b) Solder cut plane temperature distribution, 2 μm below the solder-Si interface. (c) Power cycle curve. (d) Solder diagonal cut line stress curve. (e)–(h) Solder cut plane stress distributions, 2 μm below the solder-Si interface, white arrows as the stress direction.

this study shows the same results. Fig. 11 shows the temperature and stress distribution of the IGBT module. Fig. 11(a) demonstrates the cross-sectional temperature distribution. The cut plane marked with the dashed line in Fig. 11(a) was 2 μm below the solder-Si interface, where the initial formation of voids was detected [as shown in Fig. 7(a)]. All the temperatures [see Fig. 11(b)] and stress distribution [see Fig. 11(e)–(h)] were extracted from this cut plane. Fig. 11(b) shows the cut plane temperature distribution and the diagonal cut line was marked with the arrow. The power cycle plot is demonstrated in Fig. 11(c). Fig. 11(d) shows the compressive and tensile stress curves of the diagonal cut line in one power cycle. The time of each stress curve are marked in the Fig. 11(c). The related solder cut plane stress distributions are shown in Fig. 11(e)–(h).

The heat spreads from the IGBT chip to the solder layer, creating a temperature gradient in the z-direction. In Fig. 11(b), the top surface (close to the Si chip) of the solder layer has a higher temperature than the bottom surface (close to the DBC substrate). In SAC solder the temperature gradient is approximately 966.85 °C/cm [35], which results in a 5–6 °C temperature change from top to bottom surface of the solder layer. A higher temperature results in increased biaxial (xy-direction) stress. Therefore, with a longer power cycling time, the higher biaxial stress generates a greater number of voids at the center of the solder–Si chip interface. Furthermore, the coefficient of thermal expansion (CTE) mismatch and the nonuniform temperature distribution may also lead to shear stress at the solder–Si chip interface. The voids connect horizontally under these compounded stresses. In Fig. 10(b), the green box-marked area in the solder layer has a lower temperature and less stress than the solder–Si chip interface. In this region, the biaxial stress expands the voids in the vertical direction.

In the IGBT module used in this study, the heat generation position deviates from the geometric center of the IGBT chip, and the layout of the top Cu layer on the DBC substrate is asymmetric, resulting in asymmetric temperature distribution in the x- and y-directions, as shown in Fig. 11(a). This leads to unequal biaxial stress that is different from the equal biaxial stress discussed in [13]. In Fig. 11(d), the compressive and tensile stress formed in the current-ON and current-OFF stage, respectively. The stress curves are not symmetrical to the middle point of the diagonal cut line. In the solder cut plan stress

distribution [see Fig. 11(e)–(h)], the higher stresses were concentrated in the left part of the solder shown in the figure. Therefore, vertical cracks are expected to form when unequal biaxial stress is applied. The stress directions are marked in Fig. 11(e) and (g) with white arrows. The biaxial stress indicates that both the compressive and tensile stresses are in the *x*- and *y*-directions.

In Fig. 5(n), there are more vertical cracks appearing at the upper left corner of the solder in the 100% EoL sample. The horizontal detachment is only appearing at the upper and the left edge of the solder layer, as shown in Fig. 5(l) marked with a green box. The asymmetric transient temperature and stress distribution, as shown in the simulation results, is also the driving force for these phenomena.

In the middle part between the center and edge of the solder layer, recrystallization also proceeded due to the applied stress. When the sample reaches 75% EoL, some voids are generated at the high-angle grain boundaries in this part. After more power cycles are applied to the IGBT module, a large amount of recrystallized β-Sn grains and high-angle boundaries are generated. Higher shear stress from the CTE mismatch concentrated at the edge [36] is easier to cause failure in this part, which leads to the large detachment in the 100% EoL sample.

In summary, the formation mechanism of the FCN is similar to that of the traditional detachment failure in the β-Sn phase microstructure evolution. Then, the different directions of the stress lead to different crack types and finally cause the FCN at the center and horizontal detachment at the edge.

IV. Conclusion

In this work, the SAM and X-ray methods were utilized in nondestructive inspections. It provides essential insights into the failure mechanism of the solder layer. The conclusions drawn from nondestructive inspections can be summarized as follows.

1) The power cycling test initially generated voids at the solder–Si chip interface in the center area.
2) The voids and cracks require sufficient vertical length to be detected by X-ray, while SAM results can clearly reveal horizontal cracks. With an increasing volume of voids, X-ray results exhibit a typical FCN.
3) Both X-ray and SAM are necessary to accurately determine the actual failure information of the solder layer. Besides the FCN in the X-ray results, SAM can depict horizontal cracks at the edge, especially in the 100% EoL sample.

Destructive inspections have confirmed the propagation and microstructure evolution of the FCN. Two connection types of voids are identified in the center. The voids that are close to the solder–Si interface connected horizontally, while the voids in the solder layer make vertical connections more likely. Based on the FE simulation results, the driving force of the vertical cracks is the unequal biaxial stresses generated in each cycle. Furthermore, recrystallization occurred during the PCT. Voids and cracks emerged at the high-angle grain boundary area. Then, in both the center area and middle part of the solder, the grain size decreased with more power cycles applied. The microstructure evolution of the β-Sn phase is consistent in both vertical cracks and horizontal detachment.

With the widespread application of high-frequency power devices, this study may inspire the design of fast PCT. Moreover, for the lifetime models considering t_{ON} as a variable, including the FCN as an additional variable may improve the optimization of the model when t_{ON} decreases significantly. An FE simulation including the solder layer degradation mechanism needs to be developed, as such a model can significantly contribute to establishing the new lifetime model. Due to the horizontal detachment failure mode was also observed at the edge of the sample. More research on which failure mechanism is the dominant factor of the IGBT modules' lifetime needs to be done in the future.

References

[1] R. Islam, S. M. S. H. Rafin, and O. A. Mohammed, "Comprehensive review of power electronic converters in electric vehicle applications," *Forecasting*, vol. 5, no. 1, pp. 22–80, 2022, doi: 10.3390/forecast5010002.

[2] B. N. C. V. Chakravarthi and G. V. S. K. Rao, "Impact of power quality issues in grid connected photovoltaic system," in *Proc. 4th Int. Conf. Electron., Commun. Aerosp. Technol.*, Nov. 2020, pp. 155–158, doi: 10.1109/ICECA49313.2020.9297618.

[3] A. Foote and O. C. Onar, "A review of high-power wireless power transfer," in *Proc. IEEE Transp. Electrific. Conf. Expo*, Jun. 2017, pp. 234–240, doi: 10.1109/ITEC.2017.7993277.

[4] I. Husain et al., "Electric drive technology trends, challenges, and opportunities for future electric vehicles," *Proc. IEEE*, vol. 109, no. 6, pp. 1039–1059, Jun. 2021, doi: 10.1109/JPROC.2020.3046112.

[5] X. Yang, Y. Zhang, X. Wu, and G. Liu, "Failure mode classification of IGBT modules under power cycling tests based on data-driven machine learning framework," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 16130–16141, Dec. 2023, doi: 10.1109/tpel.2023.3314738.

[6] U.-M. Choi, S. Jørgensen, and F. Blaabjerg, "Advanced accelerated power cycling test for reliability investigation of power device modules," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8371–8386, Dec. 2016, doi: 10.1109/TPEL.2016.2521899.

[7] C. Schwabe, N. Thönelt, J. Lutz, and T. Basler, "High cycle fatigue testing of silicon IGBT devices under application-close conditions," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 14516–14525, Nov. 2023, doi: 10.1109/tpel.2023.3296269.

[8] B. Ji, X. Song, E. Sciberras, W. Cao, Y. Hu, and V. Pickert, "Multiobjective design optimization of IGBT power modules considering power cycling and thermal cycling," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2493–2504, May 2015, doi: 10.1109/tpel.2014.2365531.

[9] M. Junghaenel and U. Scheuermann, "Impact of load pulse duration on power cycling lifetime of chip interconnection solder joints," *Microelectronics Rel.*, vol. 76/77, pp. 480–484, 2017, doi: 10.1016/j.microrel.2017.06.081.

[10] H. Sugimoto, Y. Kariya, R. Hanada, A. Fukumoto, Y. Ito, and S. Soda, "Fracture analysis of vertical direction crack in die attach joint for power semiconductor device," in *Proc. 6th Int. Workshop Low Temp. Bonding 3-D Integration*, May 2019, pp. 82–82, doi: 10.23919/LTB-3D.2019.8735334.

[11] H. Sugimoto, Y. Kariya, Y. Abe, R. Hanada, Y. Yokoyama, and S. Soda, "Formation mechanisms of thermal fatigue crack networks in Sn-Ag-Cu die-attach joint in high speed thermal cycling," *J. Smart Process.*, vol. 9, no. 5, pp. 224–231, 2020, doi: 10.7791/jspmee.9.224.

[12] J. Dai, J. Li, P. Agyakwa, M. Corfield, and C. M. Johnson, "Comparative thermal and structural characterization of sintered nano-silver and high-lead solder die attachments during power cycling," *IEEE Trans. Device Mater. Rel.*, vol. 18, no. 2, pp. 256–265, Jun. 2018, doi: 10.1109/tdmr.2018.2825386.

[13] K. Hosoya, Y. Kariya, H. Sugimoto, and K. Takahashi, "Fatigue crack networks in the die-attach joint of a power semiconductor module during power cycling testing and effects of test parameters on the joint fatigue life," *J. Electron. Mater.*, vol. 49, no. 10, pp. 6175–6186, 2020, doi: 10.1007/s11664-020-08381-7.

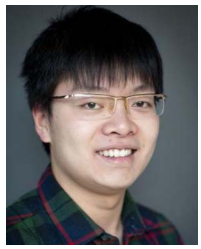
[14] S. Hartmann, M. Bayer, D. Schneider, and L. Feller, "Observation of chip solder degradation by electrical measurements during power cycling," in *Proc. 6th Int. Conf. Integr. Power Electron. Syst.*, Mar. 2010, pp. 1–6.
[15] B. Hu, S. Konaklieva, N. Kourra, M. A. Williams, L. Ran, and W. Lai, "Long-term reliability evaluation of power modules with low amplitude thermomechanical stresses and initial defects," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 602–615, Feb. 2021, doi: 10.1109/jestpe.2019.2958737.
[16] J. Chen, E. Deng, L. Xie, X. Ying, and Y. Huang, "Investigations on averaging mechanisms of virtual junction temperature determined by $V_{CE\ (T)}$ method for IGBTs," *IEEE Trans. Electron Devices*, vol. 67, no. 3, pp. 1106–1112, Mar. 2020, doi: 10.1109/ted.2020.2969727.
[17] C. Durand, M. Klingler, M. Bigerelle, and D. Coutellier, "Solder fatigue failures in a new designed power module under power cycling," *Microelectronics Rel.*, vol. 66, pp. 122–133, 2016, doi: 10.1016/j.microrel.2016.10.002.
[18] J. Sunil, S. Aslam, S. Perinpanyagam, and A. Wileman, "Finite element analysis of Si and SiC power modules for accurate reliability assessment," in *Proc. IEEE Aerosp. Conf.*, Mar. 2022, pp. 1–10, doi: 10.1109/AERO53065.2022.9843461.
[19] Z. Khatir and S. Lefebvre, "Boundary element analysis of thermal fatigue effects on high power IGBT modules," *Microelectronics Rel.*, vol. 44, no. 6, pp. 929–938, 2004, doi: 10.1016/j.microrel.2004.02.007.
[20] C. Zhan et al., "A fully coupled model of multi-chip press-pack IGBT for thermo-mechanical stress distribution prediction," *IEEE Trans. Ind. Appl.*, vol. 58, no. 3, pp. 3852–3862, May/Jun. 2022, doi: 10.1109/tia.2022.3160412.
[21] G. Petrone, C. Barbagallo, and M. Scionti, "Thermo-mechanical analysis and fatigue life prediction for an electronic surface-mount device (SMD)," in *Proc. COMSOL Conf.*, Grenoble, Catania, Italy, 2015, pp. 1–7.
[22] G. Chen et al., "Transient thermal performance of IGBT power modules attached by low-temperature sintered nanosilver," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 1, pp. 124–132, Mar. 2012, doi: 10.1109/tdmr.2011.2173573.
[23] J. Chang, L. Wang, J. Dirk, and X. Xie, "Finite element modeling predicts the effects of voids on thermal shock reliability and thermal resistance of power device," *Weld. J.*, vol. 85, no. 3, pp. 63s–70s, 2006.
[24] A. Briggs and O. Kolosov, *Acoustic Microscopy*. Oxford, U.K.: Oxford Univ. Press, 2009.
[25] *Semiconductor Devices Mechanical and Climatic Test Methods Part 34: Power Cycling*, Standard IEC 60749-34, International Electro technical Commission, 2004.
[26] E. Ben Romdhane, P. Roumanille, A. Guédon-Gracia, S. Pin, P. Nguyen, and H. Frémont, "From early microstructural evolution to intergranular crack propagation in SAC solders under thermomechanical fatigue," *Microelectronics Rel.*, vol. 126, 2021, Art. no. 114288, doi: 10.1016/j.microrel.2021.114288.
[27] J. B. Libot, J. Alexis, O. Dalverny, L. Arnaud, P. Milesi, and F. Dulondel, "Microstructural evolutions of Sn-3.0Ag-0.5Cu solder joints during thermal cycling," *Microelectronics Rel.*, vol. 83, pp. 64–76, 2018, doi: 10.1016/j.microrel.2018.02.009.
[28] A. A. Gazder, W. Cao, C. H. J. Davies, and E. V. Pereloma, "An EBSD investigation of interstitial-free steel subjected to equal channel angular extrusion," *Mater. Sci. Eng., A*, vol. 497, no. 1/2, pp. 341–352, 2008, doi: 10.1016/j.msea.2008.07.030.
[29] H. Fekiri, V. A. Esin, V. Maurel, A. Köster, and Y. Bienvenu, "Microstructure evolution of innovative thermal bridge composite (i-TBC) for power electronics during elaboration," *Mater. Des.*, vol. 137, pp. 68–78, 2018, doi: 10.1016/j.matdes.2017.10.009.
[30] N. Mookam and K. Kanlayasiri, "Effects of substrate annealing on wettability and intermetallic compound formation in Sn–3.0Cu/Cu systems," *J. Mater. Sci., Mater. Electron.*, vol. 30, no. 13, pp. 12087–12099, 2019, doi: 10.1007/s10854-019-01566-9.
[31] E. Ben Romdhane, P. Roumanille, A. Guedon-Gracia, S. Pin, P. Nguyen, and H. Fremont, "Early microstructural indicators of crack initiation in lead-free solder joints under thermal cycling," in *Proc. IEEE 71st Electron. Compon. Technol. Conf.*, 2021, pp. 2293–2301.
[32] A. Morozumi, K. Yamada, T. Miyasaka, S. Sumi, and Y. Seki, "Reliability of power cycling for igbt power semiconductor modules," *IEEE Trans. Ind. Appl.*, vol. 39, no. 3, pp. 665–671, May/Jun. 2003, doi: 10.1109/tia.2003.810661.
[33] H. Chen, J. Han, and M. Li, "Localized recrystallization induced by subgrain rotation in Sn-3.0Ag-0.5Cu ball grid array solder interconnects during thermal cycling," *J. Electron. Mater.*, vol. 40, no. 12, pp. 2470–2479, 2011, doi: 10.1007/s11664-011-1782-y.
[34] J. Lutz, T. Herrmann, M. Feller, R. Bayerer, T. Licht, and R. Amro, "Power cycling induced failure mechanisms in the viewpoint of rough temperature environment," in *Proc. 5th Int. Conf. Integr. Power Electron. Syst.*, Mar. 2008, pp. 1–4.
[35] G. Chen, L. Liu, V. V. Silberschmidt, C. Liu, F. Wu, and Y. C. Chan, "Microstructural evolution of 96.5Sn–3Ag–0.5Cu lead free solder reinforced with nickel-coated graphene reinforcements under large temperature gradient," *J. Mater. Sci., Mater. Electron.*, vol. 29, no. 7, pp. 5253–5263, 2018, doi: 10.1007/s10854-017-8489-7.
[36] E. R, G. Kavithaa, V. Samavatian, K. Alhaifi, A. Kokabi, and H. Moayedi, "Reliability enhancement of a power semiconductor with optimized solder layer thickness," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6397–6404, Jun. 2020, doi: 10.1109/tpel.2019.2951815.

Shenyi Liu received the B.S. degree in electrical engineering from Hebei University of Science and Technology, Shijiazhuang, China, in 2018, and the M.Eng. degree in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2020. He is currently working toward the D.Sc. degree in electrical engineering from the Electronics Integration and Reliability Group, Department of Electrical Engineering and Automation, Aalto University, Espoo, Finland.

His research interests include advanced packaging in power electronics and its reliability.

Vesa Vuorinen received the M.Sc. degree in materials science and engineering and the D.Sc. (Tech.) degree in electrical and communications engineering from the Department of Electronics, Helsinki University of Technology, Espoo, Finland, in 1995 and 2006, respectively.

He is currently a Principal University Lecturer and the Project Manager with the Electronics Integration and Reliability Research Group, Aalto University, Espoo. During the last decade, his research has been focusing on materials compatibility in heterogeneous systems with an emphasis on interfacial phenomena. He has also been responsible for teaching physics of failure and reliability assessment in electronics and direct research cooperation with the industrial partners for the last 20 years. He has contributed to two textbooks dealing with interfacial compatibility issues and thermodynamics of solid-state diffusion as well as authored or coauthored more than 50 scientific articles and several book chapters.



Xing Liu received the master's degree in electrical engineering in 2018 from the Chemnitz University of Technology, Chemnitz, Germany, where he is currently working toward the Ph.D. degree in electrical engineering with the Chair of Power Electronics.

His research interests include the short-circuit behavior of IGBT and SiC-MOSFET, protection methods, gate drive design, and power cycling test.

Olli Fredrikson received the M.Sc. (Tech.) degree in electrical and electronics engineering from School of Electrical Engineering, Aalto University, Espoo, Finland, in 2016.

He is currently a reliability engineer with ABB, Helsinki. He has 11 years of experience in the field of power electronics and frequency converters.

Sebastian Brand received the Ph.D. degree in electrical engineering from the University of Magdeburg, Magdeburg, Germany, in 2004.

He is a Senior Scientist with the Fraunhofer Institute for Microstructure of Materials and Systems, Halle, Germany. He leads a research-, development, and application team for nondestructive defect localization techniques in the field of failure analysis and metrology in microelectronics. His current research extends from acoustic methods (e.g., Acoustic Microscopy) over Lock-In-Thermography to magnetic imaging microscopy.

He has more than 20 years of experience in the field of acoustics in life- and material sciences and authored/coauthored more than 100 publications in this and adjacent research fields.

Nikhilendu Tiwary (Member, IEEE) received the B.Tech. degree in applied electronics and instrumentation engineering from the Institute of Technical Education and Research, Bhubaneswar, India, in 2010, and the M.Tech. degree in biomedical engineering from Indian Institute of Technology Bombay (IIT Bombay), Mumbai, India, in 2012, and the Ph.D. degree in microelectronics from the Department of Electrical Engineering, IIT Bombay, in 2019.

He is a Staff Scientist with the Department of Electrical Engineering and Automation, Aalto University, Espoo, Finland. Currently, his research interests include advanced packaging and reliability, and advanced substrates for RF and power applications.

Dr. Tiwary was a committee member of Young Professionals IEEE Electron Devices Society from mid of 2022 until 2023 and received the Certificate of Achievement from IEEE Electronics Packaging Society in 2022.

Josef Lutz (Senior Member, IEEE) received the Diploma degree in physics from the University of Stuttgart, Stuttgart, Germany, in 1983, and the Ph.D. degree in electrical engineering from the Technical University of Ilmenau, Ilmenau, Germany, in 1999.

In 1983, he was with the SEMIKRON Elektronik GmbH, Nuremberg, Germany, where he was engaged in the development of GTO thyristors and fast-recovery diodes. Since 2001, he has been a Professor with the Chair of Power Electronics and Electromagnetic Compatibility, Chemnitz University of Technology, Chemnitz, Germany. He holds several patents in the field of fast-recovery diodes.

Dr. Lutz was the recipient of the Honorable Professor Award by the North Caucasus State Technical University, Stavropol, Russia, in 2005, and the Outstanding Achievement Award from the EPE ECCE Europe Conference in 2017. He is a Member of the Board of Directors of the ZfM, International Steering Committee of the EPE, Technical Committee of the ISPSD, Advisory Board of the PCIM, Technical Program Committee of CIPS, and Program Committee of the ISPS.

Mervi Paulasto-Kröckel (Member, IEEE) received the M.Sc. (Tech.) in 1990 and the D.Sc. (Tech.) in 1995 from Helsinki University of Technology, Espoo, Finland, both in materials science and semiconductor technology.

She is a Full Professor with the School of Electrical Engineering, Aalto University, Espoo. She leads the Electronics Integration and Reliability (EILB) Group focusing on heterogeneous integration of semiconductors, three-dimensional piezoelectric microelectromechanical systems, environmental impacts, and reliability of electronics. Prior to re-establishing an academic career end of 2008, she worked more than 12 years in various research and development positions within the automotive semiconductor industry in Germany. Her group has recently developed innovative technologies for low-temperature heterogeneous integration, piezoelectric in-plane MEMS actuation, and alternative compound semiconductor substrates. She has authored and coauthored more than 150 scientific papers.

Prof. Paulasto-Kröckel is a member of Finnish Academy of Technical Sciences.