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A Novel Soft-Switched SEPIC-Based DC–DC Converter With High Voltage Gain

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ABSTRACT This study introduces a novel high-gain DC-DC converter by integrating a coupled inductor (CI) and a voltage multiplier cell (VMC) into the conventional SEPIC topology. An auxiliary switch, benefiting from zero voltage switching (ZVS), is applied to provide ZVS for the main switch over a wide output power range. Moreover, the employed diodes turn off under zero current switching (ZCS), thus eliminating reverse recovery losses and increasing efficiency. This study conducts a comprehensive analysis and compares the proposed converter with state-of-the-art topologies. The claimed features are verified by implementing a prototype that converts 36 to 250 V.

INDEX TERMS Zero voltage switching (ZVS), zero current switching (ZCS), high step-up converter, coupled inductor.

I. INTRODUCTION

The escalating consumption of fossil fuels in recent years has exacerbated global warming, emerging as one of the major concerns worldwide. Therefore, numerous solutions have been proposed to reduce the impact of this crisis on the planet. Renewable energy sources, such as photovoltaic panels, have gained popularity as a practical solution due to their remarkable advantages. However, the output voltage of these sources needs to be enhanced to supply the DC link of inverters. Hence, increasing the output voltage amplitude of panels is inevitable, and high-gain converters are required to achieve this goal [1], [2].

The ideal conventional boost converter can provide the desired voltage gain by setting the duty cycle properly. Accordingly, infinite voltage gain is accessible as the duty cycle approaches the unity. However, under non-ideal circumstances, increasing the duty cycle to considerable values leads to decreased power transferring time to the output and a rise in losses. Furthermore, the boost converter encounters significant voltage stress across semiconductors and offers limited voltage gain, presenting challenges for its utilization in high-voltage applications [3], [4].

Diverse techniques and circuits have been suggested to overcome the limitations of the boost structure. Cascading two converters is one way to increase voltage gain. A cascaded converter with a lossless snubber circuit to recover leakage inductance energy is introduced in [5]. However, the number of components utilized in this topology is substantial, resulting in a significant increase in loss and cost. In addition, using three magnetic cores in the structure makes the circuit bulky and heavy.

The authors in [6] suggest a three-level boost converter to reduce semiconductor voltage stress. However, the provided voltage gain is small, and the duty cycle is the only variable that influences voltage gain. Consequently, there is a necessity to substantially increase the duty cycle to achieve high gain, leading to an increase in conduction loss.

The interleaved technique is extensively employed to mitigate input current ripple and reduce current stress across semiconductors. The interleaved converters suggested in [7], [8], [9] accomplish this purpose. Besides using too many diodes and switches in [7] and [8], both converters use three magnetic cores, increasing the weight and volume. Also, using

four active switches in [9] complicates the control and drive circuits and increases cost.

Z-source converters can achieve a high voltage gain at small duty cycle values. However, the discontinuous input current of these converters makes their use in PV panel applications challenging [10]. To address this issue, quasi-z-source converters are introduced. The proposed structures in [11] and [12] simultaneously draw a continuous input current and have the benefits of z-source topologies. Nevertheless, using numerous components is the significant drawback of the converters.

A single-switch high-gain CI-based converter is presented in [13]. Despite the reduced number of components and simple structure, the loss of the switch is remarkable due to hard-switching performance and significant current stress. In [14] and [15], high-gain converters employing the switched-capacitor technique are proposed. The bold disadvantages of the introduced topologies are the use of many capacitors and diodes to achieve high voltage gain and substantial switching loss due to the hard-switching performance. VMC with a combination of diodes and capacitors in [16] and a combination of switch, diodes, and inductor in [17] are presented. Although the voltage gain rises by these cells, providing a significant voltage gain requires adding many cells in the converter. Consequently, the number of components in high-gain applications is significantly increased. In addition, switches in [17] turn off/on under hard switching, increasing switching loss.

The converters proposed in [18] and [19] employ auxiliary switches to provide soft-switching performance, and both converters provide significant voltage gain. However, [18] utilizes many components, and the topology in [19] has the drawbacks of omitting common ground and the substantial input current ripple. Soft-switched structures without auxiliary switches are given in [20], [21], [22], [23]. Nevertheless, the voltage gain provided by [20] is small, necessitating multiple VMCs for high-voltage applications. Converters in [21] and [22] have the disadvantages of discontinuous input current and employing many semiconductors, respectively. Notably, the diodes in [23] withstand the stress identical to the output voltage irrespective of duty cycle value and turn ratio.

Several topologies utilizing the SEPIC structure are introduced in [24], [25], [26], [27], [28]. However, the topologies introduced in [24], [25], [26], [27] suffer from hard-switching performance, whereas the design presented in [28] provides limited voltage gain. The modified SEPIC-based converter presented in [29] achieves substantial voltage gain by employing a CI and a VMC. Nevertheless, this design only provide ZCS during the switch turn-on.

This paper proposes a novel high step-up fully soft-switched converter based on SEPIC structure and CI. Besides common ground between input and load, the proposed converter provides a continuous input current with a small ripple. Both switches turn off/on at ZVS, eliminating switching loss in the topology. Additionally, ZVS turn on of switches removes capacitive loss caused by snubber capacitors during turning on. Notably, diodes turn off at ZCS, significantly reducing switching and reverse recovery losses.

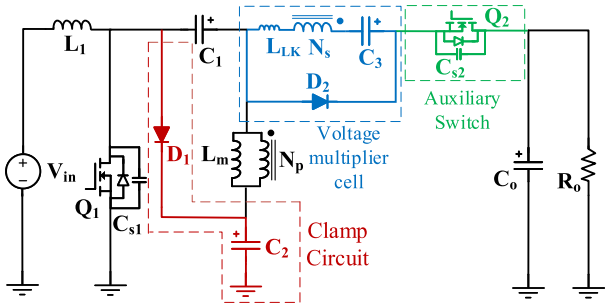

FIGURE 1. The proposed converter.

II. PRINCIPLE OPERATION

The proposed converter based on the SEPIC structure is illustrated in Fig. 1. L_1, C_1, and Q_1 are the components of the conventional SEPIC converter. It is observable that the second inductor and output diode in the conventional SEPIC converter are replaced with a CI and a switch, respectively. The CI model includes a leakage inductance (L_{LK}) referred to the secondary side, magnetizing inductance (L_m), and an ideal transformer with the turn ratio of $n = N_S/N_p$. A VMC consisting of CI secondary, C_3 and D_2, is added to the circuit to increase voltage gain.

D_1 and C_2 also make a clamp circuit to eliminate the voltage spike across the main switch. Q_2 is the auxiliary switch employed to create the ZVS circumstances for the main switch. Notably, C_{s_1} and C_{s_2} are the snubber capacitors of Q_1 and Q_2, respectively. L_1 operates in the continuous current mode (CCM) in the entire switching cycle, while L_m is assumed to be small enough that its current polarity changes in one switching period. Moreover, the semiconductors are considered ideal for simplifying calculation and analysis in the steady state. Fig. 2 illustrates the key waveforms of the proposed converter, and anticipated operating modes are depicted in Fig. 3.

Mode 1 [t_0-t_1]: Q_1 is turned on, and the input voltage magnetizes L_1. Consequently, the input current, identical to the L_1 current, increases linearly. Since the voltage difference between C_1 and C_2 is applied to L_m, its current decreases to zero. D_1 is deactivated with the clamped voltage stress equals the C_2 voltage. Moreover, Q_2 is turned off and withstands voltage stress of difference between C_1 and C_o voltages. D_2 current is diminished because of the linear decline in the current of the leakage inductor. Notably, the output capacitor supplies the load, and the following equations can be derived.

$$V_{L_1} = V_{\text{in}} \tag{1}$$

$$V_{L_m} = V_{C_1} - V_{C_2} \tag{2}$$

Mode 2 [t_1-t_2]: This mode begins when L_m current falls below zero, decreasing linearly after the polarity reverses. Notably, the CI secondary current still declines.

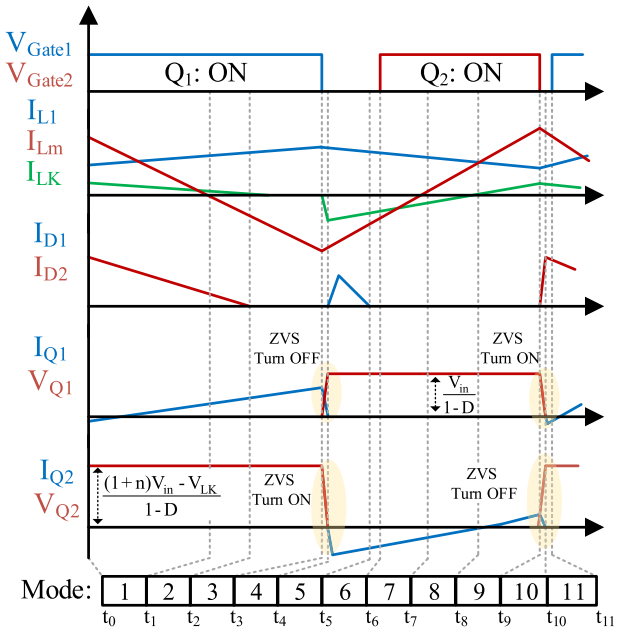

FIGURE 2. Key waveforms.

Mode 3 [t_2-t_3]: Since the passing current reaches zero, D_2 becomes deactivated at ZCS, eliminating the reverse recovery loss. The voltage stress is then clamped to the sum of C_3 and the CI secondary voltages. Furthermore, the currents of L_m and C_1 become identical, and the sum of L_1 and L_m currents flows through the main switch. The L_m current continues to decrease with the same applied voltage as in the previous modes.

Mode 4 [t_3-t_4]: Q_1 is turned off, and the snubber capacitor restricts the rate of voltage variation across it. Therefore, Q_1 is turned off at ZVS. Meanwhile, the current passes through D_2 and the leakage inductor discharges the snubber capacitor of Q_2. At the end of the mode, C_{s_1} voltage increases to its maximum value, while C_{s_2} voltage decreases until it reaches zero.

Mode 5 [t_4-t_5]: The discharging of C_{s_2} and the leakage inductance presence cause the body diode of Q_2 to conduct. Once voltage of C_{s_1} reaches V_{C_2}, D_1 begins conducting. Consequently, the applied voltage to L_m is equal to V_{C_1}, which means the slope of its current becomes positive. Also, C_1 discharges until its current equals the input current, causing D_1 to turn off at ZCS.

Mode 6 [t_5-t_6]: After D_1 turns off, part of the stored energy in L_1 and L_m is transferred to the output through the body diode of Q_2. Consequently, Q_2 can be activated at any time at ZVS. The leakage current decreases from the maximum value reached in the previous mode. The following equations can be derived.

$$V_{L_1} = V_{\text{in}} + V_{C_1} - V_{L_m} - V_{C_2} \tag{3}$$

$$V_{L_m} = \frac{V_o}{1+n} - \frac{V_{C_2}}{1+n} - \frac{V_{C_3}}{1+n} - \frac{V_{LK}}{1+n} \tag{4}$$

Mode 7 [t_6-t_7]: Q_2 turns on at ZVS due to the conduction of its body diode. Q_2 current linearly decreases until it reaches zero, after which its polarity reverses. Furthermore, the L_m current increases until it approaches zero.

Mode 8 [t_7-t_8]: The polarity of the L_m current changes, and its increase continues. Moreover, the leakage inductor current is still decreasing linearly. The leakage current reaches zero as the L_m current equals the input current.

Mode 9 [t_8-t_9]: This mode commences when the polarity of the leakage current is reversed. The current passing through Q_2 matches the leakage inductor current, leading to a linear increase in the amplitude of the Q_2 current. The leakage current can be determined using Kirchhoff's law, as indicated in (5).

$$I_{Lk} = \frac{I_{L_m} - I_{\text{in}}}{1+n} \tag{5}$$

Mode10 [t_9-t_{10}]: Due to the presence of the C_{s_2}, Q_2 can be turned off at ZVS. Resonating with leakage inductance causes the voltage of C_{s_2} to increase until its maximum voltage is reached. Q_2 turning off besides stored energy in the leakage inductance creates the circumstances in which D_2 starts conducting. Additionally, C_{s_1} discharges with the current difference between L_m, L_1, and the primary of the CI. This mode continues until C_{s_1} is completely discharged and C_{s_2} reaches its maximum value.

Mode 11 [$t_{10}-t_{11}$]: The discharge of C_{s_1} causes the diode body of Q_1 to conduct. Consequently, the main switch can be activated at ZVS, eliminating switching loss. After Q_1 turns on, C_1 current decreases until reversing the polarity, and the next cycle can be started.

III. STEADY-STATE ANALYSIS

Using (1), (2), (3), and (4) along with the volt-second balance of L_1 and L_m results in the following average capacitor voltages.

$$V_{C_1} = \frac{D}{1-D} V_{\text{in}} \tag{6}$$

$$V_{C_2} = \frac{V_{\text{in}}}{1-D} \tag{7}$$

Considering leakage inductance impact, the C_3 voltage can be obtained as (8).

$$V_{C_3} = nV_{\text{in}} - V_{LK} \tag{8}$$

Employing (4), (7), and (8) results in the output voltage equation as follows.

$$V_o = \frac{1+D+n}{1-D} V_{\text{in}} - \frac{V_{LK}}{1-D} \tag{9}$$

Considering the linear decrease of the current in the leakage inductor when the main switch is turned on, the time at which the leakage current reaches zero and the leakage inductor voltage can be expressed as (10) and (11), respectively.

$$t' = \frac{2I_o(1+n)T_s}{I_{L_m,\text{peak}} - I_{L_1,\text{min}}} \tag{10}$$

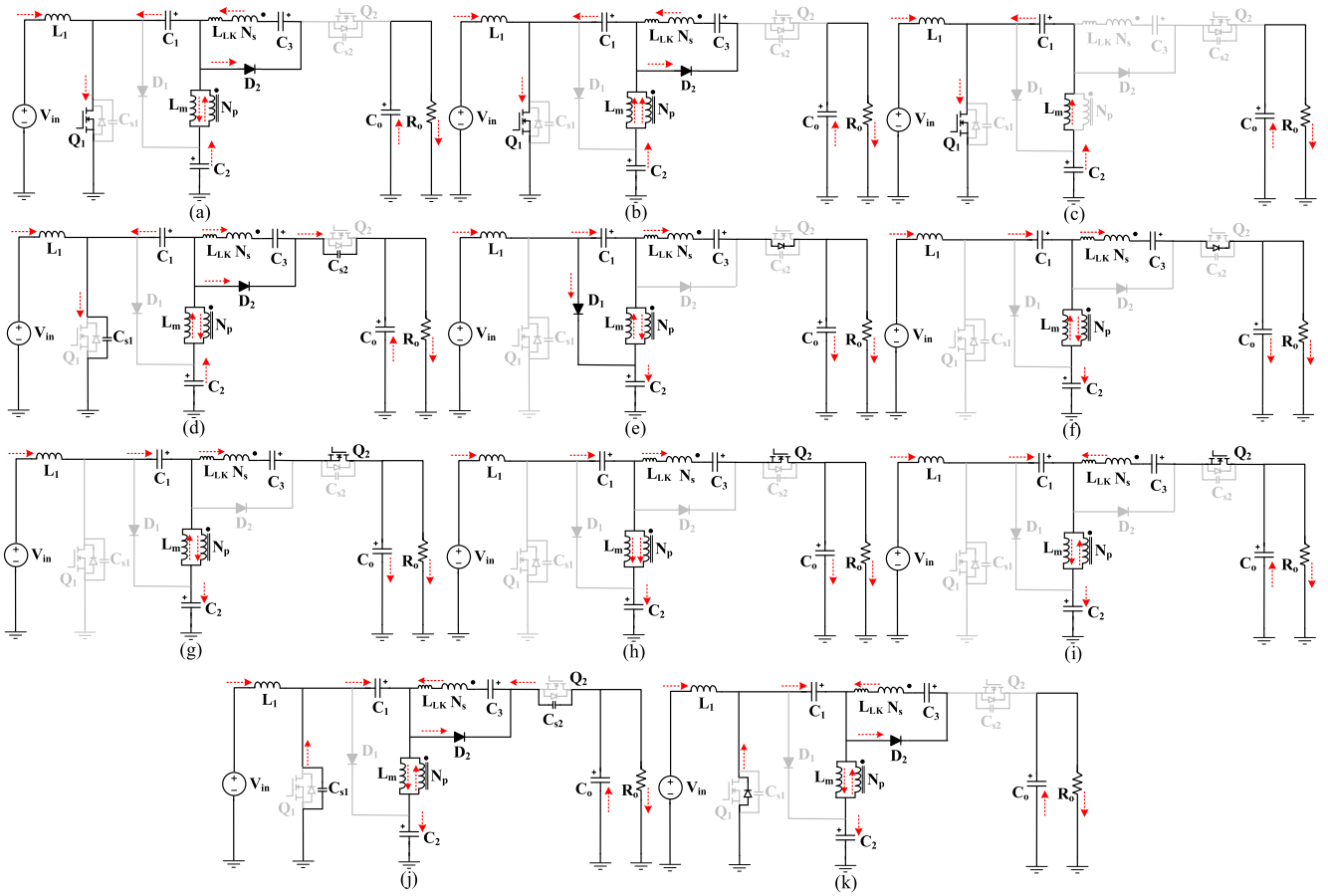

FIGURE 3. Operation modes of the proposed converter, (a) mode 1 [$t_0 - t_1$], (b) mode 2 [$t_1 - t_2$], (c) mode 3 [$t_2 - t_3$], (d) mode 4 [$t_3 - t_4$], (e) mode 5 [$t_4 - t_5$], (f) mode 6 [$t_5 - t_6$], (g) mode 7 [$t_6 - t_7$], (h) mode 8 [$t_7 - t_8$], (i) mode 9 [$t_8 - t_9$], (j) mode 10 [$t_9 - t_{10}$], (k) mode 11 [$t_{10} - t_{11}$].

$$V_{LK} = \frac{L_{LK}(I_{L_m,\text{peak}} - I_{L_1,\text{min}})}{t'(1+n)} \tag{11}$$

Regarding (3), (4), and (6)–(8), the voltage stresses across the semiconductors are as follows.

$$V_{Q_1} = V_{D_1} = \frac{V_{\text{in}}}{1-D} \tag{12}$$

$$V_{Q_2} = \frac{(1+n)V_{\text{in}} - V_{LK}}{1-D} \tag{13}$$

$$V_{D_2} = \frac{nV_{\text{in}} - V_{LK}}{1-D} \tag{14}$$

IV. DESIGN CONSIDERATIONS

According to (5), the peak of L_m current must exceed the input current to reverse the leakage current. Therefore, the following equation must be satisfied.

$$\frac{\Delta I_{L_m}}{2} + I_{L_m,avg} > I_{\text{in}} \tag{15}$$

Where ΔI_{L_m} and I_{L_m} indicate the current ripple and average current of the magnetizing inductor, respectively. Using ampere-second balance and Kirchhoff's law, the average current of L_m equals $-I_o$. Also, ΔI_{L_m} can be calculated as (16) during the main switch ON-time.

$$\Delta I_{L_m} = \frac{(V_{C_1} - V_{C_2})D}{L_m f} \tag{16}$$

Substituting (16) in (15) results in a critical inductance value of L_m as below.

$$L_m < \frac{(V_{C_1} - V_{C_2})D}{2f(I_{\text{in}} - I_o)} \tag{17}$$

To create the ZVS condition for switches in mode 10, the snubber capacitors of Q_1 and Q_2 must be discharged and charged, respectively. It can be assumed that the leakage inductance is referred to the primary side. Hence, the series L_m and L_{LK}, parallel with the L_1, can be considered the equivalent inductor that charges/discharges snubber capacitors. In other words, the equation below must be satisfied.

$$\frac{1}{2}L_{eq}{I_{eq}}^2 > \frac{1}{2}C_{eq}V^2 \tag{18}$$

where I_{eq} can be calculated as follow.

$$I_{eq} = \frac{I_{L_m} - I_{\text{in}}}{1+n} \tag{19}$$

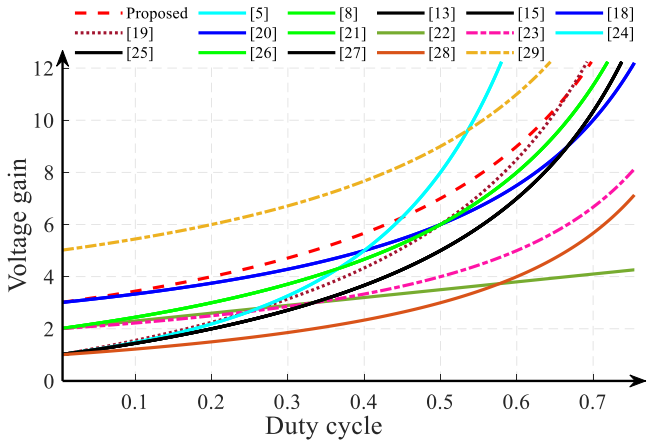

FIGURE 4. Voltage gain for investigated converters.

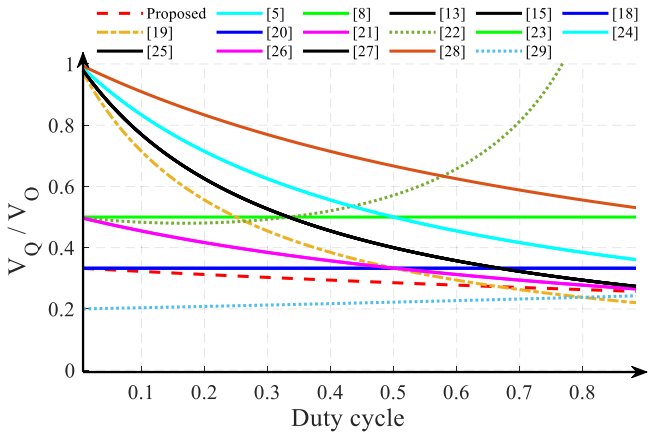

FIGURE 5. The normalized voltage stress across main switches in the investigated topologies.

Assuming the same value for snubber capacitors, the critical capacitance value can be expressed below.

$$C_{s_{1,2}} < \frac{(I_{L_m} - I_{\text{in}})^2 \left[\left(L_m + \frac{L_{LK}}{n^2} \right) || L_1 \right]}{(1+n)^2 V_{\text{in}}{}^2 (1 + (1+n)^2)} \tag{20}$$

The value of L_1, C_1, C_2, C_3, and C_o can be written as follows.

$$L_1 = \frac{V_{\text{in}} D}{f \Delta I_L} \tag{21}$$

$$C_1 = C_2 = \frac{I_o (n + D)}{f \Delta V_C} \tag{22}$$

$$C_3 = C_o = \frac{I_o D}{f \Delta V_C} \tag{23}$$

V. COMPARISON

To evaluate performance, the converter's characteristics are compared with recently introduced topologies. Table 1 displays different features and parameters of the surveyed topologies. The voltage gain relations in Table 1 are calculated by choosing $k = m = 1$, where k represents the coupling factor, and m is the number of stages in extendable topologies. Also, the gain ratio to components count is calculated with the duty cycle of 50% and the turn ratio of 2.

As a summary of Table 1, the proposed converter has a significant gain ratio to components count, which means the introduced topology can provide a high voltage gain using few components. Besides insignificant input current ripple, the proposed converter provides soft-switching for switches and common ground between the input source and the load. Fig. 4 illustrates the voltage gain of different topologies. The proposed converter demonstrates a higher voltage gain than the others over a wide range of duty cycles below 45%, except [29]. However, it is important to note that [29] uses more components than the proposed converter and only provides ZCS for the switch during turn-on. As the duty cycle exceeds 55%, the voltage gain provided by [5], [24] significantly rises. Nevertheless, The mentioned topologies suffer from hard-switching performance.

Table 1 also presents the normalized voltage stress across diodes and switches, defined as the ratio of the voltage stress on each semiconductor to the converter's output voltage. Fig. 5 shows the voltage stress across the main switch in the studied topologies. The key point is that the voltage stress on the main switch of the proposed converter remains below one-third of the output voltage across the entire duty cycle range.

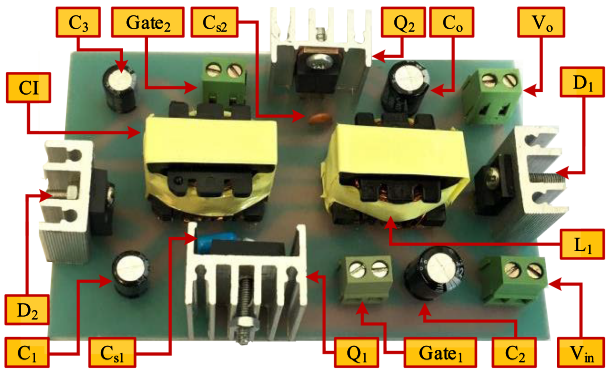

FIGURE 6. The prototype.

VI. EXPERIMENTAL RESULTS AND EFFICIENCY ANALYSIS

A prototype with 36 V input voltage, 250 V output voltage, and 100 W output power is implemented to approve the performance and theoretical relations. Notably, the duty cycle is about 50%, and the turn ratio is considered 2. Fig. 6 and Table 2 represent the prototype photograph and the characteristics of the implemented converter, respectively.

Fig. 7 illustrates the breakdown of losses in the converter at 100 W, utilizing parasitic component values obtained from the datasheets and equations provided in Table 3. Notably, the switching loss of the switches and reverse recovery loss of diodes are ignored due to the soft-switching performance of the converter. Observably, a substantial portion of the converter loss is related to the inductor.

TABLE 1. Different Features and Parameters of the Surveyed Topologies

	Voltage gain	Normalized voltage stress on main switch	Max. Voltage stress on the diodes	Soft-switching	Common ground	Gain/ No. of components	Input current ripple	D[1]	S[2]	M[3]	C[4]	Power/voltage rating
Proposed	$\frac{1+D+n}{1-D}$	$\frac{1}{1+D+n}$	$\frac{n}{1+D+n}$	✓	✓	0.7	non-pulsating with low ripple	2	2	2	4	100 W/250 V
[5]	$\frac{1+nD}{(1-D)^2}$	$\frac{1}{1+nD}$	$\frac{1+n}{1+nD}$	×	✓	0.57	non-pulsating with low ripple	6	1	3	4	200 W/400 V
[8]	$\frac{n(1+D)}{1-D}$	$\frac{1}{2(n-1)}$	0.5	✓	×	0.33	non-pulsating	7	3	3	5	210 W/420 V
[13]	$\frac{1+(n+1)D}{1-D}$	$\frac{1}{1+(n+1)D}$	$\frac{n+1}{1+(n+1)D}$	×	✓	0.5	non-pulsating with low ripple	2	1	2	3	200 W/200 V
[15]	$\frac{1+3D}{1-D}$	$\frac{1}{1+3D}$	$\frac{2}{1+3D}$	×	×	0.5	non-pulsating	2	2	3	3	200 W/260 V
[18]	$\frac{1+n}{1-D}$	$\frac{1}{1+n}$	$\frac{n}{1+n}$	✓	✓	0.43	non-pulsating with low ripple	4	2	2	6	500 W/400 V
[19]	$\frac{1+(n_1+n_2)D}{1-D}$	$\frac{1}{1+(n_1+n_2)D}$	$\frac{1+n_1}{1+(n_1+n_2)D}$	✓	×	0.6	non-pulsating	4	1	1	4	100 W/200 V
[20]	$\frac{1+n}{1-D}$	$\frac{1}{1+n}$	$\frac{n}{1+n}$	✓	✓	0.6	non-pulsating with low ripple	2	2	2	4	500 W/400 V
[21]	$\frac{2+Dn}{1-D}$	$\frac{1}{2+Dn}$	1	✓	✓	0.35	non-pulsating	8	2	2	5	400 W/432 V
[22]	$D+nD+n$	$\frac{1/(1-D)}{(D+nD+n)}$	$\frac{n/(1-D)}{(D+nD+n)}$	✓	✓	0.35	pulsating	3	2	1	4	150 W/400 V
[23]	$\frac{n}{1-D}$	$\frac{1}{n}$	1	✓	✓	0.4	non-pulsating with low ripple	2	2	2	4	300 W/400 V
[24]	$\frac{n-1+nD}{(1-D^2)(n-1)}$	$\frac{n-1}{n-1+nD}$	$\frac{n}{n-1+nD}$	×	✓	0.67	non-pulsating with low ripple	4	1	3	4	200 W/400 V
[25]	$\frac{1+3D}{1-3D}$	$\frac{1}{1+3D}$	$\frac{2}{1+3D}$	×	×	0.5	non-pulsating	2	2	3	3	100 W/200 V
[26]	$\frac{2+2D}{1-D}$	$\frac{1}{2+2D}$	$\frac{1}{2+2D}$	×	×	0.38	non-pulsating with low ripple	5	1	3	7	3000 W/800 V
[27]	$\frac{1+3D}{1-3D}$	$\frac{1}{1+3D}$	$\frac{2}{1+3D}$	×	×	0.5	non-pulsating	2	2	3	3	200 W/250 V
[28]	$\frac{1+D}{1-D}$	$\frac{1}{1+D}$	$\frac{1}{1+D}$	✓	✓	0.38	non-pulsating with low ripple	1	2	2	3	180 W/200 V
[29]	$\frac{(n+1)D+1}{1-D}+2n$	$\frac{1}{1+D+n(2-D)}$	$\frac{1+n}{1+D+n(2-D)}$	✓	✓	0.75	non-pulsating with low ripple	4	1	2	5	100 W/250 V

[1]power diodes count, [2]power switches count, [3]magnetic cores count, [4]capacitors count

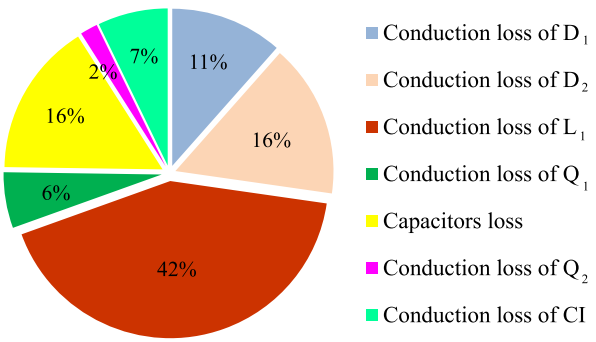

FIGURE 7. Loss breakdown of the proposed converter for 100 W output power.

The experimental waveforms of the proposed converter under full load are depicted in Fig. 8. The voltage and current of diodes are displayed in Fig. 8(a) and (b). It is observable that voltage stress across diodes validates the theoretical expectations. Additionally, both diodes turn off at ZCS, eliminating their switching and reverse recovery losses.

The gate-source voltages besides the L_1 current are indicated in Fig. 8(c). The L_1 current represents the input current appropriate for renewable energy applications due to continuity. Additionally, L_1 is magnetized as the main switch, or its body diode conducts, leading to a linear rise in the current. The voltage and current of capacitors are shown in Fig. 8(d)–(f). Notably, the current flowing through C_3 is the same as the referred leakage inductor current.

Q_1 voltage reaches zero before its current rises due to the ZVS condition, as depicted in Fig. 8(g). Also, the figure shows the ZVS performance of Q_1 at turning off, which happens due to the existence of C_{s_1}. The voltage and current of Q_2 are shown in Fig. 8(h). The initial passing current is negative, indicating that the body diode is conducting. Hence, Q_2 turns

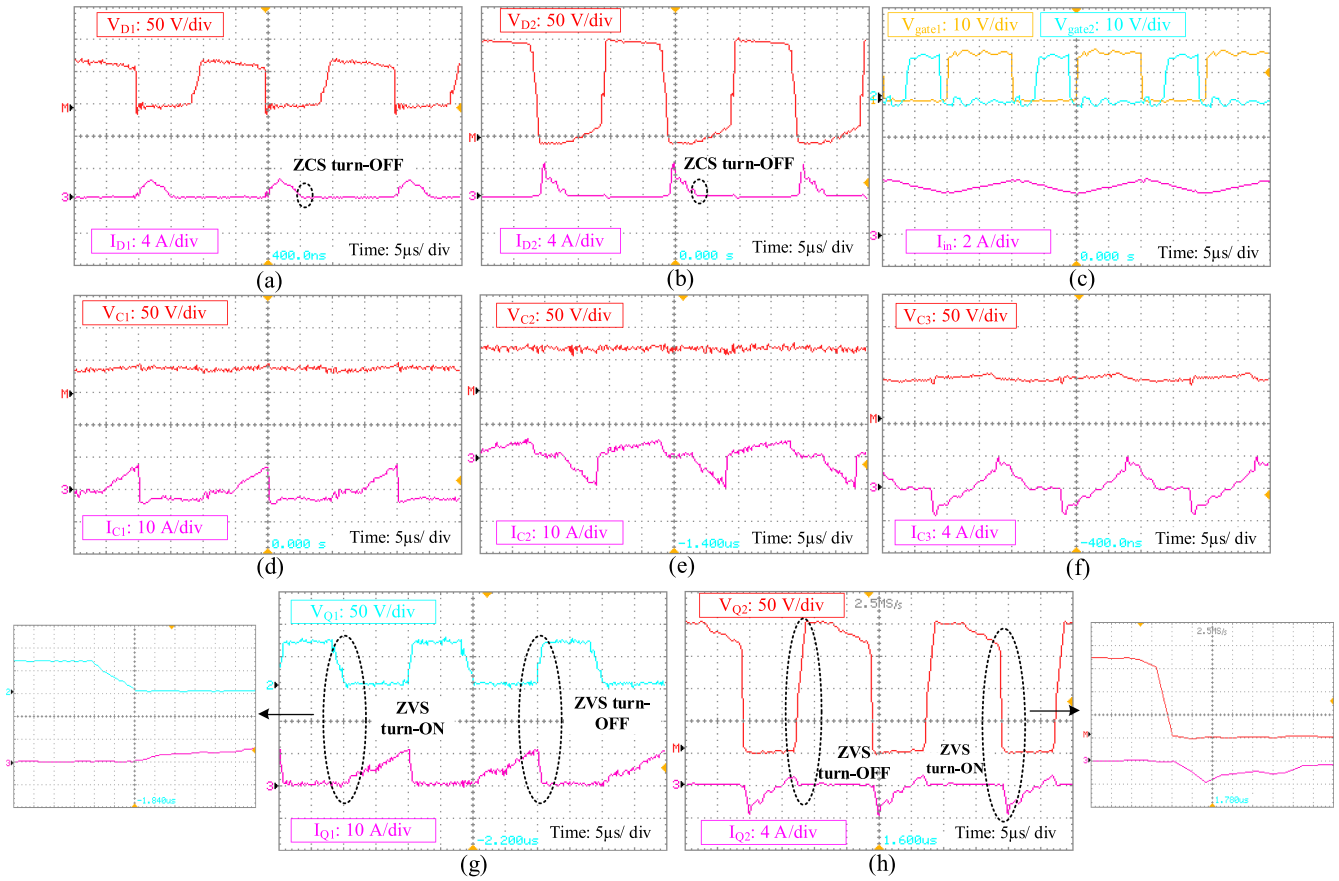

FIGURE 8. The experimental waveforms under full load. (a) Voltage and current of D_1, (b) Voltage and current of D_2, (c) Gate-source voltage of Q_1, gate-source voltage of Q_2, and input current, (d) Voltage and current of C_1, (e) Voltage and current of C_2, (f) Voltage and current of C_3, (g) Voltage and current of Q_1, (h) Voltage and current of Q_2.

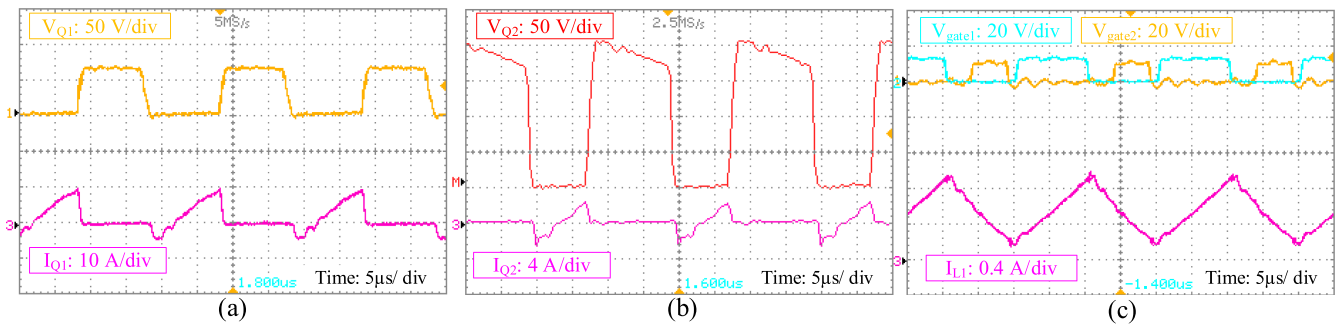

FIGURE 9. The experimental waveforms under light load. (a) Voltage and current of Q_1, (b) Voltage and current of Q_2, (c) Gate-source voltage of Q1, gate-source voltage of Q2, and input current.

on under the ZVS circumstance at any time. Furthermore, the ZVS condition at turning off is provided with the help of C_{s_2}.

To evaluate the performance of the converter under light load, the voltage and current of the main and auxiliary switches besides L_1 current at 20% of output power are illustrated in Fig. 9. When the voltage of switches reaches zero, the passing currents are negative, indicating that the body diodes of switches are conducting. Hence, soft-switching performance is not lost at light loads.

The efficiency of the proposed converter and other topologies is depicted in Fig. 10. To ensure a fair comparison, the converters are simulated after redesigning components to achieve optimized performance at the same output power. What stands out from the illustration is that the proposed converter provides higher efficiency compared to others for all

TABLE 2. Characteristics of the Implemented Prototype

Component/ Parameter	Part number/ Value
Duty cycle	50%
C_1 and C_3	6.8 μF
C_2 and C_o	10 μF
L_1	450 μH
L_m	18.2 μH
Secondary L_{LK}	2.5 μH
Primary L_{LK}	0.625 μH
Ferrite Core	E 28/10/11
CI Turns Ratio	9:18
Q_1	IRFP260
Q_2	P11NK40Z
D_1	MBR20200
D_2	SBR20A300CTFP

TABLE 3. Loss Calculations

Power Loss	Equation
Diodes loss	$I_o(V_{F_1} + V_{F_2})$
Conduction loss of Q_1	$R_{ds_1}(\frac{n+2D}{1-D} I_o\sqrt{D})^2$
Conduction loss of Q_2	$R_{ds_2}(I_o\sqrt{1-D})^2$
Conduction loss of L_1	$R_L(\frac{D+n+1}{1-D} I_o)^2$
Conduction loss of CI	$(R_{n_1} n^2 + R_{n_2})\frac{{I_o}^2}{D(1-D)}$
Capacitors loss[1]	$R_{ESR}{I_o}^2\frac{3D^2+4Dn+2n^2+1}{D(1-D)}$

[1] $R_{ESR_{C_1}} = R_{ESR_{C_2}} = R_{ESR_{C_3}} = R_{ESR_{C_o}} = R_{ESR}$

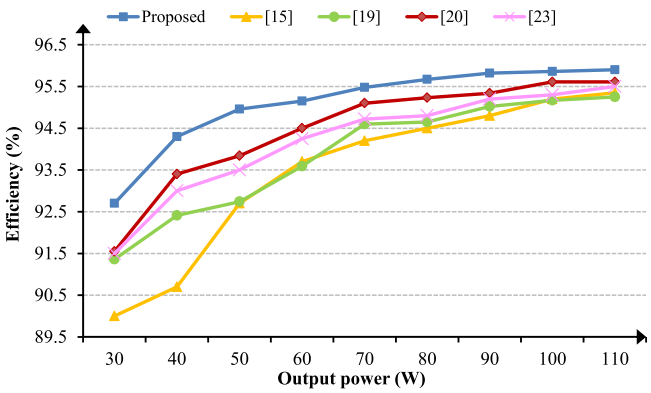

FIGURE 10. The proposed converter's efficiency compared to other topologies.

the power ranges studied. Moreover, the proposed converter has a higher efficiency in the full load than in the light load.

VII. CONCLUSION

This study presents a novel soft-switched SEPIC-based high step-up converter. By ensuring diodes turn off under ZCS conditions, the converter eliminates reverse recovery losses. Furthermore, achieving ZVS operation for both switches in turn off/on eliminates switching and capacitive turn-on losses. The proposed converter also benefits from the common ground between the input source and the load, continuous input current, and a high gain ratio to components count. Additionally, the proposed converter provide significant voltage gain while imposing minimal voltage stress on the semiconductors.

Based on experimental results, the switches demonstrated full soft-switching performance across a broad output power range, from light to full loads. Moreover, the diodes turned off under ZCS conditions, validating theoretical predictions. Besides the simple structure, all the mentioned features make the proposed converter an excellent candidate for high step-up applications.

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