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Published in:

Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC), 2017 IEEE

DOI: 10.1109/NORCHIP.2017.8124975

Published: 24/10/2017

Document Version Peer-reviewed accepted author manuscript, also known as Final accepted manuscript or Post-print

Please cite the original version:

Ahamed, R., Varonen, M., Parveg, D., Saijets, J., & Halonen, K. (2017). Design of high-performance E-band SPDT switch and LNA in 0.13 µm SiGe BiCMOS technology. In *Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC), 2017 IEEE* IEEE. https://doi.org/10.1109/NORCHIP.2017.8124975

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## Design of High-Performance E-band SPDT Switch and LNA in 0.13 µm SiGe BiCMOS Technology

Raju Ahamed<sup>1</sup>, Mikko Varonen<sup>2</sup>, Dristy Parveg<sup>1</sup>, Jan Saijets<sup>2</sup>, Kari A. I. Halonen<sup>1</sup> <sup>1</sup>Department of Electronics and Nanoengineering, Aalto University, Espoo, Finland <sup>2</sup>VTT Technical Research Centre of Finland Ltd, Espoo, Finland Email: raju.ahamed@aalto.fi

Abstract—This paper presents the design of high-performance E-band single-pole double-through (SPDT) switch and low noise amplifier (LNA) as a part of transceiver front-end in an 0.13 µm SiGe BiCMOS technology. The quarter-wave shunt SPDT switch is designed using reverse-saturated SiGe HBTs. The resulting switch exhibits an insertion loss of 2.1 dB, isolation of 26 dB, reflection coefficient better than 18 dB at 75 GHz and provides a bandwidth of more than 35 GHz. The designed switch is integrated with a single-in differential-output (SIDO) low noise amplifier (LNA) and utilized as input matching element of the LNA. The LNA utilizes a common-emitter amplifier at the first stage and a casocode amplifier at the second stage to exploit the advantages of both common-emitter and cascode topologies. The resulting LNA with integrated switch achieves a gain and noise figure(NF) of 26 dB and 6.9 dB, respectively at 75 GHz with a 3 dB bandwidth of 12 GHz. Output referred 1-dB compression point of +5.5 dBm is achieved at 75 GHz. The designed integrated block consumes 45.5 mW of DC power and occupies an area of 720 µm x 580 µm excluding RF pads.

*Index Terms*—BiCMOS, heterojunction bipolar transistor (HBT), LNA, millimeter-wave, MMIC, reverse-saturation, SiGe, SPDT, transformer balun.

## I. INTRODUCTION

The millimeter-wave field has been dominated by III-V semiconductor technologies [1]. Even though they present superior performance, they have low yield and limited integration capability. Due to recent improvements in silicon based technologies, it is possible to develop millimeter-wave systems in CMOS and SiGe technologies and the performance is competitive with the III-V technologies [2]- [3].

In many applications front-end switches are often used so that both the transmitter and receiver can share the same antenna. Using a single antenna for both the transmitter and receiver increases integration and which in turn reduces the cost. A typical transceiver front-end using transmit-receive (TR) switch to share the same antenna by both the transmitter and the receiver is shown in Fig.1. Low noise amplifier (LNA) is a critical building block in wireless receivers. Since LNA is the first block in the receiver path, the gain and noise figure from the LNA determines the noise figure of the whole receiver.

In this paper, design of an E-band SPDT switch and a transformer-based two-stage differential LNA is presented in an  $0.13 \,\mu\text{m}$  SiGe BiCMOS technology. The SPDT switch utilizes the reverse-saturated SiGe HBTs for improved per-



Fig. 1: Typical transceiver front-end where switch is used to share the same antenna by both the transmitter and the receiver.

formance. The two-stage LNA utilizes a common-emitter amplifier at the first stage and a casocode amplifier at the second stage to utilize the advantages of both common-emitter and cascode amplifier topologies.

## II. MILLIMETER-WAVE SPDT SWITCH

## A. Switch Design

The most commonly used topology for millimeter-wave switch is the quarter-wave shunt switch topology [4]. Fig.2 shows the schematic with working principle of the designed quarter-wave shunt switch utilizing reverse-saturated SiGe HBTs. In this topology, the upper device M1 is turned on with a high voltage at V1 and there is a low impedance at point A. The quarter-wave transmission line transforms the low impedance at point A into an approximately open circuit at the junction point P. Therefore, the upper-half of the switch presents nearly open circuit. As a result, RF energy at the junction point P is blocked from traveling towards the  $RF_{out1}$ port. On the other-hand, the lower device M2 is turned off with a zero voltage at V2, and there is an approximate open circuit at the point B. Therefore, a low loss path is created between  $RF_{in}$  port and  $RF_{out2}$  port which allows most of the RF energy to flow towards the  $RF_{out2}$  port. A shunt transmission line  $L_{stub}$  is used to resonate out the capacitance of the shunt device at the desired frequency. The shunt stub also provides the DC ground reference to the transistor terminal.

In this topology, the HBT is operated in "reverse-saturated" mode by connecting the collector terminal of HBT to ground and the emitter terminal to RF signal node. The reason for using reverse saturated HBT is the improved insertion



Fig. 2: Schematic and working principle of the reversesaturated shunt SPDT switch.

loss compared to the forward topology. This improvement is mainly due to higher emitter doping and also due to the better isolation of emitter from the Si substrate [4].

Control voltage values of 0 and 1 V were used for turning off and on the HBT respectively. The larger device provides better isolation but causes higher insertion loss. There is a clear trade-off between insertion loss and isolation. Therefore, the device size was selected to achieve an isolation of 25 dB with an insertion loss of 2 dB at 75 GHz. The length of inductive stub was  $250 \,\mu\text{m}$  to resonate out the off-state capacitance of shunt devices. The effect of RF pad has been taken into account only for input terminal  $RF_{in}$  as the switch will be integrated with the LNA and PA.

## B. Simulated Results

AWR AXIEM was used for EM simulation of the transmission lines, T-junction and RF pads to obtain accurate modeling. Post-layout simulation results of the designed switch are shown in Fig.3 and Fig.4. The insertion loss and isolation of the quarter-wave shunt SPDT switches with reverse-saturated HBTs are shown in Fig.3. The results show an insertion loss of 2.1 dB between ports  $RF_{in}$  and  $RF_{out2}$  and an isolation of better than 26 dB between ports  $RF_{in}$  and  $RF_{out1}$  at 75 GHz including RF pad loss at the common port. Both the input and output return losses are better than 18 dB at 75 GHz and show a very wideband response with better than 10 dB from 65 to 100 GHz. The switch is highly linear with an input referred 1-dB compression point of 16 dBm. DC power consumed by the SPDT switch is 12 mW.

#### **III. MILLIMETER-WAVE LNA**

## A. LNA Design

Commonly, millimeter-wave LNAs utilize common-emitter and cascode topologies [5]. The common-emitter amplifier provides a lower noise figure than the cascode whereas the cascode amplifier provides a higher gain than the common



Fig. 3: Simulated insertion loss and isolation of the designed reverse-saturated shunt switch.



Fig. 4: Simulated reflection coefficients of the designed reverse-saturated shunt switch.

emitter amplifier. Therefore, it is beneficial to combine both amplifier topologies to get the best performance. The commonemitter amplifier has been used at the first stage to achieve a low noise figure. The cascode configuration has been used at the second stage due to two important facts. Firstly, it has high gain and secondly the noise figure in the second stage is not that critical if the first stage has sufficient gain. As the next block after the LNA is differential one, a differential cascode stage has been used to provide differential output signal. Moreover, the linearity of the cascode stage is better than common-emitter stage due to the higher supply voltage.

Gain and noise figure are heavily dependent on the biasing of transistors. A lower noise figure can be obtained at lower bias point but the obtainable gain is also lower. As the bias voltage goes higher, the obtainable gain and noise figure increase rapidly. Therefore, a lower bias voltage was selected for the common-emitter stage to keep the noise figure low and a comparatively higher bias voltage was chosen for the cascode stage to achieve higher gain.



Fig. 5: Input matching network of the low noise amplifier.



Fig. 6: Input matching principle of a low noise amplifier using noise, gain and stability circles on the Smith chart. A, B, C and D represents the corresponding points after each element in Fig.5.

Input matching requires careful attention in the LNA design. An effective way of designing the input matching network is using the available gain, noise and source stability circles of the input transistor drawn on a Smith chart. Fig.5 shows the elements of the input matching network of the first stage LNA. The noise circles, gain circles, stability circle and the corresponding points after each element on the Smith chart are shown in Fig.6. The RF pad has been considered as the first element in the input matching network and the corresponding point on the Smith chart is A. As there is an SPDT switch before LNA, the switch is considered as a part of matching element for the LNA. This switch moves the impedance from A to B on the Smith chart. The next element is the DC block capacitor that blocks the DC from the supply towards the Port1, and ideally a short circuit at the desired frequency. However, in this design the DC block capacitor was used as a matching element. It moves the impedance point from B to C on the Smith chart. The biasing network is placed at the last position and it is used to reach the final point of input matching. It corresponds to the point D on the Smith chart. To attain higher gain, impedance was moved from point C to point D. At this point the desired noise and gain matching has been achieved. For a better noise figure one can move towards the center of the noise circles. Emitter degeneration is used to bring the gain circles and noise circles closer and to achieve simultaneous gain and noise matching. The emitter degeneration is realized by a microstrip line.



Fig. 7: Realization of transformer balun by placing two topmost metal layers on top of each other.

The interstage matching was designed so that the output of the first stage matches to the differential input of the second stage. The output from the first stage is single-ended and the differential cascode stage requires balanced signal at the input. Conversion of a single-ended signal to a differential signal is done by the transformer balun. In addition to the single-ended to differential conversion, the transformer serves for some other important purposes. The transformer is used as an impedance matching element. The transformer also provides bias points through the center-tapped primary and secondary windings [6]- [7]. In this design, the bias voltage to the second stage is provided through a balun transformer. The transformer was designed using ADS Momentum EM simulator. The primary and secondary of the transformer were realized by two topmost metal layers as shown in Fig.7. If the center point of both the primary and secondary are used to provide bias, the DC block capacitor can be eliminated. The final step to complete the LNA design is to match the output to 100  $\Omega$ . Fig.8 shows the complete schematic of the integrated SPDT switch and LNA. The RC networks on the DC path were added to improve the low frequency stability.

#### B. Simulated Results

Post-layout simulation results of the designed LNA integrated with the SPDT switch are shown in Fig.9. The LNA achieves a peak gain of 26 dB at 75 GHz and 3 dB bandwidth of 12 GHz from 68.5 GHz to 80.5 GHz. The common-emitter stage provides 7 dB of gain and differential cascode stage provides rest of the gain. The simulated noise figure is 6.9 dB and shows very wideband frequency response. Both the input and output return losses are better than 10 dB at 75 GHz. An output referred 1-dB compression point of +5.5 dBm has been achieved by the designed LNA. The DC power consumption of LNA itself is 33.5 mW. The stability factor



Fig. 8: Complete schematic of the integrated LNA and SPDT switch.

(K) and stability measure (B) shown in Fig.10 are greater than one and zero respectively, which represent the unconditional stability of the amplifier. The layout of the integrated LNA and switch is shown in Fig.11. The realized circuits occupy an area of  $720 \,\mu\text{m} \times 580 \,\mu\text{m}$  excluding the RF pads.



Fig. 9: Simulated S-parameters and noise figure of the integrated LNA and switch.

Table 1 compares the simulated performance of the designed E-band LNA including the switch to other published stateof-the-art E-band LNAs in SiGe BiCMOS processes. The designed two stage LNA together with switch demonstrates the lowest noise figure with a gain of 26 dB. As the noise figure contributed by the switch is around 2 dB, the noise figure contributed by the LNA itself is below 5 dB. The DC power consumption in the designed integrated block is 45.5 mW where the LNA itself consumes 33.5 mW that is considerably low compared to most of the other works. The designed LNA achieves the highest output 1 dB compression point ( $OCP_{1dB}$ ) among all the other published works.



Fig. 10: Simulated stability factor (K) and stability measure (B) of the E-band LNA.



Fig. 11: Layout of the integrated LNA and SPDT switch excluding RF pads.

Ref	Technology	Topology	Frequency	Gain	NF	Pdc	$OCP_{1dB}$
			(GHz)	(dB)	(dB)	(mW)	(dBm)
This**	130n BiCMOS	CE & Cascode	75	26*	6.9*	45.5*	+5.5*
[8]	350n BiCMOS	CE	77	20	5.8	40	+3
[9]	120n BiCMOS	CE	94	27	8	27.6	-
[10]	250n BiCMOS	Cascode	70	22.5	<7.2	52	+4.5
[10]	130n BiCMOS	Cascode	70	25	<9	54	+1
[11]	130n BiCMOS	CE	80	20	9	63	-

\*\* post-layout simulated \* including switch

## IV. CONCLUSION

This paper has presented high-performance SPDT switch and transformer-based single-input differential-output (SIDO) LNA in 0.13 µm SiGe BiCMOS technology. The quarterwave shunt SPDT switch achieved an insertion loss of around 2 dB, isolation of 26 dB at 75 GHz and bandwidth of more than 35 GHz from 65 GHz to 100 GHz. Design of a millimeter-wave LNA has been discussed. By utilizing switch as matching element, a transformer-based differential LNA has been designed. The designed LNA with integrated switch showed state-of-the-art performance providing the lowest noise figure of 6.9 dB with a gain of 26 dB and highest output 1-dB compression point ( $OP_{1dB}$ ) among the other E-band publications in SiGe technologies. The obtained high-results again present the potential of SiGe BiCMOS technologies for millimeter-wave system designs.

## ACKNOWLEDGMENT

This work was supported by the Finnish Funding Agency for Innovation (Tekes) as part of the 5WAVE project. The authors would like to thank Infineon Technologies for providing the foundry services for chip fabrication.

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