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A Common-Gate Common-Source Low Noise Amplifier Based RF Front-End With Selective Input-Impedance Matching for Blocker Resilient Receivers

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Abstract

This paper presents an integrated wideband RF front-end with improved blocker resilience achieved through selective voltage attenuation at both input and output nodes of the low noise amplifier (LNA). The architecture differs from traditional LNA architectures where blockers are only attenuated at LNA output node. The proposed dual attenuation is attained by designing a low intrinsic input impedance common-gate common-source low noise amplifier (CG-CS LNA) with capacitive feedback, together with an N-path filtering load. The capacitive feedback across the LNA ensures that the selective N-path filtering profile at the LNA output is transferred to the LNA input nodes creating a selective input impedance. Consequently, the achieved front-end input impedance is low at blocker frequencies and matched to the source impedance at the desired frequencies, creating the desired voltage attenuation for blockers. Further, a detailed theoretical analysis of proposed architecture is presented which leads to clear design guidelines. Evaluated in a 28nm fully-depleted silicon-on-insulator CMOS process, front-end is designed for wideband operation from 0.7 to 2.7 GHz. It consumes 11mA current from a 1V supply (excluding LO buffering) and possess a maximum NF of 5.1dB. The front-end demonstrates an out-of-band blocker compression point (BCP) of -1.5dBm and out-of-band IIP3 of +14dBm at a 100MHz offset from local oscillator frequency. In comparison to a traditional CG-CS LNA based front-end with wideband input impedance matching, the proposed front-end achieves 3.5dB improvement in the BCP at a 100MHz offset from LO.

KEYWORDS:

Blocker tolerance, Selective impedance matching, Low noise amplifier, RF front-end

1 | INTRODUCTION

Wireless receivers for emerging radio access standards such as 5G and LTE-A should ideally be able to operate on multiple frequency bands across a wireless spectrum of several GHz. Inherently, such wideband operation allows high power out-of-band (OB) blocker signals at the input of receiver front-end, which can potentially saturate the system.

⁰**Abbreviations:** Blocker tolerance, Selective impedance matching, Low noise amplifier, RF front-end

Traditionally, these OB blockers have mainly been attenuated through high-Q external off-chip RF filtering. However, since external RF filters are mostly non-tunable, multiple RF front-end filters are required to cover a broad range of frequency bands in wideband RF receivers. This creates a practical challenge to design both compact and wideband receivers. To provide a compact on-chip alternative to external off-chip filtering, techniques such as applying N-path filtering at the LNA output nodes (1, 2, 3, 4, 5, 6) and low noise transconductance amplifier (LNTA) based designs (7, 8, 9, 10) have been presented. However, as will be explained later, both of the above techniques generally implement blocker filtering at the LNA/LNTA output nodes, neglecting the filtering requirement at the LNA/LNTA input. Assuming that the blocker voltage gain to the LNA/LNTA output node is quite low, blockers can reach the front-end input swing range limits before the output swing limits. Therefore an optimum design should filter the OB blockers both at input and output nodes of RF front-end.

One can directly implement N-path filtering at LNA input but this results in increased NF due to added N-path mixers directly connected to LNA input (11). To avoid this noise penalty, N-path filters can be implemented in feedback configuration as in (12, 13, 14). In (12), an active interferer reflecting feedback loop is employed while in (13, 14), miller compensated bandpass filters, in dual negative feedback configuration, are utilized to create blocker rejection at LNA input. An active feedback technique has the disadvantage that feedback path may saturate in presence of large blocker while the dual negative feedback together with miller compensated bandpass filters in (13, 14) requires complicated dual feedback architecture for achieving the same goal. In this paper, we propose a blocker resilient RF front-end with low intrinsic input impedance at the blocker frequencies. The proposed circuit offers following key advantages over previously implemented approaches: First, the feedback path is completely passive in nature, reducing chances for feedback path saturation in presence of large blockers. Second, there are no mixers in the feedback path, reducing additional noise and LO power consumption and simplifying the feedback design and third, the proposed design is frequency agnostic meaning no prior information of blocker frequency is required for rejection.

The proposed front-end consists of a low intrinsic input impedance capacitive feedback common-gate (CG) common-source (CS) low-noise-amplifier (LNA) together with an N-path filtering load. The selective N-path filtering response at the LNA output node not only attenuates the blockers at the LNA output but also shapes the LNA input impedance response through the capacitive feedback. The shaped input impedance profile provides a low input impedance at blocker frequencies and a matched input impedance at the desired frequencies, thereby, creating additional blocker voltage attenuation at the LNA input node. In comparison to a traditional RF front based on a CG-CS LNA amplifier with wideband input impedance matching, the proposed front-end achieves +3.5dB improvement in blocker compression point (BCP) at a 100MHz offset from the LO frequency.

In our previous work (11) we have also investigated the possibility of dual node attenuation wideband RF front-end targeted for direct delta sigma receivers (DDSR's). The previously implemented RF front-end employs a global positive feedback from receiver output and an LNTA structure to attain the desired attenuation. However, there is an increased risk of instability in previous solution due to global positive feedback. Further, the solution also requires additional mixers for the feedback up conversion thereby increasing LO power consumption. In comparison, the solution proposed in this paper employs a completely different architecture to achieve the dual node attenuation using a local negative feedback LNA. This allows more sturdy operation with regards to stability.

The paper is organized as follows. Section 2 describes the prior art related to blocker tolerant RF front-ends. Sections 3 and 4 present the traditional capacitive feedback CG LNA, followed by the proposed CG-CS front-end design. Section 5 offers the necessary analysis, and based on the derived equations, design guidelines for CG-CS LNA are presented in Section 6. Section 7 details the circuit design of the CG-CS LNA and presents simulation results.

2 | PRIOR ART: BLOCKER TOLERANT RF FRONT-ENDS

As pointed out in Section I, well-known techniques such as applying N-path filtering to improve RF front-end OB blocker attenuation have been demonstrated previously (1, 2, 3, 4, 5, 6). N-path filtering as an on-chip solution provides accurately controlled high-Q RF bandpass filtering. Figure 1 shows a typical N-path filter based down-conversion receiver. The N-path capacitor C_{NP} together with feedback capacitor C_F and mixer switch resistance R_{SW} form a low pass filter at the mixer-to-baseband (BB) interface. Because a passive mixer is transparent in nature, it converts the BB low pass filtering response to an RF bandpass response. The advantage of the N-path filtering technique lies in its ease of tunability. The bandpass response can be easily tuned to the desired frequency by changing the local-oscillator (LO) frequency of the passive mixers. Further, if a higher order BB impedance is used as the N-path load, one can create a higher order bandpass response at the RF nodes(8). This helps to create additional attenuation for blocker frequencies. However, N-path filters do have some practical limitations. In contrast

to off-chip bandpass filters, blocker attenuation in N-path filters is limited by the mixer switch resistance R_{SW} and the LNA transconductance g_{mLNA} (2). This is due to the fact that at blocker frequencies, the N-path filtering capacitors provide minimum impedance, consequently making the N-path filter input impedance approximately equal to R_{SW} . This defines the approximate blocker gain as g_{mLNA} times R_{SW} . Consequently, both of these values should be minimized for reduced blocker gain. However, these parameters cannot be reduced indefinitely due to limitations on LO drive power consumption and LNA noise contribution.

Another technique for OB blocker rejection is to avoid voltage gain at RF frequencies by employing low-noise-transconductance-amplifier (LNTA)(7, 8, 9, 10). Receivers employing a LNTA's shift almost all the gain to the baseband (BB) stages, where it is easier to implement selective on-chip filtering for suppressing OB blockers. Reduced gain at RF frequencies results in a more linear RF-front end.

However, LNTA based receivers and N-path filtering techniques both generally implement filtering only at the output of the LNA/LNTA, neglecting the filtering opportunity at the LNA/LNTA input. Without filtering at input node and provided the low blocker gain from the LNA/LNTA, the LNA/LNTA transconductor input swing range may be reached before that of its output.

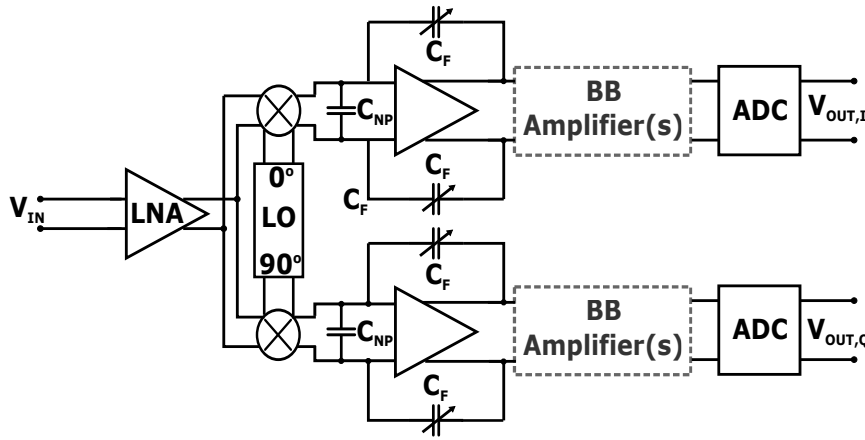


FIGURE 1 Generic block diagram of a direct conversion receiver with N-path filtering .

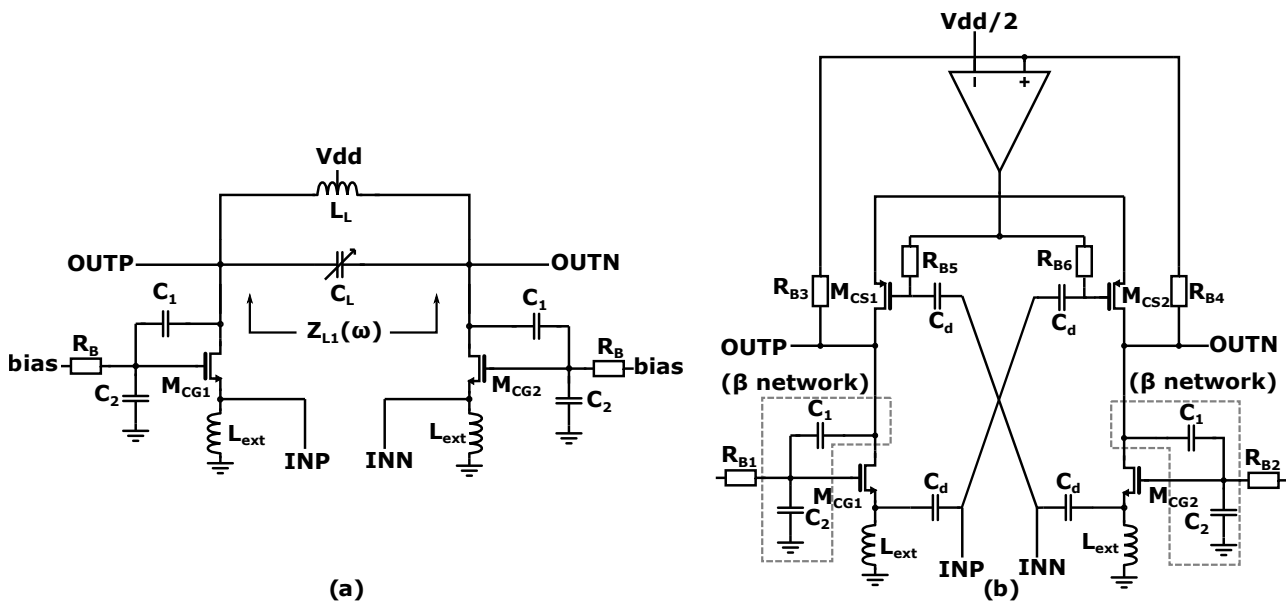


FIGURE 2 (a) Capacitive feedback CG LNA and (b) Proposed CG-CS LNA for blocker resilient RF front-ends.

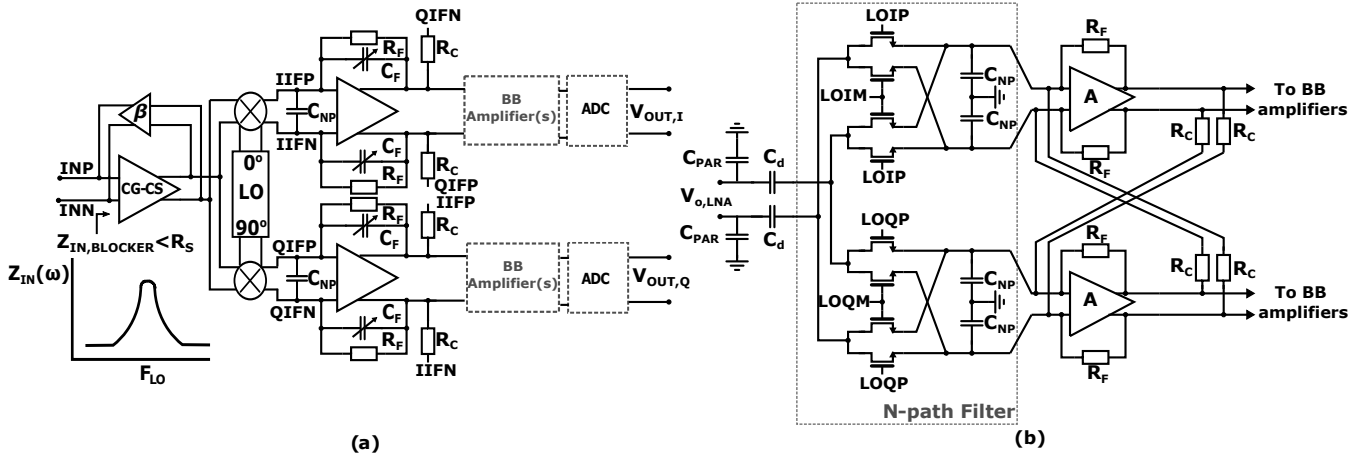


FIGURE 3 (a) Block diagram of the proposed RF front-end. (b) Differential implementation of a quadrature N-path filter load with complex BB feedback for frequency offset tuning.

This can cause the transconductor to enter into non-linear operation. Therefore, an optimum design should ideally filter the OB blockers already at the LNA/LNTA input.

Based on the aforementioned discussion, our solution is based on a low intrinsic input impedance capacitive feedback CG-CS LNA together with N-path filtering. The selective N-path response at the LNA output shapes the LNA input impedance profile, thereby creating blocker voltage attenuation at both the LNA input and output nodes.

3 | CAPACITIVE FEEDBACK CG LNA

Figure 2 (a) presents the capacitive feedback CG LNA with a selective input impedance profile, implemented in (15, 16) for an LC load. It demonstrates a narrowband input impedance profile when it is loaded by a selective impedance such as an LC resonant tank. The input impedance Z_{IN} of the LNA is given as (15):

$$Z_{IN} = \frac{1}{gm_1} + \left(\frac{C_1}{C_1 + C_2} \right) Z_{L1}(\omega), \quad (1)$$

where gm_1 is the transconductance of the device M_{CG1-2} and $Z_{L1}(\omega)$ represents the LNA load impedance at the frequency ω . From Eq. 1, one can infer the following: At OB blocker frequencies, where $Z_{L1}(\omega)$ is quite small, Z_{IN} is approximately equal to $1/gm_1$. This means that $Z_{IN} < R_S$ can be achieved by controlling the value of gm_1 . This will ensure attenuation for blockers at LNA input. At the desired frequency, however, the input impedance can be tuned to matched condition by controlling the resonant frequency of the load impedance $Z_{L1}(\omega)$ and the feedback factor β given by:

$$\beta = \frac{C_1}{C_1 + C_2}. \quad (2)$$

However, in reality, power consumption constraints of a practical design limit the designer to implement a very high value of CG gm. Therefore, in practice, blocker attenuation at LNA input due to lower LNA impedance is a compromise between input large signal linearity and power consumption. This compromise holds true for our next presented capacitive feedback CG-CS LNA as well.

4 | PROPOSED BLOCKER TOLERANT RF FRONT-END

4.1 | Capacitive Feedback CG-CS LNA

The LNA's in (15) and (16) both implement switchable LC loads to tune different frequency bands. In a wideband receiver scenario, switchable integrated LC loads consume huge silicon area while providing only a limited frequency tunability, and are therefore not a viable solution. Our proposed solution instead implements this wideband tunability through application of on-chip N-path filtering as LNA load. As per the authors knowledge this is the first paper where a capacitive feedback LNA has been implemented together with N-path filtering.

Figure 2 (b) presents the detailed diagram of the capacitive feedback CG-CS LNA while Figure 3 (a) presents the proposed blocker resilient CG-CS LNA based RF front-end. The LNA consists of push-pull CG and CS amplifiers where the capacitive feedback CG stage works in the same way as a typical capacitive feedback CG amplifier. A CS stage is added to increase the output impedance of the LNA as compared to resistive loads. This high output impedance is required for proper functioning of the N-path filtering as it affects the relative blocker attenuation (17). Furthermore, it also increases the LNA gain and provides flexibility to tune the LNA gain when needed. Resistors R_{B1} and R_{B2} provide the necessary dc-biasing while resistors R_{B3} - R_{B6} are added to sense the dc-bias voltage for the common mode feedback loop. The designed common-mode feedback loop ensures that the output common-mode voltage at OUTP/OUTN is set at half of the supply voltage, which creates an optimum output swing range.

4.2 | N-path Filter load

Figure 3 (b) presents the designed quadrature passive mixer N-path load. It consists of two quadrature passive mixers switching at an LO of 25% duty cycle. This creates a total of four switching phases. The number of N-path phases may vary depending on different N-path implementations. 8-phase and 16-phase arrangements have been reported in (18, 19). Additional N-path phases provide higher harmonic rejection and selectivity but come at the cost of increased complexity. In this paper, we have therefore restricted ourselves to a 4-phase implementation.

The N-path filter is loaded with a baseband impedance, which is a parallel combination of N-path capacitor C_{NP} (impedance $Z_{C,NP}$) and the BB amplifier input impedance Z_{BB} . The capacitors C_{NP} and C_F (multiplied by gain due to miller effect) form the total capacitance of N-path filter. They together with quadrature passive mixers constitute a first order band-pass response as seen from the RF side of mixers. Nevertheless, it is possible to implement higher order N-path baseband impedances such as in (8) with proposed LNA. Further, the baseband stages input impedance Z_{BB} is implemented through a feedback resistor R_F such that $Z_{BB} \approx R_F/(1 + A)$. Here A is the open loop gain of the feedback amplifier.

Complex feedback resistors R_C are added to compensate the effect of any parasitic capacitance at the LNA output. Any complex impedance present at the LNA output will manifest itself as a bandpass filter response offset from LO. This shifts the maximum gain of the LNA away from the LO and results in non-optimal front-end performance(20). The complex feedback resistors R_C overcome this problem by providing a complex BB input impedance(18, 21, 22).

Next we will derive the voltage gain, input impedance and NF expressions for the proposed front-end design. Unless otherwise specified, all circuit parameters in the derived expressions will be single-ended values.

5 | THEORETICAL ANALYSIS

For the derivation of desired design equations a simplified small signal model of proposed circuit can be made as shown in Figure 4 (a). In the model, R_S represents input source impedance, C_{in} is the parasitic capacitance at input nodes, gm_1 and ro_{CG} represent the CG amplifier transconductance and output impedance while gm_2 and ro_{CS} represent the CS amplifiers transconductance and output impedance. The capacitive feedback formed by capacitors C_1 and C_2 is represented through a feedback factor β . This assumption ignores the high frequency currents flowing through the capacitors C_1 and C_2 . Nevertheless, this effect of high frequency current can be included in the model as a current flowing through an equivalent capacitance of $C_1 C_2 / (C_1 + C_2)$ and can be lumped in the output capacitance $C_{out} = C_1 C_2 / (C_1 + C_2) + C_{par}$, where C_{par} is the parasitic capacitance at LNA output nodes. The LNA is loaded with an impedance Z_L , which can be represented as a parallel combination of N-path filter input impedance $Z_{NP}(\omega_{LO})$, C_{out} impedance (Z_{COUT}) and ro_{CS} .

In the N-path filter model, R_{SW} represents mixer switch resistance, $Z_{BB}(\omega_{IF})$ is the BB amplifier input impedance at intermediate frequency (IF), $Z_{CNP}(\omega_{IF})$ is the impedance of the N-path capacitor at intermediate frequency (IF) and ζ represents the frequency scaling factor. For four-phase quadrature passive mixers with 25% duty cycle, $\zeta = 2/\pi^2$. Further, $Z_{SH}(\omega_{LO})$ is virtual shunt impedance representing the power dissipation due to baseband signal upconversion. It can be expressed as(18):

$$Z_{SH} = (\sum_{n=3,7,11..}^{\infty} \frac{1}{n^2 Z_{OLNA}^*(nf_{LO})} + \sum_{n=5,9,13..}^{\infty} \frac{1}{n^2 Z_{OLNA}(nf_{LO})})^{-1} \quad (3)$$

Here, $Z_{OLNA}(nf_{LO})$ represents the LNA output impedance at specified nth harmonic of LO frequency.

As we will demonstrate later, the presented model is able to follow the transistor level design with reasonable accuracy. However, one limitation for the simplified small signal model originates from the complex nature of upconverted N-path response. Any complex impedance present at the LNA output will manifest itself as a bandpass filter response offset from the LO, shifting the maximum gain of the LNA away from LO. A slight change in gain will also be observed (20). The analytical equations do not take this complex frequency shift effect in account. This was done to avoid overwhelming complexity in derived equations and to make intuitive sense from results. Consequently, a small deviation from simulated results is expected. Nevertheless, as we will demonstrate in upcoming section, the deviation is small as long as capacitor C_1 is kept to lower values.

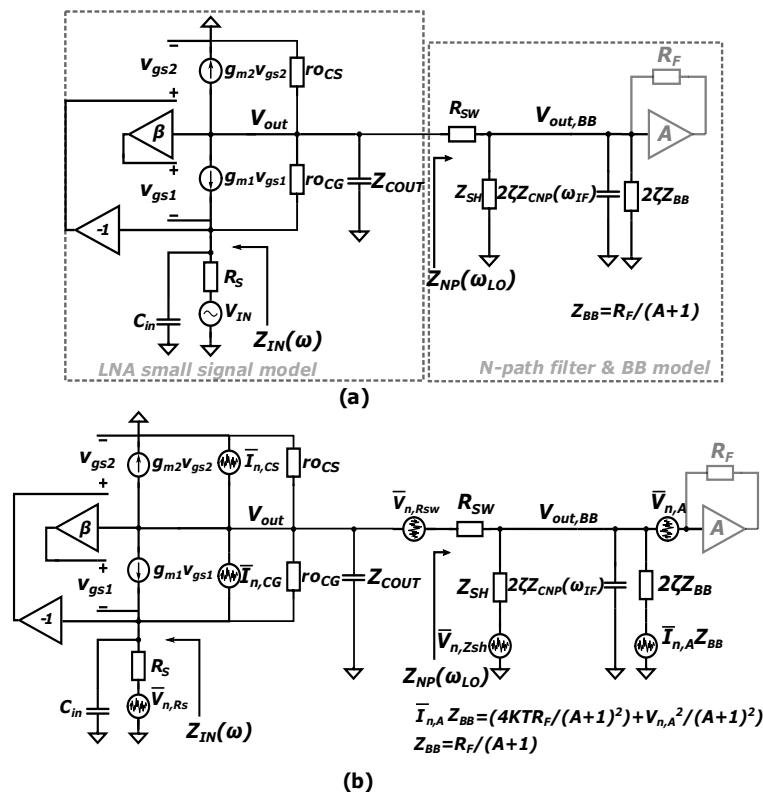


FIGURE 4 (a) Small signal model of the proposed front-end with N-path filter load and (b) its noise model.

5.1 | Voltage Gain

The RF voltage Gain (A_{vRF}) of the proposed LNA can be calculated using the small signal model shown in Figure 4 (a) and is given by:

$$A_{vRF} = \frac{2Z_L(\omega)[1 + ro_{CG}(gm_1 + gm_2)]}{\kappa}, \quad (4)$$

$$\kappa = R_S + Z_L + ro_{CG} + R_S(ro_{CG}gm_1 - Z_Lgm_2) + Z_Lro_{CG}\beta gm_1(1 - R_Sgm_2) + sC_{in}(R_SZ_L + R_Sro_{CG} + R_SZ_Lro_{CG}\beta gm_1), \quad (5)$$

and

$$\beta = \frac{C_1 + C_{GD,CG}}{C_1 + C_{GD,CG} + C_2}. \quad (6)$$

Here $C_{GD,CG}$ is the gate-to-drain capacitance of the CG transistor and $Z_L(\omega)$ is the parallel combination of N-path filter input impedance $Z_{NP}(\omega_{LO})$, C_{out} impedance (Z_{COUT}) and ro_{CS} . $Z_{NP}(\omega_{LO})$ can be given by (20):

$$Z_{NP}(\omega) = R_{SW} + 2\zeta Z_{BB}(\omega_{IF}) || Z_{SH}(\omega_{LO}) || 2\zeta Z_{CNP}(\omega_{IF}). \quad (7)$$

The total capacitance of N-path filter C_{NP} required to achieve certain BB bandwidth can be derived as:

$$C_{NP} \approx \frac{2\zeta[1 + (Z_{OLNA} + R_{SW})](1/Z_{SH} + 1/2\zeta Z_{BB})}{2\pi f_{BW}(Z_{OLNA} + R_{SW})} \quad (8)$$

The derived voltage gain Eq.4 is quite complex to offer intuitive understanding for the proposed circuit. We therefore, simplify the Eq.4 by neglecting the parasitic capacitances and CG/CS amplifier output impedances. This simplification results in further deviation from transistor level simulation results. Nevertheless, it allows us to crudely establish circuit behavior in terms of main design parameters. The simplified form of Eq.4 can be given as:

$$A_{vRF} = \frac{2(gm_1 + gm_2)Z_L(\omega)}{1 + gm_1[\beta Z_L(\omega) + R_S - gm_2\beta R_S Z_L(\omega)]} \quad (9)$$

Eq. 9 suggests that gain can be controlled mainly with gm_1, gm_2, β and Z_L . As we will demonstrate later, first three of these parameters directly influence the noise and input impedance-profile of LNA and therefore, should be chosen to meet the required noise levels and input impedance profile. This leaves us with Z_L to control LNA gain which is inherently a bandpass response due to $Z_{CNP}(\omega)$. At the desired frequencies, $Z_{CNP}(\omega)$ in Z_L behaves as a very high impedance and therefore can be neglected. This means that Z_L can be controlled through $Z_{BB}(\omega_{IF})$ to achieve the desired gain. In contrast, at the far-away blocker frequencies, the $Z_{CNP}(\omega)$ behaves as nearly short-circuit causing Z_L to approach R_{SW} impedance. This means that if R_{SW} is kept small, the gain at blocker frequencies can be reduced to a much lower value as desired.

RF-to-BB voltage gain of the proposed front-end can be found as:

$$A_{vBB} = A_{vRF} \left(\frac{\pi}{2\sqrt{2}} \right) \left(\frac{Z_{BBtot}}{Z_{BBtot} + R_{SW}} \right), \quad (10)$$

where

$$Z_{BBtot} = 2\zeta Z_{BB}(\omega_{IF}) || Z_{SH}(\omega_{LO}) || 2\zeta Z_{NP}(\omega_{IF}). \quad (11)$$

and the factor $\frac{\pi}{2\sqrt{2}}$ comes from the Fourier series analysis of a quadrature downconversion mixer with 25% dutycycle.

5.2 | Input Impedance

Based on the proposed front-end small signal model, presented in Figure 4, the input impedance (Z_{IN}) can be derived as:

$$Z_{IN} = \frac{Z_L + r_{oCG} + Z_L r_{oCG} \beta g m_1}{1 + r_{oCG} g m_1 - Z_L g m_2 - Z_L r_{oCG} g m_1 g m_2 \beta + s C_{in} [Z_L + r_{oCG} + Z_L r_{oCG} \beta g m_1]}, \quad (12)$$

To provide an intuitive understanding, Eq.12 can be simplified by neglecting the effect of parasitic capacitances and CG/CS amplifier output impedances. Though this simplification results in further deviation from transistor level simulation results, it allows us to crudely establish circuit behavior in terms of main design parameters. The simplified form of Eq.12 can be given as:

$$Z_{IN} = \frac{1}{g m_1 (1 - \beta g m_2 Z_L(\omega))} + \frac{\beta Z_L(\omega)}{1 - \beta g m_2 Z_L(\omega)} \quad (13)$$

Similar to an LC load, the $Z_L(\omega)$ load created by N-path filtering presents a bandpass filter response at RF, i.e, high impedance at the desired frequency and low impedance at blocker frequencies. Consequently, Eq. 15 suggests that at blocker frequencies, contribution of $Z_L(\omega)$ to the input impedance Z_{IN} is minimal and Z_{IN} is roughly equal to $1/g m_1$. To create a selective input impedance profile, a high value of $g m_1$ is selected such that the input impedance at blocker frequencies is much lower than the source impedance R_S . On the other hand, at the desired frequency, higher $Z_L(\omega)$ increases the Z_{IN} beyond $1/g m_1$ but can be tuned to matched condition by proper selection of feedback factor β .

5.3 | Noise Figure

For the proposed architecture, a noise model constituting all major noise sources can be constructed as shown in Figure 4 b). For the LNA, main noise contribution comes from the channel currents of CG and CS devices while in the N-path filter load, the main noise contributors are the R_{SW} thermal noise and the noise produced by Z_{SH} . Through a simplified nodal analysis, we can derive the noise factor F of proposed front-end as:

$$F = 1 + \left(\frac{4 Z_L(\omega)^2 \gamma g m_1}{A_{vRF}^2 R_S} \right) \left(\frac{r_{oCG} - R_S r_{oCG} g m_2 + s C_{in} R_S r_{oCG}}{\alpha} \right)^2 + \left(\frac{4 Z_L(\omega)^2 \gamma g m_2}{A_{vRF}^2 R_S} \right) \left(\frac{R_S + r_{oCG} + R_S r_{oCG} g m_1 + s C_{in} R_S r_{oCG}}{\alpha} \right)^2 + \left(\frac{\overline{V_{NP}^2} (R_{OLNA} / (R_{OLNA} + Z_L))^2}{K T R_S A_{vRF}^2} \right), \quad (14)$$

where

$$\alpha = R_S + Z_L + r_{oCG} - R_S Z_L g m_2 + r_{oCG} g m_1 (R_S + Z_L \beta) - R_S Z_L r_{oCG} \beta g m_1 g m_2 + s C_{in} [R_S Z_L + R_S r_{oCG} + R_S Z_L r_{oCG} \beta g m_1], \quad (15)$$

and LNA output resistance is given as:

$$R_{OLNA} = \frac{r_{oCS} (R_S + r_{oCG} + R_S r_{oCG} g m_1)}{R_S + r_{oCG} (1 + g m_1 R_S) + r_{oCS} (1 - g m_2 R_S) + r_{oCG} r_{oCS} \beta g m_1 (1 - g m_2 R_S)}, \quad (16)$$

In Eq. 14, the second and third terms in the NF expression account for the noise contributions from the CG and CS devices respectively, while the last term shows the contribution of the N-path filter and the upconverted noise from BB stages. In the NF expression, factor γ accounts for a constant MOSFET noise parameter whose value is derived to be 2/3 for long channel devices. Recent submicron processes tend to exhibit higher values. $A v'$ and $\overline{V_{NP}^2}$ are respectively the loaded voltage gain and the input referred noise of the N-path filter and BB stages at ω_{IF} . $\overline{V_{NP}^2}$ can be derived from (17),(18) as:

$$\overline{V_{NP}^2} = 4 K T R_{SW} |\rho (Z_{SH} 2 \zeta Z_{BB})|^2 +$$

$$4KTRe(Z_{SH})(|\rho 2\zeta Z_{BB}(R_{SW} + Z_{OLNA})|)^2 + 4KTR_F(|\rho \frac{Z_{SH}(R_{SW} + Z_{OLNA})}{1 + A_{BB}}| \frac{2\sqrt{2}}{\pi})^2 +$$

$$(|\rho \frac{Z_{SH}(R_{SW} + Z_{OLNA})}{1 + A_{BB}}| \frac{2\sqrt{2}}{\pi})^2 \overline{V_{N,amp}^2} + (|2\rho\zeta Z_{BB}(R_{SW} + Z_{OLNA} + Z_{SH})| \frac{2\sqrt{2}}{\pi})^2 \overline{V_{N,amp}^2}, \quad (17)$$

where

$$\rho = \frac{(Z_{BBtot} + R_{SW})/Z_{BBtot}}{(R_{SW} + Z_{OLNA})(2\zeta Z_{BB} + Z_{SH}) + Z_{SH}2\zeta Z_{BB}}, \quad (18)$$

and $\overline{V_{N,amp}^2}$ is the input referred noise of the BB amplifier, A_{BB} is the open loop voltage gain of the BB integrator and R_F is the feedback resistor across the BB integrator such that:

$$Z_{BB} = \frac{R_F}{1 + A_{BB}}. \quad (19)$$

The first term of Eq. 17 corresponds to the noise contribution from R_{SW} , the second term to the noise contribution of Z_{SH} , the third term to the noise contribution of R_F , and finally the fourth and fifth terms correspond to the noise contribution from the BB amplifier. As can be observed from Eq.17, the noise contribution from the baseband amplifiers $\overline{V_{N,amp}}$ and R_F is divided by the gain of LNA and therefore has a reduced effect in overall $\overline{V_{NP}}$ value. This leaves R_{SW} and Z_{SH} as main noise contributors in overall $\overline{V_{NP}}$. These values however, can not be changed arbitrarily due to LO driver and LNA power consumption constraints.

One can simplify the NF Eq. 14 by neglecting the effect of parasitic capacitances and CG/CS output impedances. The simplified equation can be given as:

$$F = 1 + (\frac{Z_L(\omega)^2 \gamma g m_1}{A v'^2 R_S})(\frac{1 - g m_2 R_S}{\alpha})^2$$

$$+$$

$$(\frac{Z_L(\omega)^2 \gamma g m_2}{A v'^2 R_S})(\frac{1 + g m_1 R_S}{\alpha})^2 + (\frac{\overline{V_{NP}^2}}{4KTR_S A v'^2})(\frac{1 + g m_1 R_S}{\alpha})^2, \quad (20)$$

where

$$\alpha = 1 + g m_1(R_S + Z_L\beta - Z_L(\omega)R_S\beta g m_2) \quad (21)$$

However, even the simplified form of Eq. 14 offers little intuition about design trade-offs of proposed circuit. Therefore, in the upcoming Section 7, we will utilize the derived equations to constitute a graphical approach for intuitively explaining the design trade-offs.

5.4 | Analysis Validation

To confirm the analytical results in equations 4-21, we designed a transistor level CG-CS LNA based front-end in a 28nm FDSOI CMOS technology, with the following practical values: $g m_1 = 80\text{mS}$, $g m_2 = 30\text{mS}$, $r o_{CG} = 900\Omega$, $r o_{CS} = 1600\Omega$, $R_{SW} = 10\Omega$, $C_{NP} = 10\text{pF}$, $C_F = 1.8\text{pF}$, $C_1 = 300\text{fF}$, $C_2 = 5\text{pF}$, $R_F = 16.6\text{k}\Omega$, $C_{in} = 300\text{fF}$, $C_{GD,CG} = 100\text{fF}$, $C_{out} = C_{out,par} + (C_1 + C_{GD,CG})C_2 / (C_1 + C_{GD,CG} + C_2) = 370 + 100 = 470\text{fF}$, $\overline{V_{NP}^2} = 5 \times 10^{-18} \text{V}^2/\text{Hz}$, $\gamma = 1.1$ and an ideal BB amplifier with open loop voltage gain of 25dB. The values of $g m_1$, $g m_2$, R_{SW} , C_{NP} , C_F , C_1 , C_2 and R_F were chosen while keeping in mind their practically implementable range and design targets(as explained in Section 7) for proposed design while $r o_{CG}$, $r o_{CS}$, C_{in} , C_{out} , $C_{GD,CG}$, $\overline{V_{NP}^2}$ and γ are the estimated values based on transistor modeling in the used FDSOI process. Later in Section 7, front-end will be designed with above design parameters. Results for the LNA input impedance and voltage gain are plotted in Figures 5 and 6, respectively. As can be seen, the analytical and simulated results match quite closely. The small difference in the simulated and analytical results can be attributed to a complex LNA output impedance caused by C_{out} . Any complex impedance present at the LNA output will manifest itself as a bandpass filter response offset from the LO, shifting the maximum gain of the LNA away from LO(20). To avoid overwhelming complexity in derived equations and to make intuitive sense from results,

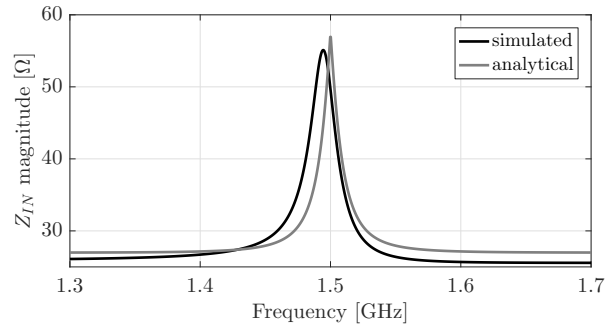


FIGURE 5 Comparison between calculated and simulated input impedance.

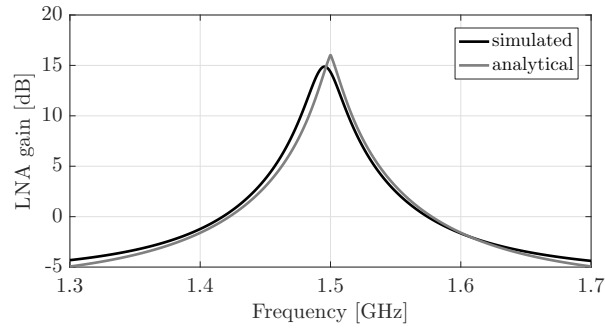


FIGURE 6 Comparison between calculated and simulated LNA gain.

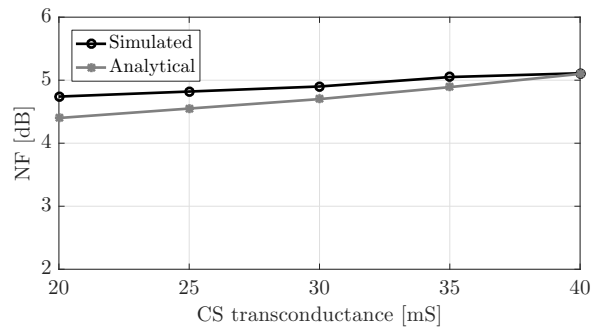


FIGURE 7 Comparison between calculated and simulated NF.

the analytical equations do not take this complex frequency shift effect in account. Therefore, a small deviation from simulated results is expected. For the quantitative noise analysis, we compare the NF results from Eq. 14 with transistor-level front-end simulations. Figure 7 presents the simulated and calculated NF versus CS transconductance gm_2 . It can be seen that the NF is high for higher values of gm_2 . This dependence of NF on gm_2 will be further elaborated in following section.

6 | DESIGN GUIDELINES

The design targets for the proposed front-end are to provide high blocker resilience through improved large signal linearity and dual node blocker voltage attenuation, with acceptable NF and input matching. In this section we examine the proposed front-end to obtain optimum circuit parameter values such as gm_1 , gm_2 , β and Z_L , meeting the design requirements.

We begin by assuming a fixed load impedance of $Z_L = 500\Omega$. This is done to simplify the analysis by reducing additional variables. Later, we will demonstrate how Z_L affects the overall front-end response. With the selected value of Z_L , first, we use Eq. 13 to plot the required feedback factor β for an ideal input match, against different values of gm_1 and gm_2 . The derived β values are plotted in Figure 8. These derived values are then used to calculate the LNA NF in impedance-matched conditions, using Eq. 21. We assume that $V_{NP}^2 = 5 \times 10^{-18} V^2/Hz$ and $\gamma = 1.1$ for the analysis. The resulting NF is plotted for different values of gm_1 and gm_2 in Figure 9.

NF results in Figure 9 demonstrate that a smaller value of gm_2 is desired for reduced NF. We can achieve this smaller gm_2 value by having a smaller aspect-ratio for CS device. However, too small aspect-ratio for the CS device in comparison to the CG reduces the LNA linear output swing range, and consequently lowers the large signal linearity. This is depicted in Figure 10, where the transistor-level simulation results for NF and maximum peak output voltage swing range are plotted against CS transconductance gm_2 . As expected, a smaller gm_2 leads to reduced NF and output peak voltage swing range. The decrease in output swing range can be attributed to a higher saturation voltage (V_{DSAT}) of the CS devices. Consequently, gm_2 cannot be reduced significantly in comparison to gm_1 , without significantly affecting the larger signal linearity of LNA. The choice of gm_2 is thus a trade-off between NF and large signal linearity.

In the next step, we examine the effect of $Z_L(\omega)$ on the front-end performance. In Figure 11, we plot the required value of β for input matching at two different values of $Z_L(\omega)$ values. It can be observed that for higher values of $Z_L(\omega)$, one needs a lower β to achieve input matching. After a certain limit, designing the LNA for lower values of β becomes impractical due to very small values of C_1 . Once C_1 approaches closer to the CG gate-to-drain parasitic capacitance C_{GD} , the effect of C_{GD} is significant and therefore needs to be considered in the effective feedback factor β . Therefore, we propose designing the CG-CS LNA for moderately lower values of $Z_L(\omega_0)$.

In conclusion, based on the above reasoning, we propose designing of capacitive feedback CG-CS amplifier with $gm_2 < gm_1$ and a moderately low value of $Z_L(\omega)$ to ensure practical values for C_1 .

7 | PERFORMANCE EVALUATION

Based on the design guidelines in Section 6, we selected $gm_1 = 80mS$ and a lower $gm_2 = 30mS$ for LNA design. Selection of $gm_2 < gm_1$ is a compromise between large-signal linearity and NF. Detailed diagram of designed circuit is shown in Figure

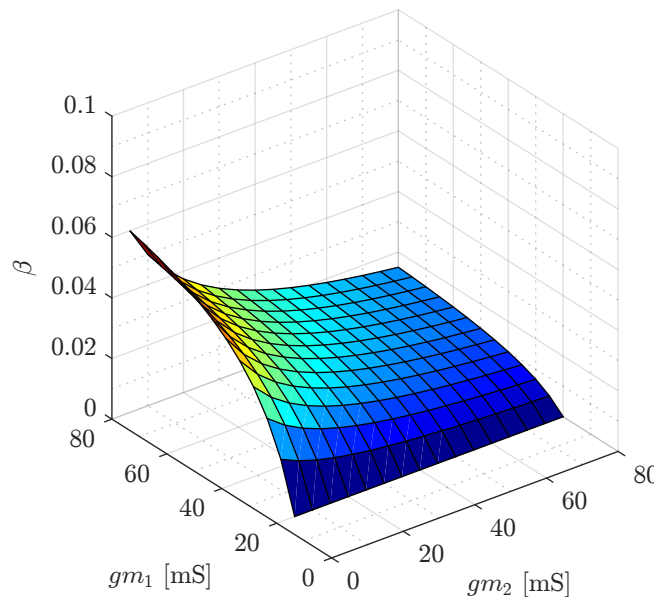


FIGURE 8 Required feedback factor β , for $Z_{IN} = 50\Omega$, for different values of gm_1 and gm_2 .

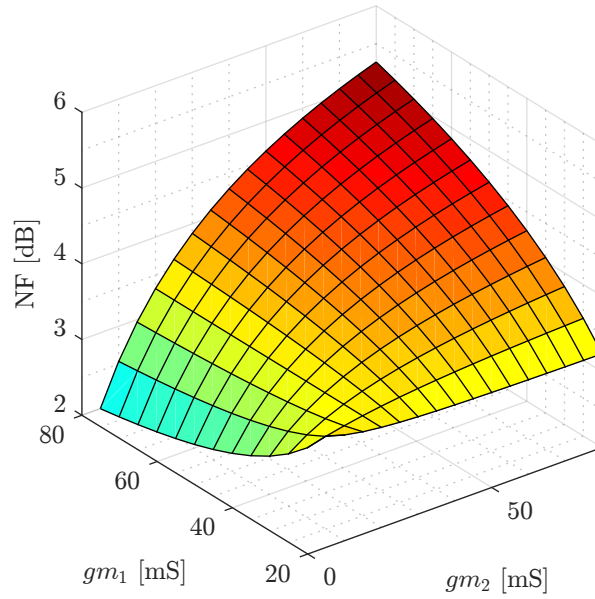


FIGURE 9 Theoretical NF, for $Z_{IN} = 50\Omega$, for different values of gm_1 and gm_2 .

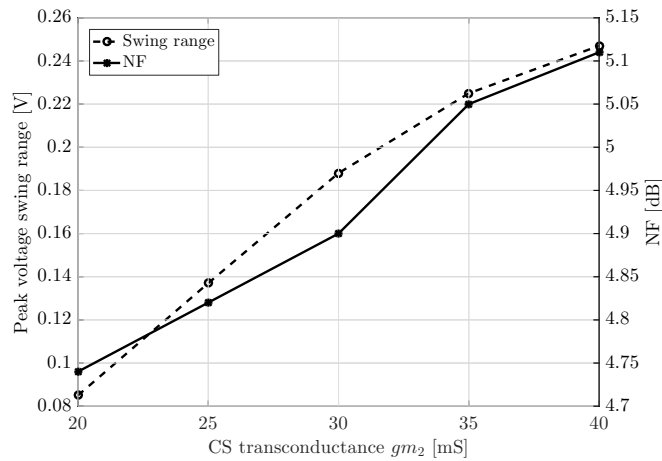


FIGURE 10 Transistor level simulations for output voltage swing range and NF, versus CS transconductance gm_2 .

12 .To maximize output voltage swing range, the output common mode voltage of the LNA was set to half of the supply voltage by implementing the common-mode feedback loop depicted in Figure 2 . A quadrature passive mixer with a switch resistance $R_{SW} = 10\Omega$ together with the baseband capacitance $C_{NP} = 10\text{pF}$ and an ideal differential BB amplifier with Miller capacitance $C_F = 1.8\text{pF}$ formed a first order N-path filter. This $R_{SW} = 10\Omega$ was achieved with transistor width of $12\mu\text{m}$ by the application of proper body-bias in FDSOI process. This reduced the LO buffer sizes and consequently their current consumption to 1mA. The value of feedback resistor R_F was set to $16.5\text{k}\Omega$ to adjust the front-end voltage gain to 15dB. For Additionally, in order to match the pre-layout simulated response more closely to the real measurements, estimated values of key PCB and layout parasitics, pad capacitances, bondwire inductances and s-parameter models of the off-chip RF chokes (L_{ext}) were included in simulations.

The parasitic capacitance associated with the LNA output node can shift the LNA center frequency away from the LO frequency(20). This was corrected by implementing a resistive complex negative feedback from the output node of the baseband differential amplifier, as depicted in Figure 3 (b).

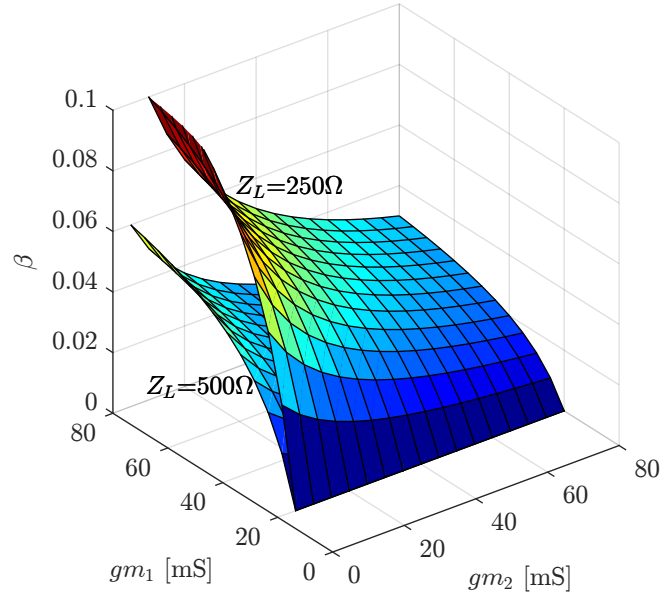


FIGURE 11 Feedback factor β , at $Z_{in} = 50\Omega$, for different values of g_{m1} and g_{m2} . For higher Z_L , a lower value of β is required for input matching.

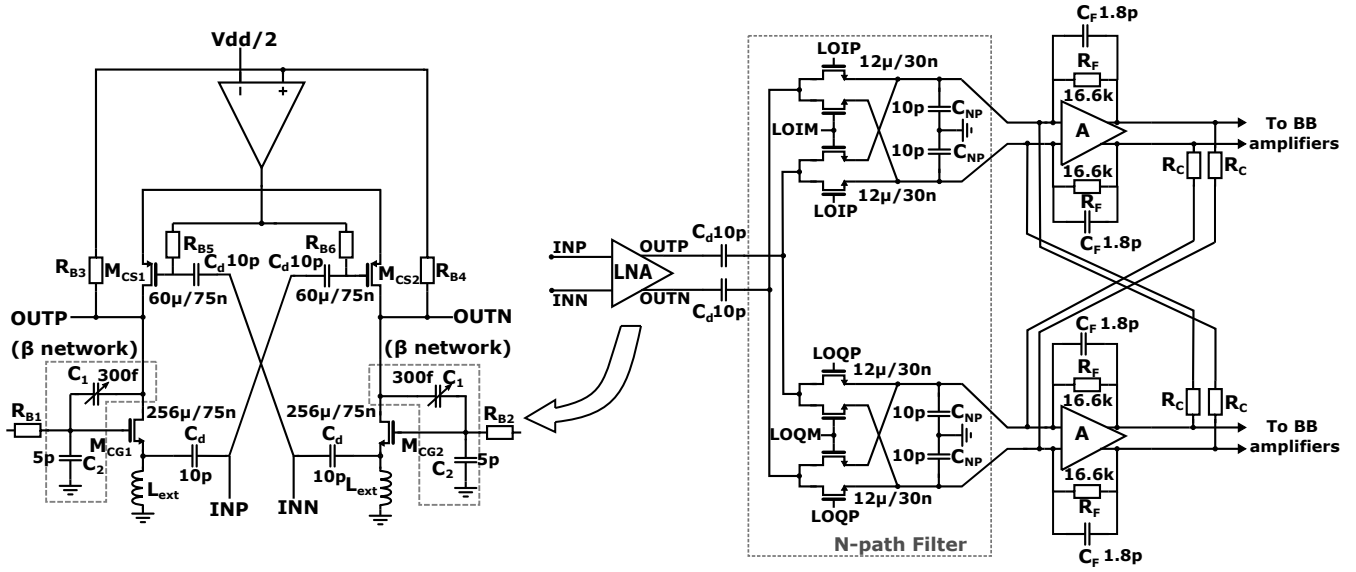


FIGURE 12 Designed circuit for simulations.

The proposed front-end was evaluated in a 28nm fully-depleted silicon-on-insulator (FD-SOI) CMOS process with 1V supply voltage. The front-end is configurable from 0.7-2.7GHz with BB bandwidth of 10MHz and consumes 11.5mA current, excluding LO buffering.

Figure 13 demonstrates the simulated differential Z_{IN} . As can be seen, $Z_{IN} \approx 25\Omega$ at blocker frequencies. Assuming an antenna impedance of 100Ω (differential), this creates the required blocker voltage attenuation. Additionally, we observe $Z_{IN} > 25\Omega$ for the upper end of the 0.7-2.7GHz band. At higher frequencies the effect of parasitics changes the effective feedback factor β and causes a change in Z_{IN} . Figures 14 and 15 show the simulated gain and S_{11} for the proposed front-end. Gain and

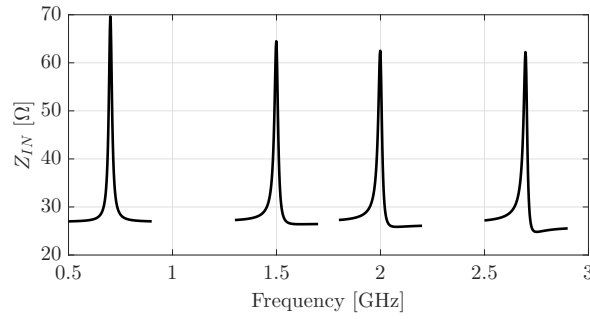


FIGURE 13 Simulated real part of the LNA input impedance Z_{IN} around $f_{LO} = 0.7, 1.5, 2,$ and 2.7 GHz.

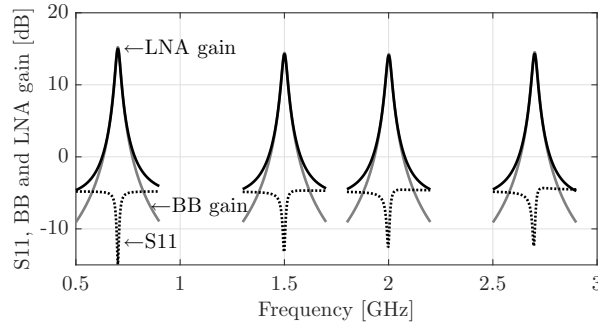


FIGURE 14 Simulated S_{11} , LNA and front-end downconversion gain around $f_{LO} = 0.7, 1.5, 2,$ and 2.7 GHz.

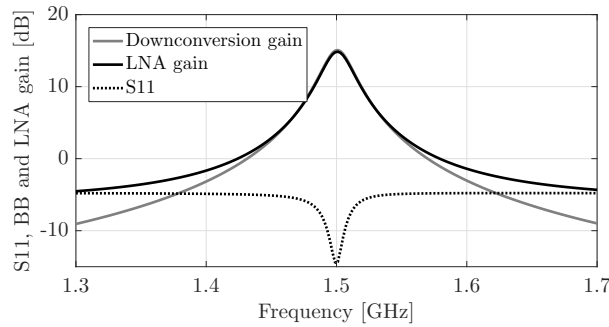


FIGURE 15 Simulated S_{11} , LNA and front-end downconversion gain.

S_{11} have been plotted at four operating frequencies in the 0.7-2.7GHz band, demonstrating the desired configurability. Figure 16 presents the front-end NF and LNA reverse isolation across the whole band of 0.7-2.7GHz. A maximum NF of 5.1dB and minimum reverse isolation of -19dB is observed. As explained in the previous sections, there is a compromise between large signal linearity and NF. Therefore, we choose a moderately high value of NF to have better large signal performance. Further, the reverse isolation results demonstrate atleast 19 dB suppression of LO oscillator leakage to antennas compared to mixer-first receivers. Figure 17 presents the front-end blocker 1dB compression point (BCP) when loaded with a first order N-path response. The simulated results demonstrate the blocker tolerance of -1.5dBm at a 100MHz offset from the LO frequency. Further, in order to quantitatively observe the improvement of BCP thanks to the selective input impedance profile, a CG-CS LNA based RF front-end with flat wideband input matching was designed and simulated for same the voltage gain and baseband bandwidth. Its simulated BCP results are plotted in the same Figure 17. The proposed front-end demonstrates 3.5dB improvement in BCP at a 100MHz offset from the LO frequency, thanks to selective input impedance matching.

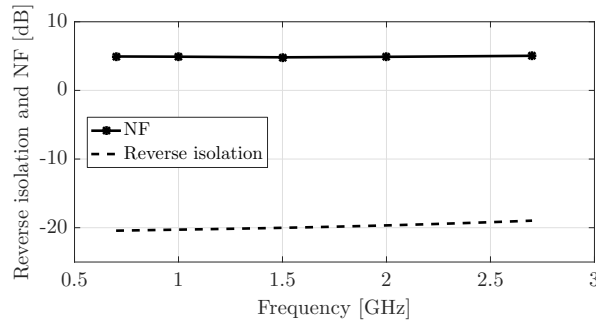


FIGURE 16 Simulated front-end noise figure and LNA reverse isolation for different operating frequencies.

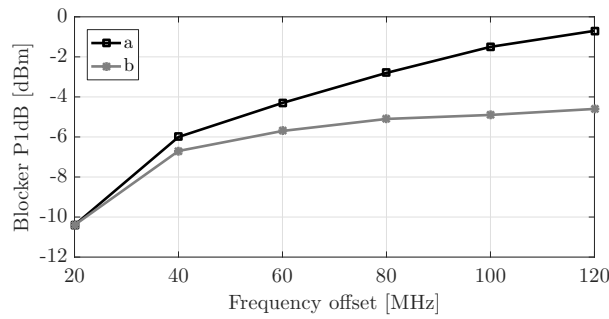


FIGURE 17 (a) Simulated out-of-band blocker compression point (BCP) of the proposed RF front-end and (b) BCP for CG-CS LNA based RF front end with wideband input matching. In comparison to (b), the proposed front-end achieves 3.5dB higher BCP at a 100MHz offset from LO.

Table 1 compares the performance of proposed front-end with other relevant front-end structures with blocker rejection at LNA input. As desired, the front-end achieves competitive large signal linearity even with a reduced power supply and lower power consumption with a simplified passive feedback approach.

8 | CONCLUSION

Emerging wideband RF-to-digital receivers need to operate in the presence of strong OB blockers. These blockers can cause receiver input amplifiers to saturate and therefore make its operation non-linear. In this paper, we have presented a blocker resilient low intrinsic input impedance RF front-end. The front-end achieves this blocker resilience through blocker attenuation at both front-end input and output nodes. This dual attenuation is achieved through tunable N-path filtering at the CG-CS LNA output nodes, which is in turn reflected back to the LNA input through capacitive feedback. The resulting input impedance of RF front-end is lower at blocker frequencies while being matched at desired frequencies, thereby creating additional blocker attenuation at the RF front-end input. Further, a detailed theoretical analysis of proposed architecture is presented which leads to simplified design guidelines.

The front-end is designed for an operating frequency of 0.7 to 2.7GHz, where desired configurability is achieved by tuning the center frequency of the N-path filter through the LO signal. Evaluated in a 28nm FD-SOI, simulated results demonstrate wideband tunable operation in the operating band with maximum a NF of 5.1dB. The front-end achieves -1.5dBm of input BCP and +14dBm of OB IIP3 at a 100MHz frequency offset from the LO frequency. In comparison to relevant front-end architectures (12, 13, 14), where blocker rejection is performed at LNA input, the proposed front-end offers a simplified and passive feedback path. This reduces the possibility of feedback path saturating in presence of large blockers. When compared to traditional CG-CS LNA amplifier based RF front end with wideband input impedance matching, the proposed front-end achieves 3.5dB improvement in blocker compression point (BCP) at a 100MHz offset from the LO frequency.

9 | ACKNOWLEDGEMENTS

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TABLE 1 Front-end performance summary

Parameter	This work ⁷	Interferer reflecting loop LNA(13)	Miller bandpass filters LNA(12)
Operating band (GHz)	0.7-2.7	0.2-1.6	0.05-2.5
Conversion Gain (dB)	15	13-22	38
Power (mW)	11.5	13	20
Supply voltage(V)	1	1.6	1.2
Baseband bandwidth (MHz)	10	20	0.35-20
Process	28nm FDSOI	65nm CMOS	65nm CMOS
Maximum NF (dB)	5.1	3.6	2.9
OB IIP3 (dBm)	+14 ¹	+14.5 ²	+10 ³
BCP (dBm)	-1.5 ⁴	-4 ⁵	0 ⁶

1) First blocker at 100MHz offset from f_{LO} 2) First blocker at 80MHz offset from f_{LO} 3) First blocker at 20MHz offset from f_{LO}
4) Blocker at 100MHz offset from f_{LO} 5) Blocker at 80MHz offset from f_{LO} 6) Blocker at 20MHz offset from f_{LO} 7) Simulated response. δ