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Electronic Quality Improvement of Highly Defective Quasi-Mono Silicon Material by Phosphorus Diffusion Gettering

*Zhengjun Liu, Ville Vähänissi, Hannu S. Laine, Morten Lindeberg, Marko Yli-Koski, and Hele Savin**

Quasi-mono silicon (QM-Si) attracts interest as a substrate material for silicon device processing with the promise to yield single-crystalline silicon quality with multicrystalline silicon cost. A significant barrier to widespread implementation of QM-Si is ingot edge-contamination caused by the seed material and crucible walls during crystal growth. This work aims to recover the scrap material in QM-Si manufacturing with a process easily adaptable to semiconductor device manufacturing. A phosphorus diffusion process at 870 °C for 60 min significantly improves the electronic quality of a QM-Si wafer cut from a contaminated edge brick. The harmonic minority carrier recombination lifetime of the wafer, a key predictor of ultimate device performance, experiences a tenfold increase from 17 to 178 µs, which makes the scrap QM-Si material usable for device fabrication. Local areas with suboptimal (<50 µs) lifetimes remaining can be further improved by a high temperature anneal before the phosphorus diffusion process.

1. Introduction

Due to its abundance and flexible electronic properties, silicon is the work horse material for a wide range of electronics applications, such as integrated circuits (IC), optoelectronics, microelectromechanical systems (MEMS), and photovoltaics (PV). A key aspect of any silicon device processing is the control of both intrinsic and extrinsic defects that can lower the performance of silicon devices even at parts-per-trillion concentrations.[1–5] Single crystalline silicon (sc-Si) typically contains the lowest concentrations of these defects, which makes it the most dominant substrate material within the electronics industry. However, the cost of the sc-Si is high compared to that of other silicon materials, such as multicrystalline silicon (mc-Si). Therefore, the development of cost-effective substrate materials will contribute to the cost reduction for all silicon-based industries.

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The need for cost reduction is particularly imperative for the PV industry due to its commoditized nature. It is estimated that for photovoltaics to play a significant role in mitigating climate change, a two- to tenfold increase in PV manufacturing capacity is needed by 2030.[6] Given that the silicon substrate comprises almost 50% of the capital expenditure of solar cell manufacturing, reducing the capital expenditure of the silicon substrate is a central issue for the PV industry.[7,8] To reduce the cost to the level of mc-Si while keeping the higher performance of sc-Si, a new type of silicon casting method has been proposed in the last decade, called quasi-mono silicon (QM-Si).[9] QM-Si is a casting method which utilizes a single crystalline seeding layer to yield a single crystalline ingot.

A significant issue preventing the widespread application of QM-Si is the low ingot yield. The material loss is mainly attributed to the region with very low minority carrier lifetime, which is typically denoted as the "red zone", at the edge of the QM-Si ingot.[10,11] Minority carrier lifetime plays a crucial role in controlling the performance of silicon semiconductor devices,[12,13] and hence this region is unusable for device processing. Many research groups have identified experimentally and numerically that iron contamination is the main cause of the red zone for casting silicon.[14,15] While the iron contamination is also a problem in traditional mc-Si, it is particularly aggravated for seed-assisted silicon casting due to the back diffusion from the seed,[16–18] which leads to an extended red zone for the QM-Si.

Within silicon, iron can be present in either precipitated or dissolved state. The dissolved state is typically the more detrimental of the two, and consists mostly of interstitial iron.[19] An effective way to decrease the interstitial iron concentration of red zone wafers is phosphorus diffusion gettering (PDG). Several researches have shown that PDG is effective in decreasing the iron contamination in sc-Si and mc-Si wafers.[20–23] However, gettering in QM-Si is still in its infancy,[24,25] and in particular, no reports of red zone wafers exhibiting promising device potential (high minority charge carrier lifetime) have been made. Furthermore, the thermal stability of the gettered iron has not been studied.

This work solves the red zone problem of QM-Si wafers by implementing a PDG process, which may take place simultaneously during phosphorus doping in semiconductor device fabrication, particularly if combined with an etch-back process.[26] The PDG behavior is analyzed for QM-Si wafers across the solidification direction from the highly contaminated bottom

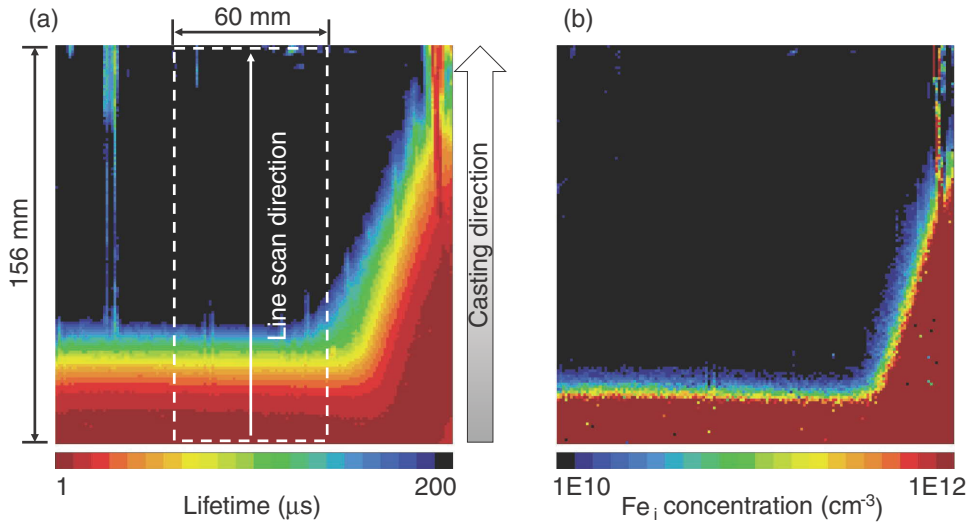

Figure 1. a) Minority carrier lifetime map of a QM-Si wafer with the red zone and b) the corresponding interstitial iron concentration map.

region of the ingot. In addition, we show a method to improve the thermal stability of QM-Si wafers during post-PDG high-temperature processing.

2. Results

Figure 1 shows the minority carrier lifetime map and the corresponding interstitial iron concentration ([Fe_i]) map of a typical red zone QM-Si wafer used in this work. An anti-correlation of [Fe_i] and lifetime is evident. The high [Fe_i] near the bottom and right edge is a result of the long (≈24 h) and high temperature (starting above 1400 °C) ingot crystallization and cooling process, during which iron can diffuse from the seed layer (bottom edge) and the crucible wall (right edge). As the solidification begins from the ingot bottom, the bottom part of the ingot remains at a higher temperature for a longer time, which gives more time for iron to diffuse. This leads to the red zone narrowing along the casting direction, as seen in Figure 1a,b.

To evaluate the minority carrier lifetime development as a function of ingot height and the corresponding iron gettering behavior, line scans were taken across the wafers. The characterized area is within the dashed line frame shown in Figure 1a. At each scanned height the lifetime value was obtained by averaging the values at the same height over a 60 mm wide region.

In order to evaluate the effect of the PDG process, **Figure 2** compares the minority carrier lifetime and interstitial iron concentration scan along the wafer height of a QM-Si wafer, which experienced the PDG process and that of a QM-Si wafer without any gettering process as a reference. For the reference wafer, a low minority carrier lifetime region (<100 µs) is present at the bottom region which extends up to 45 mm. Then the lifetime increases gradually and stabilizes at ≈160 µs until a wafer height of around 65 mm, above which a uniform lifetime distribution is observed.

The lifetime line scan profile of the QM-Si wafer after the PDG process shows significant lifetime improvement compared to that without the gettering process over the whole

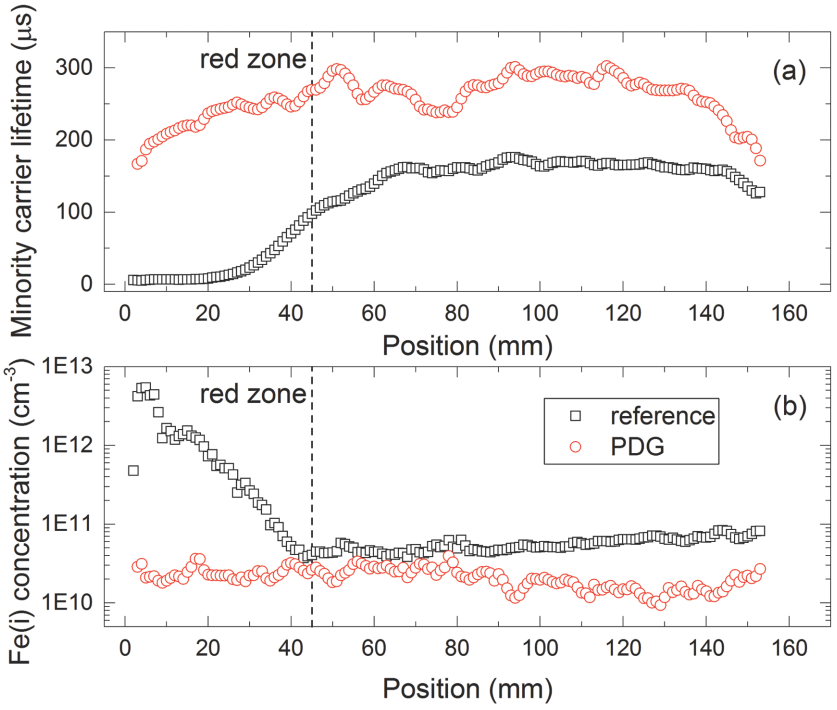

Figure 2. Line scans of a) minority carrier lifetime and b) interstitial iron concentration along the wafer height of the QM-Si wafers without gettering process and experienced the PDG process.

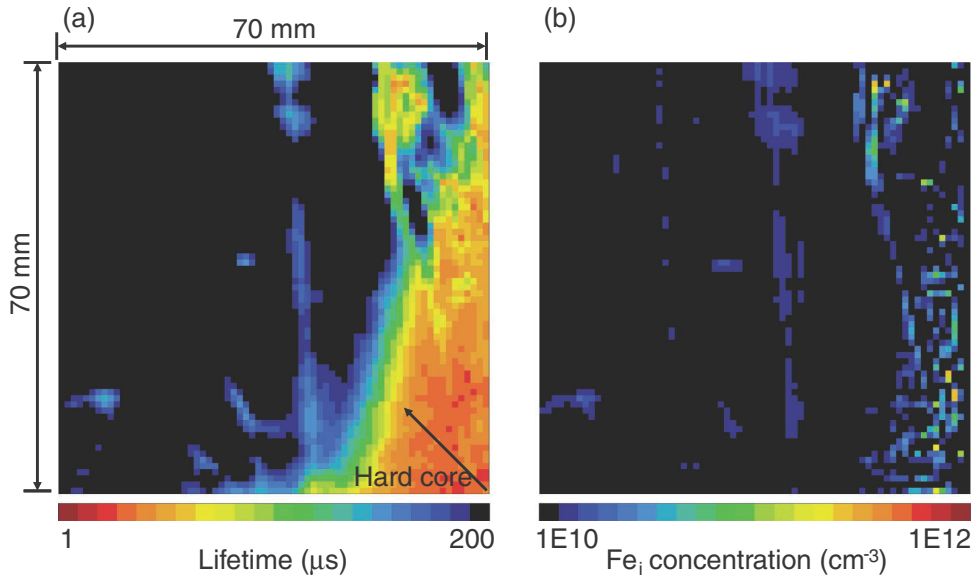

Figure 3. a) Minority carrier lifetime map and b) the corresponding interstitial iron concentration map of the corner region of the QM-Si wafer after the PDG process. Note the different length scale from Figure 1.

range of the wafer height in the characterized region. After the PDG process, the lifetime distribution is relatively uniform across the wafer height. A tremendous lifetime improvement is observed at the wafer bottom and the red zone is successfully removed from the characterized region. The line scan of the interstitial iron concentration verifies that the PDG process is effective in decreasing the interstitial iron level. By applying the PDG process, the full wafer harmonic minority carrier lifetime, a solid predictor of PV device potential,[13,27] experienced a ten-fold increase from 17 to 178 μs. This result promises device performance improvement without introducing significant extra processes to the manufacturing if the phosphorus doping profile optimization is taken into account in the PDG. Given that the extended red zone near the ingot bottom can be recovered, the main cause of the material loss of a QM-Si ingot is prevented.

The interstitial iron concentration is not the sole factor that determines the lifetime and the usability of the QM-Si wafer. **Figure 3** displays lifetime and [Fe_i] in the corner region of the QM-Si wafer after the PDG process. A small red zone still persists in the lifetime map, while the interstitial iron concentration has been decreased to a relatively uniform level. The region with lifetime lower than 50 μs is denoted as the hard core red zone. The presence of the hard core could be an indication of iron precipitation, as these corner regions are known to be ideal precipitation sites for iron and other transition metals.[28,29] Iron precipitates are known to cause charge carrier recombination,[30,31] and are known to be difficult to getter via PDG.[32–34] They can also dissolve during thermal processing following the PDG, which is typical in, e.g., silicon solar cell processing,[35] which increases their harmful impact.[36]

In order to facilitate the hard core removal, a modified PDG process was implemented. In particular, a high-temperature anneal 900–1100 °C in temperature and 10–30 min in length was performed prior to the PDG step.[37–40] The purpose of this step is to dissolve iron precipitates and leave a majority of iron atoms in a dissolved, mobile state, in which they can easily be gettered by the PDG.

Figure 4 shows the hard core width of the QM-Si wafers after the high-temperature anneal and PDG. To observe changes in the wafer bulk quality, the emitter was etched and surface was passivated with atomic layer deposition (ALD)-grown aluminum oxide (Al_2O_3) prior measurements. The pre-PDG high-temperature anneal has a distinct positive impact on the detrimental red zone: after PDG, the hard core width follows a decreasing trend with increasing dissolution temperature. This observation agrees with the hypothesis that in the hard core region, iron precipitates are a major defect that limits the usability of the QM-Si, and the dissolution anneal before the

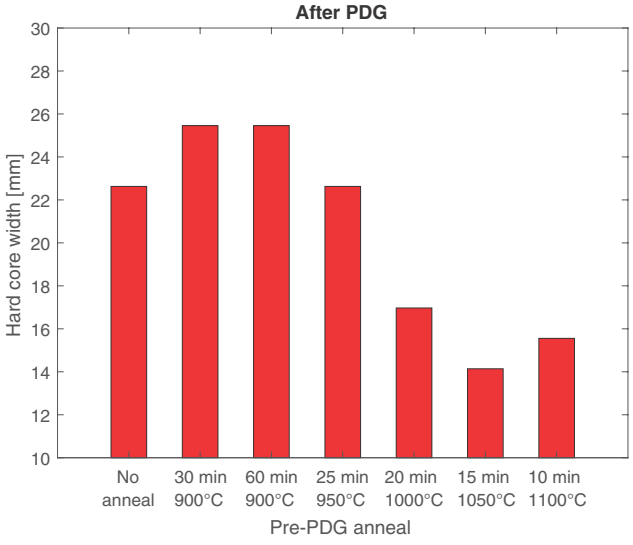

Figure 4. Hard core (<50 μs region) width of the QM-Si wafers after PDG with the indicated pre-PDG dissolution anneal temperatures and durations.

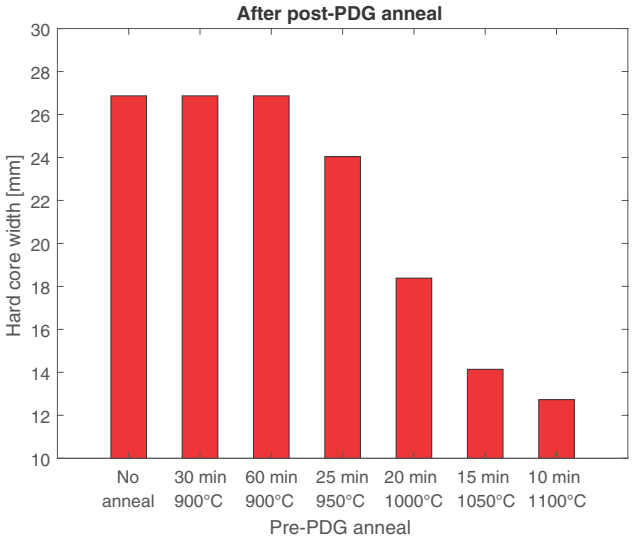

Figure 5. Hard core (<10 µs region) width of the QM-Si wafers after the post-PDG anneal at 900 °C for 60 min with the pre-PDG anneal temperatures and durations.

PDG facilities the hard core reduction. At best, the dissolution anneal is able to cut the hard core width to almost half, from the original 23 mm down to ≈15 mm.

To investigate the tolerance of the achieved benefit during high-temperature processing after the PDG, the wafers experienced an emitter etch and a 900 °C, 60 min oxidation anneal, which dissolved any remaining precipitates within the bulk of the wafers. This process reveals the effectiveness of the combined high-temperature anneal and PDG process in removing both interstitial and precipitated iron from the wafer bulk. **Figure 5** shows that the positive trend in the hard core width reduction is maintained. Here we use 10 µs as the benchmark for the hard core, due to the lower surface passivation quality of the thermal oxide. Similarly as in Figure 4, the pre-PDG anneal reduces the hard core width to less than half of its original width. In conclusion, even the residual contamination left after the effective PDG process can be further mitigated.

3. Conclusion

This work presents an easily adaptable process to significantly reduce material loss during QM-Si processing. A significant fraction of QM-Si ingots are typically discarded as unusable due to iron contamination from the seed layer and the crucible wall.[10,11,14,15] A PDG process with phosphorus diffusion at 870 °C for 60 min followed by a low temperature anneal (LTA) significantly increased the harmonic minority carrier lifetime of a QM-Si wafers cut directly from the edge of an ingot from 17 to 178 µs.

Additionally, we showed that the detrimental effect of iron precipitation is highest near the bottom corner of the crucible, resulting in a small, very low lifetime region after post-PDG high temperature processing. This local degradation could be mitigated by adding a high-temperature anneal 900–1100 °C in temperature and 10–30 min in length prior to the PDG step.

4. Experimental Section

The wafers used in this work originated from the scrap material located at the bottom edge region, which was typically discarded as unusable, of a commercial-scale p-type QM-Si ingot. All the wafers were cut vertically from the ingot with the thickness of 200 µm and area of 156 mm × 156 mm, with the red zone along the wafer bottom and partly one side. The selected wafers were neighboring wafers that covered an ingot width of several millimeters, providing comparable starting quality for all specimen.

Figure 6 describes the process flow and temperature–time profile of the experiment. Before processing, possible surface contamination was removed by cleaning the wafers in an RCA-1 solution, followed by a brief dip in a dilute hydrofluoric acid (HF) solution. After the cleaning, the wafers were subjected to the PDG process. The PDG process started with the spin coating of a Filmtronics P509 solution as the phosphorus source. The phosphorus diffusion took place in a nitrogen atmosphere at 870 °C for 60 min, after which the wafers were cooled down to 700 °C at 4 °C min^{-1} and annealed at 700 °C for 90 min. This process created a heavily phosphorus doped layer with enhanced iron solubility, which consequently generated a strong driving force for iron segregation toward the n^+ region, where iron was significantly less detrimental.[22] The phosphorus diffusion temperature and duration provided an optimal tradeoff between the dissolution of iron precipitates and thermal degradation of the silicon.[41] The moderate ramp rate from phosphorus diffusion to LTA prevented the formation of small

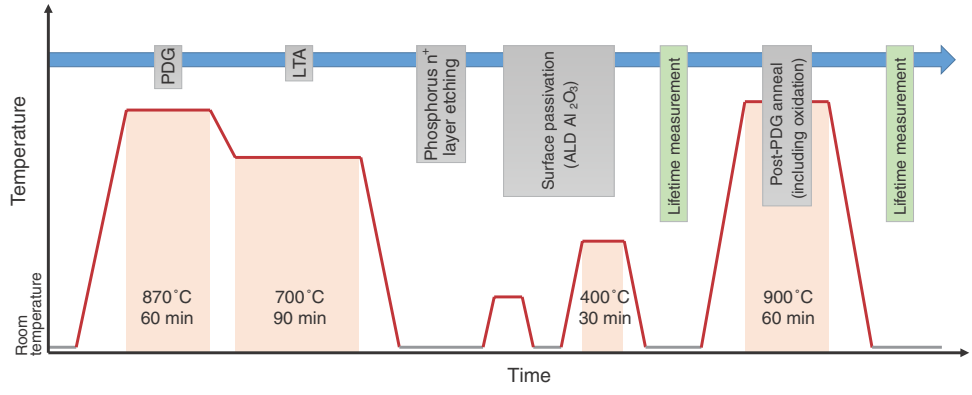

Figure 6. Process flow and temperature-time profile of the PDG process and thermal stability test experiment.

deleterious iron precipitates.[36] The 700 °C LTA enhanced the solubility segregation toward the highly doped emitter at lower temperatures and allowed the equilibrium segregation condition to be reached.[42,43] The resulting sheet resistance of the phosphorus n^+ layer was measured with a four-point probe to be ≈25 Ω sq^{-1}. The phosphorus depth profile was previously probed via secondary ion mass spectroscopy in a similarly manufactured emitter in ref. [44] (see Figure 3b).

In order to measure the minority carrier lifetime from the bulk silicon, the phosphorus glass was removed from the wafer surface in a dilute HF solution and the phosphorus doped n^+ layer was removed in an HNO_3:CH_3COOH:HF solution. Subsequently, the wafer surface was passivated by ALD Al_2O_3. The thickness of the Al_2O_3 film was ≈22 nm, and the passivation layer was annealed in a nitrogen atmosphere at 400 °C for 30 min to activate the passivation, resulting in a surface recombination velocity of ≈7 cm s^{-1}.[45]

The minority carrier lifetimes of all samples were characterized with microwave-assisted Photoconductance Decay (μ-PCD) method using Semilab WT-85 scanner with a 905 nm excitation laser, 200 ns pulse length, 1 mm^2 pulse spot size, and 1.2×10^{13} photons per pulse. The interstitial iron concentration was calculated by the change in lifetime before and after the dissociation of Fe-B pairs by illumination.[46] The μ-PCD method allowed mapping lifetime and interstitial iron concentration of the full wafer.

To study the thermal stability of the iron contamination after gettering, surface passivation was removed from all the tested samples and the samples were subjected to a post-PDG anneal at 900 °C for 60 min including a 40 min thermal oxidation step. Then the minority carrier lifetime and interstitial iron concentration were recharacterized with the same method as indicated above, with the thermal silicon dioxide (SiO_2) serving as the surface passivation layer. Prior to the lifetime measurement, −800 nC cm^{-2} of negative corona charge was deposited on the oxide to enhance the surface passivation, resulting to a surface recombination velocity of ≈40 cm s^{-1}.

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Keywords

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[1] T. Buonassisi, A. A. Istratov, M. Matthew, B. Lai, Z. Cai, S. M. Heald, E. R. Weber, *Nat. Mater.* **2005**, *4*, 676.
[2] J. R. Davis, A. Rohatgi, R. H. Hopkins, P. D. Blais, P. Rai-Choudhury, J. R. McCormick, H. C. Mollenkopf, *IEEE Trans. Electron Devices* **1980**, *27*, 677.
[3] G. Coletti, P. C. P. Bronsveld, G. Hahn, W. Warta, D. Macdonald, B. Ceccaroli, K. Wambach, N. Le Quang, J. M. Fernandez, *Adv. Funct. Mater.* **2011**, *21*, 879.
[4] B. O. Kolbesen, W. Bergholz, H. Wendt, *Mater. Sci. Forum* **1989**, *38–41*, 1.
[5] E. P. Burte, W. Aderhold, *Solid-State Electron.* **1997**, *41*, 1021.
[6] D. B. Needleman, J. R. Poindexter, R. C. Kurchin, I. M. Peters, G. Wilson, T. Buonassisi, *Energy Environ. Sci.* **2016**, *9*, 2122.
[7] T. Saga, *NPG Asia Mater.* **2010**, *2*, 96.
[8] D. M. Powell, R. Fu, K. Horowitz, P. A. Basore, M. Woodhouse, T. Buonassisi, *Energy Environ. Sci.* **2015**, *8*, 3395.
[9] N. Stoddard, B. Wu, I. Witting, M. C. Wagener, Y. Park, G. A. Rozgonyi, R. Clark, *Solid State Phenom.* **2008**, *131–133*, 1.
[10] T. U. Nærland, L. Arnberg, A. Holt, *Prog. Photovoltaics* **2009**, *17*, 289.
[11] M. C. Schubert, J. Schön, F. Schindler, W. Kwapil, A. Abdollahinia, B. Michl, S. Riepe, C. Schmid, M. Schumann, S. Meyer, W. Warta, *IEEE J. Photovoltaics* **2013**, *3*, 1250.
[12] H. J. Queisser, E. E. Haller, *Science* **1998**, *281*, 5379.
[13] R. Jayakrishnan, S. Gandhi, P. Suratkar, *Mater. Sci. Semicond. Process.* **2011**, *14*, 223.
[14] B. Gao, S. Nakano, K. Kakimoto, *Cryst. Growth Des.* **2012**, *12*, 522.
[15] Z. Li, L. Liu, G. Zhou, *J. Appl. Phys.* **2014**, *115*, 174903.
[16] G. Zhong, Q. Yu, X. Huang, L. Liu, *J. Cryst. Growth* **2014**, *402*, 65.
[17] M. Trempa, C. Reimann, J. Friedrich, G. Müller, L. Sylla, A. Krause, T. Richter, *J. Cryst. Growth* **2015**, *429*, 56.
[18] D. Zhu, L. Ming, M. Huang, Z. Zhang, X. Huang, *J. Cryst. Growth* **2014**, *386*, 52.
[19] A. A. Istratov, H. Hieslmair, E. R. Weber, *Appl. Phys. A* **1991**, *69*, 13.
[20] V. Vähänissi, M. Yli-Koski, A. Haarahiltunen, H. Talvitie, Y. Bao, H. Savin, *Sol. Energy Mater. Sol. Cells* **2013**, *114*, 54.
[21] A. Haarahiltunen, H. Savin, M. Yli-Koski, H. Talvitie, J. Sinkkonen, *J. Appl. Phys.* **2009**, *105*, 023510.
[22] H. Talvitie, V. Vähänissi, A. Haarahiltunen, M. Yli-Koski, H. Savin, *J. Appl. Phys.* **2011**, *109*, 093505.
[23] A. Bentzen, A. Holt, *Mater. Sci. Eng., B* **2009**, *159*, 228.
[24] B. P. Rand, J. Genoe, P. Heremans, J. Poortmans, *Prog. Photovoltaics* **2012**, *15*, 659.
[25] R. Søndenå, K. E. N, G. Stokkan, H. Dalaker, T. Lehmann, L. Arnberg, M. Di Sabatino, in *Proc. 31st European PV Solar Energy Conf. and Exhibition* (Ed: S. Rinck, N. Taylor, P. Helm), WIP Wirtschaft und Infrastruktur GmbH & Co. Planungs-KG, München **2015**, p. 571.
[26] H. Wagner, A. Dastgheib-Shirazi, B. Min, A. E. Morishige, M. Steyer, G. Hahn, C. del Cañizo, T. Buonassisi, P. P. Altermatt, *J. Appl. Phys.* **2016**, *119*, 185704.
[27] T. Buonassisi, A. A. Istratov, M. D. Pickett, M. A. Marcus, T. F. Ciszek, E. R. Weber, *Appl. Phys. Lett.* **2006**, *89*, 042102.
[28] M. Seibt, R. Khalil, V. Kveder, W. Schröter, *Appl. Phys. A* **2009**, *96*, 235.
[29] W. Kwapil, J. Schön, W. Warta, M. C. Schubert, *IEEE J. Photovoltaics* **2015**, *5*, 1285.
[30] M. Negoita, T. Tan, *J. Appl. Phys.* **2003**, *94*, 5064.
[31] D. P. Fenning, J. Hofstetter, M. I. Bertoni, G. Coletti, B. Lai, C. del Cañizo, T. Buonassisi, *J. Appl. Phys.* **2013**, *113*, 044521.
[32] A. E. Morishige, M. A. Jensen, J. Hofstetter, P. X. T. Yen, C. Wang, B. Lai, D. P. Fenning, T. Buonassisi, *J. Appl. Phys.* **2016**, *108*, 202104.
[33] A. E. Morishige, H. S. Laine, J. Schön, A. Haarahiltunen, J. Hofstetter, C. del Cañizo, M. C. Schubert, H. Savin, T. Buonassisi, *Appl. Phys. A* **2015**, *120*, 1357.
[34] J-F. Lelièvre, J. Hofstetter, A. Peral, I. Hoces, F. Recart, C. del Cañizo, *Energy Procedia* **2011**, *8*, 257.
[35] T. Buonassisi, A. A. Istratov, S. Peters, C. Ballif, J. Isenberg, S. Riepe, W. Warta, R. Schindler, G. Willeke, Z. Cai, B. Lai, E. R. Weber, *Appl. Phys. Lett.* **2005**, *87*, 121918.
[36] D. P. Fenning, A. S. Zuschlag, M. I. Bertoni, B. Lai, G. Hahn, T. Buonassisi, *J. Appl. Phys.* **2013**, *113*, 214504.
[37] G. F. Martins, P. Macdonald, T. Burton, R. S. Bonilla, P. R. Wilshaw, *Energy Procedia* **2015**, *77*, 607.

[38] B. Michl, J. Schön, W. Warta, M. C. Schubert, *IEEE J. Photovoltaics* **2013**, *3*, 635.
[39] V. Osinniy, A. Nylandsted Larsen, E. Hvidsten Dahl, E. Enebakk, A.-K. Søiland, R. Tronstad, Y. Safir, *Sol. Energy Mater. Sol. Cells* **2012**, *101*, 123.
[40] D. Macdonald, S. P. Phang, F. E. Rougieux, S. Y. Lim, D. Paterson, D. L. Howard, M. D. de Jonge, C. G. Ryan, *Semicond. Sci. Technol.* **2012**, *27*, 125016.
[41] D. Macdonald, A. Cuevas, in *Proc. 16th European Photovoltaic Solar Energy Conf.* (Ed: H. Scheer), James & James, London **2000**, p. 1707.
[42] S. Joonwichien, I. Takahashi, S. Matsushima, N. Usami, *Energy Procedia* **2014**, *55*, 203.
[43] M. Rinio, A. Yodyunyong, S. Keipert-Colberg, Y. P. B. Mouafi, D. Borchert, A. Montesdeoca-Santana, *Prog. Photovoltaics* **2011**, *19*, 165.
[44] V. Vähänissi, A. Haarahiltunen, H. Talvitie, M. Yli-Koski, H. Savin, *Prog. Photovoltaics* **2013**, *21*, 1127.
[45] G. von Gastrow, S. Li, M. Putkonen, M. Laitinen, T. Sajavaara, H. Savin, *Appl. Surf. Sci.* **2015**, *357*, 2402.
[46] A. Haarahiltunen, H. Väinölä, M. Yli-Koski, E. Saarnilehto, J. Sinkkonen, *ECS Meeting* **2004**, *5*, 135.