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A 30-dBm Class-D Power Amplifier with On/Off Logic for an Integrated Tri-Phasing Transmitter in 28-nm CMOS

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***Abstract*— This paper presents an eight-unit class-D power amplifier (PA), implemented in 28-nm CMOS. The PA is designed to utilize tri-phasing modulation, which combines coarse-amplitude polar modulation with fine-resolution outphasing components. This new technique enables achieving the back-off efficiency of multilevel outphasing without linearity-degrading discontinuities in the output waveform. Each PA unit contains a cascoded output stage with a 3.6-V supply voltage, and on/off logic enabling multilevel operation controlled by low-voltage signals. The PA achieves a peak output power of 29.7 dBm with a 34.7% efficiency, and is verified to operate with aggregated LTE signals at bandwidths up to 60 MHz at 1.7-GHz carrier frequency.**

***Index Terms*— CMOS integrated circuits, outphasing, power amplifiers, radio transmitters, tri-phasing**

I. Introduction

One of the fundamental challenges in designing radio transmitters and their power amplifiers (PA) is achieving high power efficiency without compromising linearity. This goal, in conjunction with the development towards increasingly digital-intensive circuit solutions, favors utilizing highly efficient, nonlinear switch-mode PAs. With such PAs, amplitude modulation requires discarding the conventional Cartesian transmitter structure in favor of alternative architectures. One of these architectures is outphasing, which produces amplitude modulation by altering the phase offset between two constant-envelope signal components. While enabling the use of efficient nonlinear PAs, outphasing transmitters nonetheless suffer from declining efficiency in power back-off.

Previously, improved back-off efficiency has been achieved with multilevel outphasing, in which the output amplitude is modulated by both a phase offset and discrete amplitude levels [1]. However, we have observed that amplitude-level transitions in multilevel outphasing cause inherent discontinuities in the output waveform, degrading the transmitter linearity. In order to eliminate this degradation while retaining the efficiency improvement, we have developed a new transmitter architecture

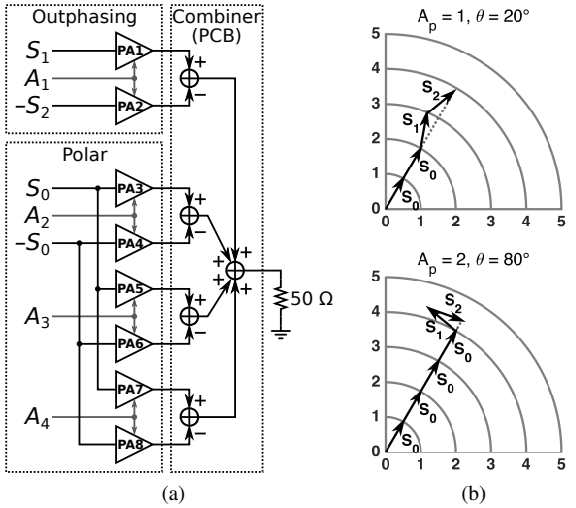


Fig. 1. (a) Block diagram of the designed tri-phasing PA system. (b) Vector illustration of the tri-phasing concept.

called tri-phasing. By combining coarse-amplitude polar modulation with fine-resolution outphasing components, tri-phasing achieves the back-off efficiency of multilevel outphasing without discontinuities at amplitude-level transitions. Thus, the new architecture merges the advantages of outphasing and multilevel outphasing, particularly high linearity and back-off efficiency.

This paper presents a class-D PA implemented in 28-nm CMOS, designed to operate as part of a tri-phasing transmitter. In addition to being the first tri-phasing PA, our circuit also contains the first measured implementation of the on/off logic concept introduced in [2]. The PA achieves a peak output power of 29.7 dBm with an efficiency of 34.7% at 1.77 GHz, and is verified to operate at a 60-MHz modulated signal bandwidth. The paper is organized as follows: Section II presents the concept of tri-phasing and the PA-system structure. Section III describes the PA design in detail, followed by measurement results in

Section IV. Section V concludes the paper.

II. Tri-Phasing PA System

This section introduces the concept of tri-phasing, a technique to achieve the back-off efficiency of multilevel outphasing with superior linearity. The block diagram of our tri-phasing PA system is depicted in Fig. 1(a). All eight class-D PA units are integrated on a single chip, and the power combiner is implemented with coupled transmission lines on PCB. The PA units are divided into polar and outphasing sections consisting of three and one PA pairs, respectively. The polar section provides coarse amplitude modulation by altering the number of active PA pairs. The constantly active outphasing PA pair enables fine amplitude resolution between polar steps by varying the phase difference between input signals S_1 and S_2. Due to the voltage-subtracting characteristic of the power combiner, one input signal in each PA pair is inverted. The signal construction in tri-phasing is illustrated with vectors in Fig. 1(b).

The phase-modulated tri-phasing signal components are

$$S_0(t) = \cos(\omega t + \phi(t)) \tag{1}$$

$$S_1(t) = \cos(\omega t + \phi(t) + \theta(t)) \tag{2}$$

$$S_2(t) = \cos(\omega t + \phi(t) - \theta(t)), \tag{3}$$

where ω is the angular carrier frequency, $\phi(t)$ is the polar phase, and $\theta(t)$ is the outphasing angle. When the number of active polar PA pairs is $A_p(t)$, the output signal is

$$S_{out}(t) = 2A_p(t)S_0(t) + S_1(t) + S_2(t). \tag{4}$$

By substituting (1), (2) and (3), we obtain

$$S_{out}(t) = 2[A_p(t) + \cos(\theta(t))]\cos(\omega t + \phi(t)). \tag{5}$$

As shown by (5), the phase modulation is defined by the polar phase, while the amplitude modulation is a combination of coarse polar and fine outphasing elements. When a coarse amplitude level is crossed, one polar PA pair is switched on or off, and the outphasing angle instantaneously shifts from 0° to 90° or vice versa. Ideally, this leads to smooth transitions with no abrupt change in waveform even when harmonic components are present, unlike in multilevel outphasing. The number of active PA pairs at any given output amplitude is equal between the two architectures, ideally leading to equal efficiency.

III. PA-Unit Design

In this section, we describe the design details of the PA unit, shown as a schematic in Fig. 2. The output stage has a cascoded class-D structure implemented with 1.8-V thick-oxide transistors. Thus, the output voltage is always divided between two transistors, which enables using a supply voltage of 3.6 V. Switch-mode operation requires the gate voltages of M_1 and M_4 to swing between 0–1.8 V and 1.8–3.6 V, respectively. Such voltages are provided by the driver stages (DRV), each of which consists of four inverters with increasing transistor sizes. Because the PA is designed to operate with input signals generated in the 1.0-V supply domain, DC-block capacitors and resistors are employed for biasing. The 0.9-V and 2.7-V bias voltages are generated by on-chip inverters with feedback resistors, not included in the schematic.

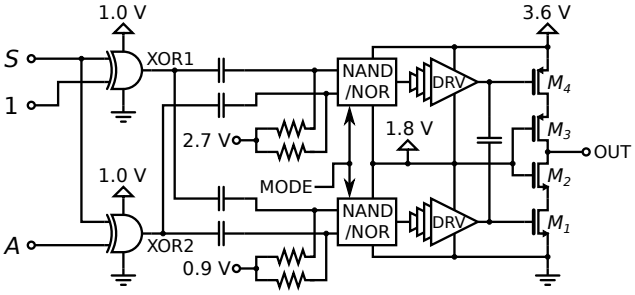


Fig. 2. Simplified schematic of the PA unit.

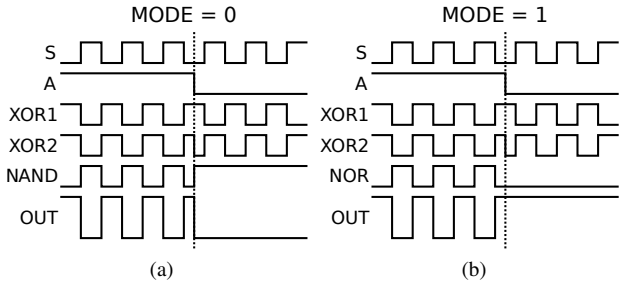


Fig. 3. Waveforms illustrating the on/off logic operation when the NAND/NOR gates are in (a) NAND mode; (b) NOR mode.

In order to operate as an integrated part of a tri-phasing transmitter, each PA unit is required to switch its output on and off during transmission according to the 1.0-V domain signal A. For this purpose, the circuit includes on/off logic developed from the concept presented in [2]. This solution enables generating the output-stage gate voltages in both on and off states in a manner that allows constant bias voltages and quick switching between the states. In the presented implementation, the on/off logic consists of two XOR gates in 1.0-V domain and NAND/NOR gates in 0–1.8-V and 1.8–3.6-V domains. The NAND/NOR gates of each PA unit can be individually configured to operate as NAND or NOR gates by a single control bit (MODE).

The operation principle of the on/off logic is illustrated by example waveforms in Fig. 3. The input signals of the two XOR gates are a phase-modulated rail-to-rail RF signal S, a constant logical one, and an amplitude bit A.

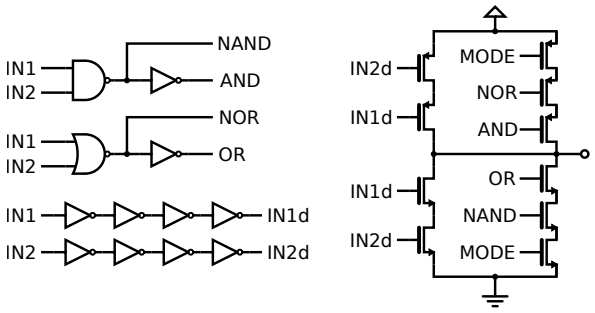


Fig. 4. Schematic of the NAND/NOR gate.

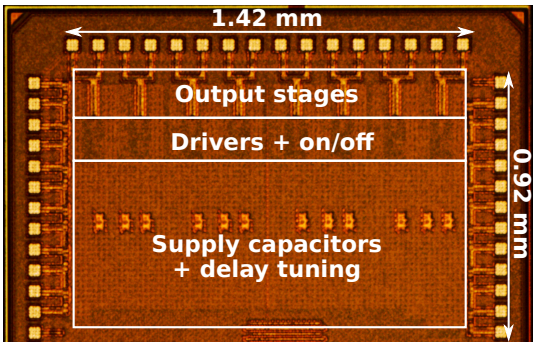
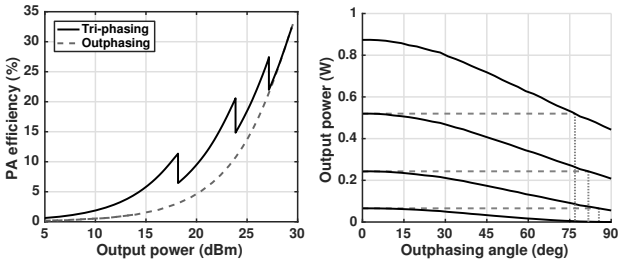


Fig. 5. Die micrograph of the PA.



(a) (b)

Fig. 6. CW measurement results at 1.7 GHz: (a) efficiency as a function of output power; (b) output power as a function of outphasing angle.

The XOR gates produce equally delayed output signals that are identical to each other when $A = 1$ and inverse when $A = 0$. These two signals, after biasing with DC-block capacitors and resistors, are fed into NAND/NOR gates. In the case of identical inputs, the NAND/NOR gates reproduce the signal at the output. With inverse signals, the outputs of these blocks are constant, and thus the output stage is switched off. The control bit MODE defines whether the PA-unit output voltage is high or low in the off state. This flexibility enables optimal spectral performance with both voltage-adding and subtracting power combiners [3].

The schematic of the NAND/NOR gate is presented in Fig. 4. The primary design goal is to minimize timing differences between the two operation modes and thus optimize linearity when the modes are different between PA units. The input signals are fed into NAND and NOR gates, whose outputs are also inverted. In addition, chains of four inverters are employed to approximate the delay of the aforementioned gates. In the on state, when IN1d and IN2d are identical, the core circuit on the right side of Fig. 4 operates as an inverter. In the off state, when IN1d is the inverse of IN2d, the AND and NOR signals are low, and the NAND and OR signals are high. Thus, the output voltage is defined by MODE, which chooses whether all NMOS or PMOS transistors on the right side of the core conduct. As a result, the circuit as a whole operates as a NAND gate when MODE is zero and as a NOR gate when MODE is one.

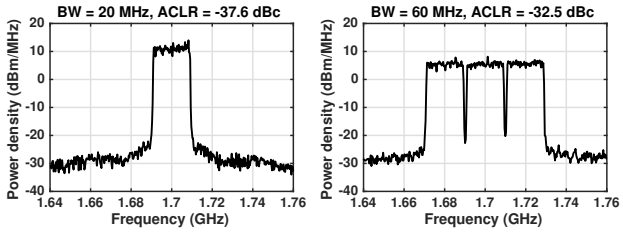
IV. Experimental Results

The presented PA was implemented in 28-nm CMOS. The die micrograph is shown in Fig. 5. The eight PA units are located near the top edge, and each of their outputs is connected to two bonding pads, which are wire-bonded to the power combiner on PCB. 12 digitally controlled delay lines for static fine-tuning of the signal timing are also visible. The remainder of the depicted area is mostly occupied by supply capacitors and routing of supply and ground nodes. The depicted die area, excluding pads, is 1.31 mm^2, of which the PA units occupy 0.44 mm^2.

In all measurements, the PA input signals were produced by phase modulators resembling the design reported in [4]. Presented efficiency figures include all power consumption in the 1.8-V and 3.6-V supply domains. The power consumption in the shared 1.0-V supply is dominated by additional circuitry and is thus excluded from the PA efficiency. The output power is measured at the combiner output without de-embedding the combiner loss. The MODE bits of all PA units are set to zero.

Continuous-wave (CW) measurement results at 1.7 GHz are depicted in Fig. 6. The maximum output power achievable by the PA is 29.7 dBm (0.93 W) at 1.77 GHz, with an efficiency of 34.7%. In tri-phasing mode at 1.7 GHz, the peak power is reduced to 29.4 dBm (0.87 W) by the power-combiner frequency response and duty-cycle mismatches caused by the modulators. The PA efficiency is depicted as a function of output power in Fig. 6(a), demonstrating the efficiency improvement of tri-phasing compared to outphasing.

Fig. 6(b) presents the CW output power as a function of the outphasing angle at all four coarse amplitude levels. These results show that there are no gaps in achievable



(a) (b)

Fig. 7. Measured spectra with (a) 20-MHz LTE and (b) 60-MHz aggregated LTE signals.

TABLE I
COMPARISON OF MEASUREMENT RESULTS.

	JSSC [5]	JSSC [6]	ESSCIRC [7]	This work
CMOS tech. (nm)	32	45	45	**28**
PA class	Class D	Class D	Class E	**Class D**
Peak P_{out} (dBm)	25.3	31.5	31.6	**29.7**
Peak efficiency (%)	35	27	43.7	**34.7**
Carrier freq. (GHz)	2.4	2.4	2.4	**1.7**
64-QAM signal	WiFi	WiFi	LTE	**LTE**
Mod. P_{out} (dBm)[1]	19.6	24.8	26.6	**23.1**
Mod. efficiency (%)[1]	21.8	16	20.1	**15.3**
Max. BW (MHz)	20	20	20	**60**

[1] Bandwidth = 20 MHz

levels of output power due to the slight overlap in the output power ranges of any two adjacent amplitude levels. The maximum outphasing-angle range corresponding to the overlap is 13°. This is significantly smaller than the similar redundancy in multilevel outphasing, where an outphasing angle of 90° always corresponds to a zero output power. Thus, in addition to previously mentioned advantages over multilevel outphasing, tri-phasing also features an increased effective output-amplitude resolution.

The modulation performance of the PA was evaluated with 20-MHz LTE and 60-MHz aggregated LTE signals at a carrier frequency of 1.7 GHz. Signal component separation was performed according to measured minimum and maximum CW output power at each coarse amplitude level, but otherwise no predistortion was used. Fig. 7 depicts the resulting spectra, where the peak-to-average power ratio (PAPR) is limited such that the EVM of each carrier is at most 8%. With a 20-MHz bandwidth, the PA achieves an average output power of 23.1 dBm with an efficiency of 15.3% and an ACLR of -37.6 dBc. With a 60-MHz bandwidth, the average output power is 22.4 dBm, the efficiency is 13.8%, and the ACLR is -32.5 dBc.

Table I summarizes the results and compares them to previously published CMOS PAs that use outphasing or related techniques and integrate all PA units on a single die. Among the compared PAs, our implementation features the widest reported signal bandwidth.

V. Conclusion

In this paper, we have presented the first reported tri-phasing PA, implemented in 28-nm CMOS. We introduced tri-phasing, a new transmitter architecture capable of achieving the back-off efficiency of multilevel outphasing without linearity degradation caused by waveform discontinuities at amplitude transitions. The presented PA contains eight units with cascoded class-D output stages, and features on/off logic circuitry that enables multilevel operation with input signals produced by low supply-voltage phase modulators. The measured peak output power at 1.77 GHz is 29.7 dBm with an efficiency of 34.7%. Operation with modulated signals has been verified at bandwidths up to 60 MHz, which is the widest reported bandwidth among similar PAs.

Acknowledgment

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