Haapala, Tuomas; Halonen, Kari

A Fully Integrated Digitally Programmable Pulse Shaping 6.0-8.5 GHz UWB IR Transmitter Front-End for Energy Harvesting Applications

Published in:
2018 IEEE International Symposium on Circuits and Systems (ISCAS)

DOI:
10.1109/ISCAS.2018.8350895

Published: 01/01/2018

Please cite the original version:
A Fully Integrated Digitally Programmable Pulse Shaping 6.0-8.5 GHz UWB IR Transmitter Front-End for Energy Harvesting Applications

Tuomas Haapala, Kari Halonen
SMARAD-2/Department of Electronics and Nanoengineering, Aalto University School of Electrical Engineering, Espoo, Finland
Email: firstname.lastname@aalto.fi

Abstract—This paper presents a fully integrated ultra-wideband impulse radio transmitter front-end (TFE) that is compliant with the European spectral mask. The compliance is achieved by means of 4-bit digital pulse shaping and an integrated matching network. The center frequency of the TFE is digitally tunable with 24 MHz resolution between 6.5 - 8.0 GHz. The TFE delivers at least 2.0 pJ pulses over the whole frequency range and achieves 4.4 % efficiency at 7.5 GHz center frequency and 4 MHz pulse repetition rate. The static power consumption is 480 nW, which enables the TFE to reach high efficiency levels even at low pulse repetition rates. The TFE is designed in a commercial 65-nm CMOS process. The performance of the TFE is evaluated through post-layout simulations.

I. INTRODUCTION

Many internet of things scenarios predict an exponentially growing number of ambient sensors for the near future. To avoid extensive wiring, many of these sensors are made capable of wireless data transfer. In addition, some of these wireless sensors employ energy harvesting to limit the number of batteries that would eventually require replacing.

Ultra-wideband impulse radios (UWB IRs) have been proposed as a potential candidate for realizing wireless capabilities for energy-autonomous sensor nodes [1], [2]. Most recently published low-power UWB IRs target the U.S. UWB mask between 3.1 – 4.8 GHz, regulated by the Federal Communication Commission (FCC). This allows power savings due to low center frequency and relaxed spectral requirements compared to Asia and Europe. However, UWB IRs designed for the FCC mask rarely comply with the regulations of other regions due to the relaxed requirements, which limits the global applicability of these designs. In addition, most regions only allow usage of the 3.1 – 4.8 GHz frequency range presuming appliance of mitigation techniques [3]. The band is also surrounded by strong narrow-band ISM and WLAN interferers, which makes receiver design more challenging.

Edge-combining IR UWB transmitters have demonstrated adequate pulse shaping (PS) capabilities for potential compliance with the European (EC) UWB mask [4]. However, edge combiners based on a delay chain often suffer from coarse digital frequency tuning resolution [4]–[7] or they rely on analog frequency tuning [8].

This work presents a fully integrated edge-combining UWB IR transmitter front-end (TFE) that complies with the EC UWB mask [9] between 6.0 - 8.5 GHz up to moderate pulse repetition rates (PRRs). The compliance is achieved by means of 4-bit pulse-shaping and an integrated matching network. The frequency band above 7.25 GHz has a wide unrestricted global availability [3]. In addition, the TFE demonstrates a novel digital center frequency \( f_c \) tuning method based on switchable supply capacitor banks that shows an excellent linearity over a wide tuning range and a high tuning resolution. The TFE demonstrates a very low static power consumption level that allows high-efficiency operation also at low PRRs. The generated pulse energy level suffices for a line-of-sight communication range of more than ten meters with a high-quality receiver [2], [7].

II. IMPLEMENTATION

A block-level description of the designed impulse-combining TFE architecture is presented in Fig. 1. There are 32 programmable delay units (\( \Delta \)), routers (R), combiners (C), a power amplifier (PA) and a matching network (MN).

![Fig. 1. Edge-combining TFE architecture. The TFE consists of delay units (\( \Delta \)), routers (R), combiners (C), a power amplifier (PA) and a matching network (MN).](image-url)
impulses propagated by the routers are serialized by parallel-to-series (PTS) converters $\alpha$ and $\beta$ that consist of impulse combiners (C). The delay chain delivers alternate impulses to PTS converter $\alpha$ and the rest to $\beta$. This interleaving relaxes the speed requirement of the combiners. Finally, the generated trains of serial impulses trigger the power amplifier (PA) that has an integrated matching network (MN).

### A. Digitally tunable delay unit

The applied delay units are similar to the implementation in [7]. The delay unit propagates and reloads fast, allowing a high maximum center frequency and a high maximum PRR. Instead of using programmable driver transistors [4], [5], programmable capacitive loading [6] or analog supply voltage control [8], however, we propose adjusting the propagation delay of the delay units by altering their supply voltage level by means of a digitally programmable capacitor bank. Based on simulations, some advantages of the proposed method include high linearity and a wide tuning range.

A gradual drop in the supply level of the delay units during pulse generation will translate into an increased $\delta$ (decreased $f_c$) along the delay chain. For this reason, the power supply of an edge-combining impulse transmitter needs extensive buffering especially in energy harvesting applications where the applied harvester cannot necessarily provide high current levels. To relieve supply buffering requirements, we propose giving each delay unit an isolated supply. Since every delay unit is triggered only once per generated pulse, the isolated supply voltages can drop significantly during trigger propagation and the applied harvester cannot necessarily provide high current buffering especially in energy harvesting applications where the applied harvester cannot necessarily provide high current levels. To relieve supply buffering requirements, we propose giving each delay unit an isolated supply. Since every delay unit is triggered only once per generated pulse, the isolated supply voltages can drop significantly during trigger propagation while the TFE still retains a constant $\delta$ along the delay chain.

The isolated supply of a delay unit, $V_{dd\Delta}$, is created by a capacitor bank as presented in Fig. 2(a). Capacitor $C_0$ provides a low-resistance energy buffer for the delay unit. Initially, switches $S_1$ are open and switches $S_3$ connected to either $V_{dd}$ (1.2 V) or $V_{dd2}$ (0.6 V), charging unit capacitors $C_u$ through switches $S_2$. The position of switches $S_3$ is controlled by binary control word $tune\_freq$. Capacitor $C_0$ is charged to $V_{dd}$ through a separate switch (not shown in Fig. 2(a)). During pulse generation, switches $S_2$ are opened and switches $S_1$ then closed, connecting unit capacitors $C_u$ and capacitor $C_0$ in parallel. The consequent charge distribution between the capacitors sets the targeted $V_{dd\Delta}$ level. The capacitor bank is returned back to the initial state after pulse generation.

A transient simulation of the behavior of $V_{dd\Delta}$ during pulse generation is shown in Figure 2(b). It also shows the control voltages for switches $S_1$ and $S_3$, a low control voltage level denoting a closed switch. Initially, capacitor $C_0$ is charged to $V_{dd}$. $V_{dd\Delta}$ has settled to its target level at about 2 ns. The delay unit is triggered at around 4.5 ns, resulting in consumed charge and a consequent drop in $V_{dd\Delta}$. The capacitor bank is recharged immediately after pulse generation.

The final implementation uses binary 5-bit capacitor banks ($C_u = 33 \text{ fF}$) for coarse $V_{dd\Delta}$ tuning and binary 4-bit capacitor banks ($C_u = 2.1 \text{ fF}$) for fine $V_{dd\Delta}$ tuning.

### B. Other blocks

Fig. 3(a) shows the implementation of the routers and combiners. The routers are based on two cascaded inverters, the transparency of the former being controlled by a switch transistor. A single router comprises 4 inverter pairs that constitute the 4 output channels. The combiners convert 4 parallel input impulses into a single output impulse. An impulse at the gate of one of the input transistors M1 – M4 pulls node 1 low, which results in the output node being pulled high by inverter 11. The feedback path composed of inverter I2 and transistor M5 return node 1 back to its original state, after which the output is also returned low. Transistor M6 keeps node 1 pulled high at the steady state. The proposed combiner propagates fast since it does not include any cascode transistors. In addition, the combiners have a small input capacitance.

The PA design is shown in Fig. 3(b). It has 4 input channels, each of which is divided to 2 sub-channels for impulse trains coming from PTS converters $\alpha$ and $\beta$. After buffering, the impulse trains are combined at the drain of the PA. Fig. 3(c) shows the schematic of the fully integrated wideband MN. The MN consists of an elliptic low-pass section (enclosed...
III. SIMULATION RESULTS

The TFE was designed using a commercial triple-Vt 65-nm CMOS process and validated through post-layout (PL) simulations in Spectre. In addition, the MN was analyzed and adjusted through electromagnetic (EM) simulations in Momentum. The TFE measures 240 \( \mu \)m x 340 \( \mu \)m including the delay chain supply capacitor banks but excluding the PA and MN. The PA and MN measure 280 \( \mu \)m x 470 \( \mu \)m.

Simulation results for the MN are presented in Fig. 4. Fig. 4(a) is normalized to 50 \( \Omega \). The -1 dB passband of the MN ranges from 5.7 GHz to 9.1 GHz. In that range, the real part of \( Z_L \) is matched to approximately 30 \( \Omega \) while the imaginary part remains small. The minimum attenuation in the passband is 2.4 dB. Between 6.5 - 8.0 GHz, the maximum group delay variation over a 500 MHz band is less than 10 ps.

The full \( f_c \) tuning range of the TFE is shown in Fig. 5(a). Here, \( f_c \) is given by the inverse of the average propagation delay over a single delay unit. The target \( f_c \) band between 6.5 - 8.0 GHz is fully covered at tt, ss and ff process corners over the temperature range from -40 to 80 °C.

A Monte Carlo (MC) simulation of the fine frequency tuning resolution of the delay chain is presented in Fig. 5(b). The data consists of 32 MC points at tt corner, each of which comprises 15 fine tuning steps in the middle of the full tuning range (480 steps in total). TFE has an average fine frequency tuning resolution of 19.6 MHz with a 1.2 MHz standard deviation (\( \sigma \)). The equivalent voltage step is 0.76 mV. A 64-point MC simulation in the middle of the tuning range gives an average coarse tuning step of 218 MHz with a 1.5 MHz standard deviation.

The PS performance of the TFE is depicted in Fig. 6. The TFE is programmed with a Gaussian envelope of constant pulse length that results in a 500-MHz signal bandwidth. The four target sub-bands are centered at 6.5, 7.0, 7.5 and 8.0 GHz.
Fig. 6(a) shows that the TFE generates a constant output pulse energy over the target $f_c$ range. More energy is consumed per pulse ($E_p$) at higher frequencies since more impulse combinations (sub-pulses) are required for pulse generation. At a 2.1 pJ pulse energy ($E_p$) and 7.5 GHz $f_c$ setting, the TFE consumes 48 pJ per pulse, corresponding to 4.4 % efficiency ($\eta$). The static power consumption ($P_s$) is 480 nW.

The maximum PRR of the TFE is about 25 MHz at ss corner, limited by the reload time of the delay chain supply capacitor banks. However, the maximum continuous PRR is limited by the spectral quality of transmission. Example pulse envelopes at 7.5-GHz $f_c$ are shown in Fig. 6(b). At medium $E_p$ levels around 2 pJ, the mask is violated by the main lobes at 4 MHz PRR. The power spectral densities (PSDs) of four 2 pJ output pulse trains at 4 MHz PRR at the target sub-bands is shown in Fig. 6(c).

### IV. COMPARISON WITH OTHER WORKS

The performance of the TFE is compared with the current state of the art in Table I. The selected works have been verified by measurements and combine a high $E_p$ level with a low or moderate PRR option. The TFE is set to 7.5 GHz $f_c$ for a wide global availability.

The proposed TFE is the only one to target the EC UWB mask. Despite the more strict spectral requirements, the integrated matching network and a high $f_c$, the TFE achieves a comparable $E_p$ and $\eta$. The novel $f_c$ tuning method achieves a better resolution than most designs. Fig. 7 demonstrates how the TFE retains a very low power consumption level over a wide range of PRRs due to its low $P_s$ level. This feature is practical in energy harvesting applications where the accessible power level may vary from microwatts to milliwatts depending on ambient conditions and harvester size. While the transmitters in [7], [15] and [16] demonstrate a slightly lower power consumption, they operate at the low FCC band, suffer from coarse frequency tuning and lack PS capabilities.

### V. CONCLUSION

This paper presents a fully integrated UWB IR TFE whose performance was evaluated through post-layout simulations. The compliance with the EC UWB mask is achieved by means of 4-bit pulse shaping and an integrated PA matching network. Unlike designs targeting the FCC UWB mask, this design has a wide global applicability. The TFE delivers 2.1 pJ pulses at 7.5 GHz center frequency with 4.4 % total efficiency, demonstrating a comparable performance to the state of the art.

The novel digital $f_c$ tuning method based on isolated supply capacitor banks allows a wide tuning range with an improved tuning resolution of 24 MHz between 6.5 – 8.0 GHz. The $P_s$ is 480 nW, allowing a high efficiency level even at low data rates. The low $P_s$ level and the isolated supply capacitor banks improve the practicality of the design in energy harvesting applications.

### ACKNOWLEDGMENT

This work was funded by The Naked Approach (40336/14, 3246/31/2014) and Towards Digital Paradise (2727/31/2016) projects granted by Business Finland, EffiNano project granted by Aalto University School of Electrical Engineering (10/2012, 1/2014) and Aalto ELEC Doctoral School. The authors thank Tuomas Rantataro, Mika Pulkkinnen and Jarno Salomaa for their technical advice.
REFERENCES


