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A 180-nW Static Power UWB IR Transmitter Front-End for Energy Harvesting Applications

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Abstract—This paper presents a versatile, FCC compliant ultra-wideband impulse radio transmitter front-end (TFE) that performs well at a wide range of pulse repetition rates up to 105 MHz. The TFE delivers 2.2 pJ pulses with 6.7 % efficiency at 3.8 GHz center frequency. The leakage power is 180 nW from a 1.2 V supply. The TFE operates robustly with a variety of power sources, including a 6.5 cm² photovoltaic array in office illumination. Along with the low static power consumption level, this feature makes the TFE suitable for energy harvesting applications. The TFE is fabricated in a 180 nm CMOS process.

I. INTRODUCTION

Novel internet of things applications are enabled by energy autonomous wireless sensor nodes that power themselves by harvesting ambient energy. A possible use case is a gadget-free, batteryless gesture sensor that controls an intelligent space wirelessly. A variety of data rates and a wireless link range of at least 10 meters have to be supported in order to ensure wide applicability. The acquirable power levels by means of energy scavenging are commonly very low compared with battery-powered devices, which puts an emphasis on ultra-low power performance.

Ultra-wideband impulse radio (UWB IR) transmitters suit applications with variable data rates and a strict power budget particularly well due to their heavily duty-cyclable character. At low pulse repetition rates (PRRs), the total power consumption is dominated by static power, such as leakage power and the overhead power of bias circuits. At high PRRs, the total power drain is dominated by pulse generation. Consequently, the demand for substantial data rate scalability brings about a design target to both maximize pulse generation efficiency and minimize static power consumption. An appropriate control on the output pulse waveform is necessary in order to ensure that the power spectral density (PSD) of the output pulse fits a certain standard. In addition, a picojoule range output pulse energy level is required for reaching a communication range of more than 10 meters.

An implementation of a UWB IR transmitter front-end (TFE) architecture was presented in [1] that meets the aforementioned requirements. It was also later applied in [2]. The architecture is outlined in Fig. 1. A trigger signal propagates through a series of delay blocks that each generate a single rectangular pulse one after another. The rectangular pulses are buffered and delivered to a power amplifier (PA) where they are superposed. The weight of each buffer can be tuned individually, which makes the output pulse envelope programmable. The propagation delay of the delay chain can be altered, which translates into a tunable output pulse center frequency. The

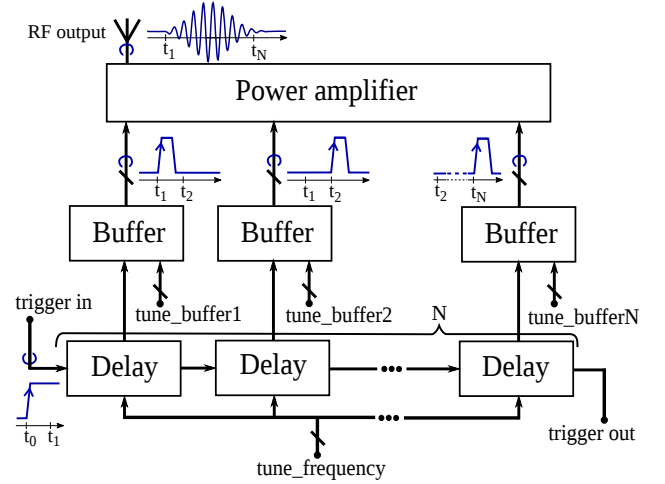


Fig. 1. Conceptual block diagram of the applied TFE architecture.

front-end is inherently in a quiescent mode between pulses. Only leakage power is consumed during quiescence since no active circuitry is required, such as bias circuits.

This paper introduces such modifications to the previous implementations that improve the usability of the design in energy harvesting applications while maintaining a comparable overall performance over a wide range of PRRs. Implementation in a 180 nm CMOS process facilitates a low total leakage current level but simultaneously slows the architecture down and increases parasitic capacitive loading. The retardation problem is addressed by a novel delay block design. The front-end efficiency is boosted by circuitry reductions that are enabled by allowing a fixed output pulse envelope. The TFE is demonstrated to perform robustly when powered by a small photovoltaic array.

II. TRANSMITTER FRONT-END IMPLEMENTATION

The proposed TFE is shown in Fig. 2. The front-end is triggered by a falling edge that is transformed into a rectangular pulse by a simple trigger modifier circuitry. The rising edge generated by the modifier triggers the delay chain, whereas the falling edge initiates an immediate reset process. This arrangement ensures insensitivity to input trigger duty cycle and transition time variation.

In comparison with the design in [1], the parallel programmable PA transistors have been removed, which reduces the capacitive loading of the delay chain and the PA output

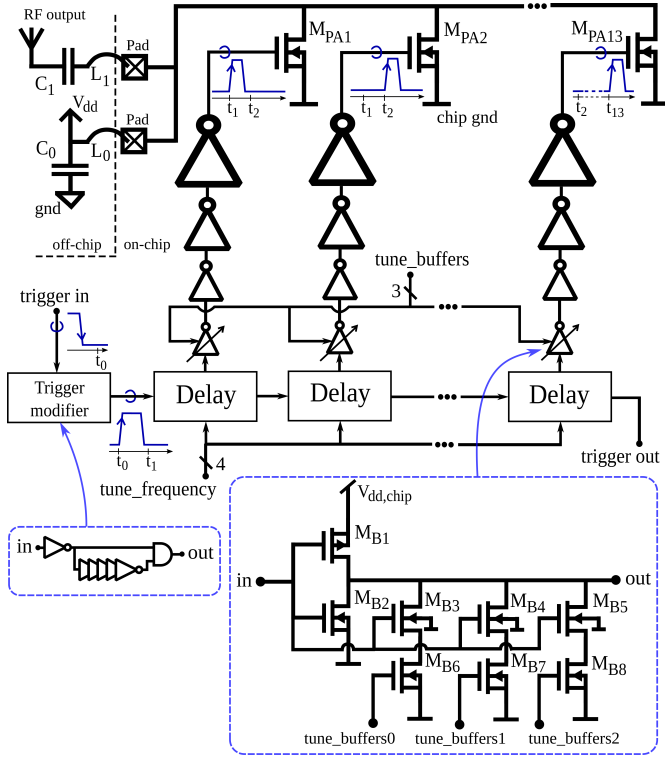


Fig. 2. UWB IR transmitter front-end.

and decreases the total power consumption. As a penalty, the output pulse envelope becomes non-programmable and it must be fixed in the design stage. Each delay block drives a tapered buffer inverter chain. The first inverters of the chains are tunable, as shown at the bottom of Fig. 2. The summed drive strength of transistors $M_{B2} - M_{B5}$ is controlled by switch transistors $M_{B6} - M_{B8}$. The tunability of the first buffer inverters allows adjusting the width of the pulses that drive the PA. This ensures that the pulses do not overlap in time at any output pulse center frequency. The delay chain comprises 13 delay blocks.

The output pulse waveform is generated as the superposition of the signals from PA transistors $M_{PA1} - M_{PA13}$. These transistors are sized so that they generate a Gaussian output pulse envelope. A parallel band-pass LC circuit is formed by bonding wire L_0 , the parasitic capacitance of the two chip pads and the drains of transistors $M_{PA1} - M_{PA13}$. A series band-pass LC circuit is formed by bonding wire L_1 and discrete capacitor C_1 . Capacitor C_0 acts as a discrete wideband supply decoupler for the PA and measures 20 nF. Large on-chip current peaks during the generation of a pulse are buffered by a 2 nF on-chip capacitor, which allows the usage of power sources with low current drive strength.

The delay block design in [1] induces a strong trade-off between the minimum propagation delay and the block reset time. In this work, the delay block design has been revised in order to make the propagation of a trigger fast enough in the used process while maintaining a high maximum PRR. The schematic of the novel delay block design is shown in Fig. 3. The transistors with thick symbols are wide. Transistor M_{D13} uses the same configuration as the tunable transistor in the

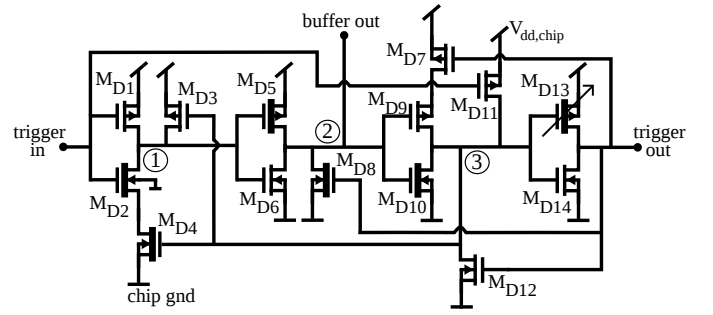


Fig. 3. Delay block.

buffer chain, thus enabling an adjustable propagation delay.

Initially, the input node, node 2 and the output node are pulled low. Nodes 1 and 3 are pulled high. A rising edge in the input propagates through the delay block like in a series of inverters. During the propagation, feedback transistor M_{D3} pulls node 1 back to positive supply. Finally, node 2 is restored to ground by the feedback from the output node through transistor M_{D8} and feed-forward from node 1 through transistor M_{D6} .

A falling edge in the input starts the reset process of the block, during which node 3 is pulled high by transistor M_{D11} , followed by the output node being pulled low by transistor M_{D14} . Transistor M_{D11} has to be sized wider than transistor M_{D12} to ensure that node 3 can be pulled high reliably.

The presented delay chain structure has several advantages over the conventional solution. Firstly, a propagating trigger is always driven by wide transistors, which makes the propagation fast. Secondly, nodes 1 and 2 are set back to their initial state during propagation, making also the following reset process fast. Thirdly, node 2 is pulled by wide transistors with no other transistors in cascade, making the driving of that node efficient. This is important because the node is loaded by a buffer inverter. The foremost drawback of the design grounds from the relatively complex structure, which increases parasitic capacitive loading and, therefore, requires additional energy per triggering.

The wide transistors were scaled for minimum propagation time based on simulations. Too narrow transistors cannot provide enough current for quick propagation whereas too wide transistors add more to the parasitic load than to the driving capability. Transistors M_{D11} and M_{D14} were sized for keeping the reset time bearable. The rest of the transistors do not drive critical signals and, therefore, they were sized for minimal capacitive loading.

III. MEASUREMENT RESULTS

The TFE was implemented in a 180 nm CMOS process and bonded directly to a PCB. It measures 350 μm x 80 μm . A 1.2 V supply was used. A die photograph of the front-end is shown in Fig. 4.

A 20 Gsa/s oscilloscope was employed for measuring the output waveform of the TFE for different center frequency and buffer tuning combinations. A measured output pulse train at 105 MHz PRR is presented in Fig. 5. The shown pulses

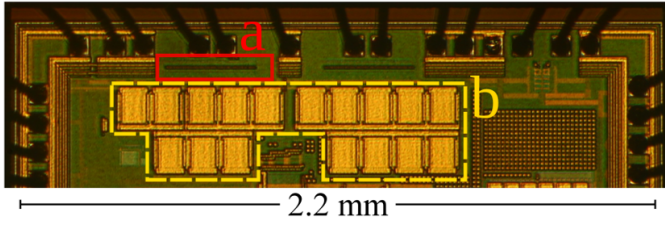


Fig. 4. Die photograph showing the TFE (a) and a 2 nF on-chip supply decoupling capacitor (b).

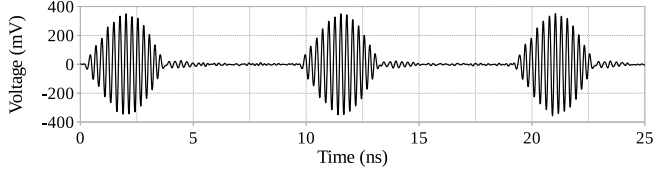


Fig. 5. Measured pulse train at 105 MHz PRR.

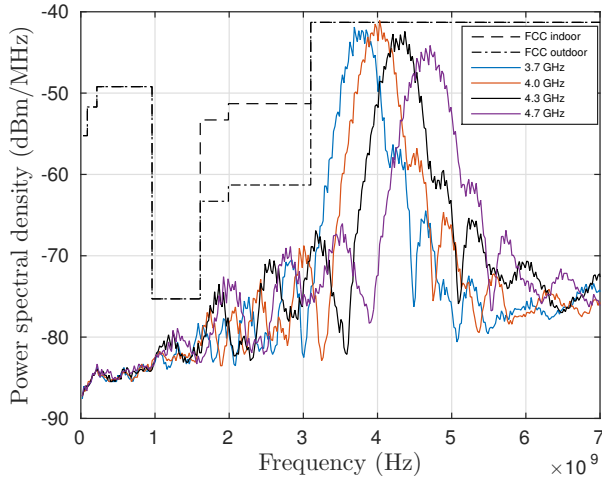


Fig. 6. Measured power spectral densities of four pulse trains of different center frequencies at 8.5 MHz PRR.

have a center frequency of 3.9 GHz and energy of 2.1 pJ. The same pulse energy was measured at 100 kHz PRR, which demonstrates that no considerable pulse energy deterioration occurs as the PRR is increased. The visible residual oscillation after each pulse is caused by reflections between the input port of the oscilloscope and the transmitter output. The reset time of the delay chain is approximately 10 ns.

Fig. 6 shows the power spectral densities of four output pulse trains of different center frequencies at 8.5 MHz PRR. The PSDs were measured with a spectrum analyzer using a 1 MHz resolution bandwidth and a power average mode. The PSDs show that the generated pulse trains are compatible with the FCC mask. The minimum output pulse center frequency is 2.9 GHz and the maximum is 4.8 GHz.

The leakage power of the TFE is 0.18 μ W. The trigger modifier block, delay blocks and buffer blocks consume 11.3 pJ per pulse in total, while the energy consumption of the PA is strongly dependent on the used setting. The largest pulse measures 2.2 pJ at 3.8 GHz center frequency and 10 MHz PRR. Generating this pulse consumes 32.8 pJ of energy

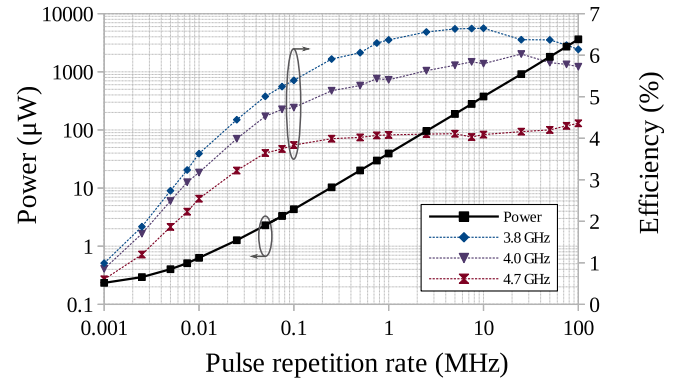


Fig. 7. Measured power consumption and efficiency profile of the TFE. The presented power consumption curve is that of the 4.0 GHz pulse train.

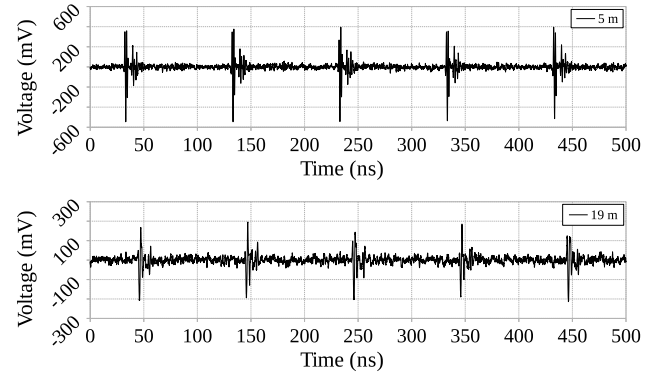


Fig. 8. Received signal at two distances from the TFE at 10 MHz PRR.

in total, resulting in 6.7 % front-end efficiency, defined as the ratio of the output pulse energy to the consumed active energy per pulse. The pulse energy for a 4.7 GHz pulse train at 10 MHz PRR is 1.4 pJ. The measured power consumption and efficiency profile for the TFE is depicted in Fig. 7.

A receiver front-end was built of discrete components in order to estimate an approximate communication range for the TFE. The TFE was set to 4.0 GHz center frequency and 10 MHz PRR. Planar, elliptical dipole antennas were employed of 3 dBi nominal gain and return loss better than -12 dB. Fig. 8 shows the received signal at 5 and 19 meter distance from the TFE. The measurement result demonstrates that the TFE achieves a practical communication range.

The TFE's support for low-quality power sources was evaluated by powering it with a commercial 6.5 cm² photovoltaic (PV) array under 410 lx illumination, which corresponds to an office environment. The maximum power point of the employed PV array was approximately 25 μ W at 1.2 V output voltage. The output voltage of the PV array was regulated by a low-dropout regulator (LDO) integrated on the same die with the TFE, equivalent to the implementation reported in [3]. A current bias and a reference voltage for the LDO were provided from external sources. Fig. 9 shows the behavior of the system with the TFE set to 4.0 GHz center frequency and PRR swept. The TFE operated robustly up to 500 kHz PRR after which the LDO output voltage began to drop, resulting in the gradual deterioration of the pulse waveform. The TFE

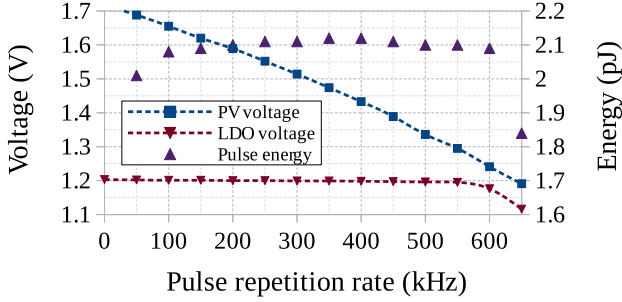
TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH OTHER HIGH PULSE ENERGY UWB IR TRANSMITTER FRONT-ENDS.

	This work	Miranda 2010 [1]	Ebrazeh 2015 [2]	Crepaldi 2011 [5]	Wentzloff 2007 [6]	Dokania 2010 [7]	Phan 2008 [8]
CMOS technology (nm)	180	65	90	90	90	90	180
Supply voltage (V)	1.2	0.75 / 1.2	1.2	0.9-1.1	1.0	0.9	1.5
Center frequency range (GHz)	2.9 - 4.8	3.6 - 7.5	2.9 - 6	2.9 - 3.8	3.45 - 4.65	3.5 - 4.5	3.5 - 4.5
Pulse amplitude (Vpp)	0.72	1.0	0.51	0.61	0.7	0.5	0.16
Pulse energy (pJ)	2.2	2.4 ^a	0.44 ^b	1.9 ^c	2.7 ^{d,†}	1.0 ^e	0.13 ^f
Consumed energy per pulse (pJ)	32.8	9.6 ^a	18.5	65	37	29	16.8
Efficiency [‡] (%)	6.7	25 ^a	2.4 ^b	2.9 ^c	7.3 ^{d,†}	3.4 ^e	0.77 ^f
Static power consumption (μW)	0.18	13	n.a.	184	96	2.8	3900

[‡] Ratio of the output pulse energy to the consumed active energy per pulse. [†] Rectangular pulse waveform. ^a Estimated from Fig. 5 at 0.75 V antenna driver voltage.

^b Estimated from the larger pulse in Fig. 6. ^c Estimated from Fig. 11 a. Compensated for the reported 1.2 dB cable loss. ^d Estimated from the larger pulse in Fig. 6, 4.6.

^e Estimated from Fig. 7 b. ^f Estimated from Fig. 10 b.


 Fig. 9. Operation of the TFE powered by a 6.5 cm² PV array at 410 lx.

was tested further under various illuminations with similar results. The results show that the TFE operates robustly with low-quality power sources without additional off-chip energy buffers. Furthermore, the result demonstrates the utility of the TFE's low leakage power level in ultra-low power applications.

The TFE consumes 16.4 pJ/bit when using on-off-keying (OOK) with a balanced bit stream. However, the value decreases to 8.2 pJ/bit if differential pulse position modulation (DPPM) is utilized with 4 bits encoded per pulse. Previously, we showed in [4] that this TFE, paired with a low-power DPPM modulator and a low-power ring oscillator, enables a 45.2 % total transmitter energy per bit improvement compared to OOK with a bit error rate of better than 10^{-6} in a low-frequency package.

The measurement results are summarized and compared with other works in Table I. The performance figures are estimated for Gaussian output pulse waveform when available for comparable spectral quality. The comparison demonstrates that the designed front-end achieves an extremely low power consumption level at low PRRs while providing a comparable efficiency, a large output pulse energy and an extremely low leakage current level.

IV. CONCLUSION

This paper presented a versatile FCC-compliant UWB IR TFE design that performs well with a wide range of PRRs and various power sources. These features are attained by employing an architecture and a process that allow keeping the total static power consumption level low while achieving a high efficiency, a controllable pulse waveform and a large pulse energy. A novel delay block design was introduced that propagates and resets fast in the given process.

The TFE delivers 2.2 pJ pulses at 3.8 GHz center frequency with 6.7 % total efficiency. It operates up to a 105 MHz PRR with no significant deterioration in the output pulse waveform. The leakage power is 0.18 μW. The TFE functions reliably in office illumination when powered by a small PV array and an integrated LDO, which demonstrates applicability with ultra-low power energy harvesting systems.

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