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A Wideband Blocker-Resilient Direct $\Delta\Sigma$ Receiver With Selective Input-Impedance Matching

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Abstract—This paper presents a wideband blocker-tolerant Direct $\Delta\Sigma$ receiver (DDSR). Blockers are attenuated through selective input impedance matching and optimized gain design. The created impedance profile provides low receiver input impedance at blocker frequencies, while at desired frequencies, the impedance is boosted to matched condition through an up-converted positive feedback from the DDSR output. Receiver is evaluated in a 28nm fully-depleted silicon-on-insulator CMOS process with total power consumption of 25mW at 1V supply voltage. The receiver is designed for configurable operation from 0.7-2.7GHz, a baseband bandwidth of 10MHz, demonstrates a maximum noise figure of 6.2dB, and achieves a peak SNDR of 53dB with an out-of-band 1dB input compression point of -11.5dBm at 100MHz offset.

I. INTRODUCTION

Digital intensive wideband receivers, for emerging radio access standards such as 5G and LTE, are in growing demand due to their ease of configurability. One such digital intensive architecture is the direct $\Delta\Sigma$ receiver (DDSR) as illustrated in Figure 1 [1]. The architecture differs from the conventional direct conversion receiver by embedding RF front-end blocks as a part of delta-sigma-modulator (DSM) loop-filter. In this way, signal discretization already begins at RF and the DSM loop-filter now performs both functions of channel select filtering (CSF) and quantization noise shaping.

Inherently, such wideband DDSRs are exposed to high-power out-of-band (OB) blockers. If not attenuated, these blockers can completely saturate the receiver (RX) and make the RX operation non-linear. Techniques such as applying N-path filtering at the LNA output and low-noise transconductance amplifier (LNTA)/mixer first arrangements have been reported earlier for OB blocker attenuation [2], [3]. However, as will be explained later, all these techniques have certain limitations when it comes to blocker attenuation.

Compared to previously introduced techniques, the blocker-resilient DDSR proposed in this paper adds additional band-pass filtering at the DDSR input through selective input impedance matching. Additionally, an approach for optimized receiver gain design is followed which results in an improved near-band compression point.

The paper is organized as follows. Section II describes the limitations of blocker rejection with basic N-path filtering and how the blocker rejection can be improved. Section III

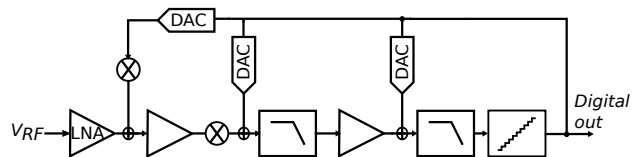


Fig. 1. Generic block diagram of the direct $\Delta\Sigma$ receiver. RF stages are included in the $\Delta\Sigma$ modulator (DSM) loop-filter.

details theoretical aspect of proposed DDSR while section IV covers its transistor level implementation details. The paper finishes with performance evaluation results in section V and conclusion in section VI.

II. BLOCKER REJECTION FOR A DDSR

Typically, a DDSR implements basic N-path filtering techniques for OB blocker rejection at the LNA output [1], [4]. However, there are two limitations with this approach. First, the gain/loss of far-away blockers is limited by the N-path mixer switch resistance (R_{ON}) and the LNA transconductance (gm_{LNA}) which should both be minimized. These parameters cannot be reduced indefinitely due to limitations on LO drive power consumption and LNA noise contribution. Second, filtering is implemented only at the output of the LNA, neglecting the filtering requirement at the LNA input. Without input filtering and provided the low blocker gain at the LNA output, LNA transconductor can enter non-linear operation if the blocker reaches the input swing limitations of the transconductor. Therefore, an optimum design should ideally filter the OB blockers already at the LNA input. Input transconductor non-linearity can also be overcome by completely eliminating it in mixer first arrangements. However, in DDSRs, mixer first arrangements pose quantization noise image emission to antenna [1]. Therefore, mixer first topology is problematic for our application.

Another important aspect for optimized OB blocker rejection is to only apply the minimum possible gain required in the RX chain. For basic N-path filters, lower gain will result in lower near-band blocker gain and consequently improve the near-band compression point. However, generally gain cannot

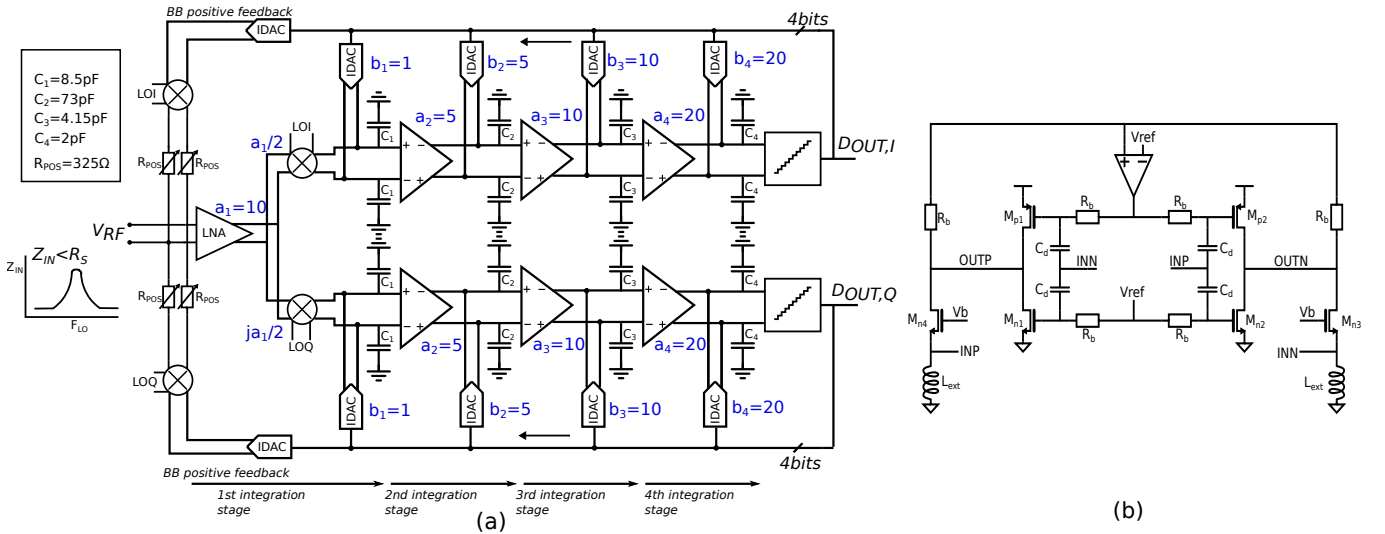


Fig. 2. (a) Proposed wide-band DDSR architecture. Blockers are attenuated through low LNA input impedance (Z_{IN}) while positive feedback from BB increases the Z_{IN} to matched condition for desired frequency (b) Common-Gate Common-Source (CG-CS) LNA schematic.

be reduced indefinitely as it's needed for two reasons. First, it suppresses noise contributions from the later stages of the receiver. From this point of view only minimum gain, which suppresses the noise contribution of later stages, should be applied. Second, gain is needed so that the weakest input signal appearing at the ADC input is sufficiently greater than the quantization noise of the ADC. For DDSRs, however, the quantization noise profile is shaped by $\Delta\Sigma$ modulator (DSM) feedback. A properly designed DSM feedback ensures that the quantization noise in desired band is much lower than thermal noise floor, resulting in reduced dependency of the RX gain on ADC signal to noise ratio (SNR) requirements.

Based on the aforementioned discussion, our proposed DDSR consists of optimized receiver gain design together with tunable bandpass filtering at RF input. In coming sections we detail the design of RF front-end and DDSR loop filter.

III. RECEIVER DESIGN

A. Front-end Design

Figure 2 shows the block diagram of the proposed DDSR. Blocker filtering at the input is implemented by designing a low intrinsic input impedance (Z_{IN}) Common-Gate Common-Source (CG-CS) LNA while for desired frequency Z_{IN} is boosted to match source impedance (R_S) through implementation of up-converted positive feedback from baseband (BB). The amount of positive feedback can be adjusted through the resistance R_{POS} . Neglecting any non idealities, the overall receiver input impedance of LNA can then be approximated as:

$$Z_{IN}(f_{LO}) = \frac{Z_{LNA}}{1 - \gamma A_V \left(\frac{Z_{IN}}{Z_{IN} + R_{POS}} \right)} \quad (1)$$

where $Z_{IN}(f_{LO})$ is the input impedance at the desired frequency, Z_{LNA} is the intrinsic input impedance of the LNA, A_V denotes

the voltage gain of the DDSR and γ represents passive mixer conversion losses.

B. DSM Design

DSM filter design starts by dividing the gain in the RX chain. For optimized blocker rejection, minimum required gain is applied only in the first stage of DDSR loop filter. After this, the number of stages required for quantization noise shaping can be derived from [4]:

$$n = \frac{\log\left(\frac{\Delta^2}{6f_s k T G_{RX} F_{RX}}\right)}{2 \log\left(\frac{f_{NSP}}{f_{BW}}\right)} \quad (2)$$

where Δ is the quantizer step size, f_s is the sampling frequency, K is Boltzmann constant, T is the temperature in Kelvins, G_{RX} is the RX power gain, F_{RX} is the noise factor of the RX excluding quantization noise, f_{BW} is BB bandwidth cutoff frequency, and f_{NSP} is the combined noise shaping pole cutoff frequency. f_{NSP} is selected such that the quantization noise is attenuated far below the thermal noise floor inside the desired band.

For an initial f_{NSP} selection at 10 times f_{BW} , we can calculate required noise shaping poles as $n = 2.57$ or 3. Apart from noise shaping, channel select filtering (CSF) is also needed from DSM loop filter. As gain is only applied in a single stage, a single CSF pole is positioned at f_{BW} . This CSF pole and three noise shaping poles create a fourth order DSM loop filter which was implemented through a cascade-of-integrators in feedback (CIFB) topology, where the first stage provides channel select filtering and the other three stages provide noise shaping for the DDSR. As an initial value for the DSM filter, Butterworth filter coefficients were chosen due to minimal peaking in its signal transfer function (STF) response. Final filter coefficients values after scaling with stage gains and referring to f_{BW} are shown in Figure 2(a).

In the proposed DDSR, an additional positive feedback from the DDSR baseband is needed for input impedance matching. To keep the DSM filter design simple and to avoid the risk of instability, positive feedback was designed separately after the 4th order DSM implementation. Positive feedback increases the RX gain and hence reduces BB channel bandwidth. Therefore, initial design of the DSM loop filter starts with smaller gain and selection of f_{BW} 1.5 times than desired $f_{BW} = 10\text{MHz}$ so that positive feedback reduces the bandwidth to the desired f_{BW} after implementation.

In order to avoid risk of quantization noise up-conversion through positive feedback quadrature mixers, $f_s = f_{LO}$ was selected. This ensured that the up-converted quantization noise falls out of the desired band and causes minimal NF degradation. The quantizer/IDACs for DDSR were implemented as ideal 4bit components with 600mV differential input range. A clock delay of 200ps, for $f_s = f_{LO}$, was added between the quantizer output and the IDACs input for modeling real clock skew.

IV. SYSTEM IMPLEMENTATION

The DDSR is designed for an RX gain of 20dB. The RF front-end of DDSR consists of an LNA implementation with a parallel combination of CG and push-pull CS amplifiers [5]. The parallel combination increases the LNA g_{mLNA} , and push-pull configuration helps to achieve better large signal linearity. The differential intrinsic input impedance of the LNA was designed to be around 25Ω differential by increasing the single ended CG g_m from usual 20mS to be 40mS.

Positive feedback from the output of the BB amplifiers is up-converted to the RF nodes through passive quadrature mixers. The amount of positive feedback is controlled through series resistors R_{POS} . The stability of positive feedback loop was analyzed through transient and simple pole-zero transfer function analysis [6]. Results confirmed stability for $R_{POS} > 250\Omega$. For design implementation, we selected $R_{POS} = 325\Omega$, which ensured stability at all process corners.

Transistors with a large aspect-ratio of $48/0.03\mu\text{m}$ were implemented in the main path mixers. This ensured a small switch resistance of 8Ω for better attenuation at far away offsets from f_{LO} . As there was no such requirement of smaller R_{ON} for the positive feedback mixers, their aspect-ratio was selected to be four times smaller than main path mixers.

BB integrators were implemented through self-biased differential pair configurations. The first BB integrator is designed for a higher transconductance of 25mS for lower noise contribution. The later baseband stages are designed with a smaller transconductance of 3mS. Capacitors C_1 - C_4 implement the required BB bandwidth cutoff frequency (f_{BW}) and noise shaping pole cutoff frequency (f_{NSP}) in the DSM filter. Their values were selected based on the final tuned Butterworth coefficients.

V. PERFORMANCE EVALUATION

The proposed DDSR was evaluated in a 28nm fully-depleted silicon-on-insulator (FD-SOI) process through transient and

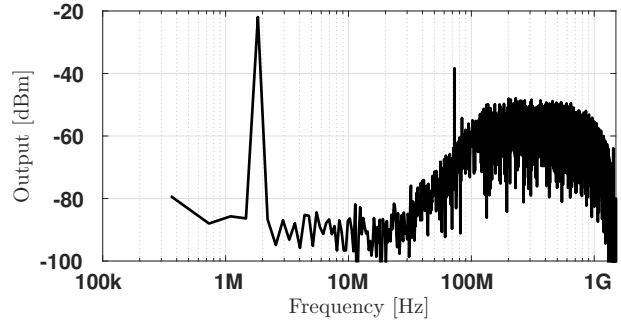


Fig. 3. Output spectrum at $f_{LO} = f_{CLOCK} = 1.5\text{GHz}$, Signal power $P_{IN} = -43\text{dBm}@f_{LO}+1.83\text{MHz}$, Blocker power $P_{BLOCKER} = -43\text{dBm}@f_{LO}+73\text{MHz}$ and BB bandwidth of 10MHz.

steady state analysis. The RX is reconfigurable from 0.7-2.7GHz with a BB bandwidth of 10MHz. Further, based on our previous implementation [4], we added estimated values of PCB and layout parasitics, I/O pad capacitances, bondwire inductances and s-parameter models of 20nH off-chip RF-chokes, and clock delay between quantizer and IDACs in order to match the simulated results more closely to the real scenario.

The spectrum of the the DDSR output bit stream is shown in Fig. 3. First, the desired in-band signal is amplified with around 20dB of RX gain. Second, the blocker is attenuated by the channel select filtering (CSF) response and third, the quantization noise is shaped by the DDSR feedback loop such that there is little in-band quantization noise left.

Figures 4 show the RX SNDR versus input signal and blocker powers. the RX achieves a maximum SNDR of 53dB at P_{IN} of -43dBm. Further, a decrease in SNDR is observed at blocker input powers greater than -35dBm for an input signal power of -80dBm. At low signal powers, the difference between ideal and simulated SNDRs is approximately equal to RX NF.

Figure 5 shows the simulated steady-state analysis results of DDSR gain and S_{11} . During the steady state simulations, the effects of quantizer and DACs were not considered. However, the results still reasonably match with the DDSR output spectrum in Figure 3. As desired, RX gain of 20dB is observed within 20MHz RF bandwidth. Further, a differential input impedance of 25Ω can be seen, which creates the required blocker attenuation at LNA input.

Figures 6 shows the simulated blocker input compression point (BCP), NF and RX gain. The RX achieves an BCP of -11.5dBm at 100MHz offset from the f_{LO} with a maximum receiver integrated NF of 6.2dB.

VI. CONCLUSION

A blocker resilient DDSR, with a low intrinsic input impedance front-end and optimized receiver gain, has been proposed which reduces the blocker gain at LNA input and output nodes. This ensures that the voltage swing limits are pushed towards much stronger blocker signals. For the desired frequency, input impedance is boosted to matched condition

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work ⁶	[3]	[4]	[1]	[2]
Carrier Frequency (GHz)	0.7-2.7	0.6-3	0.7-2.7	0.9	0.1-1.5
Gain (dB)	20	50	-	40	38
Noise Figure (dB)	5.6-6.2	2.4-3.5	5.9-8.8	6.2	1.5-2.9
Blocker input P1dB ¹ (dBm)	-11.5@10f _{BW}	-20@10f _{BW}	-14@10f _{BW} ²	-18@20f _{BW}	-17@10f _{BW}
OB IIP3 (dBm)	0@10f _{BW}	-10@10f _{BW}	-4@10f _{BW} ²	-	-
Peak SNDR (dB)	53	52	43	56	-
BB bandwidth (f _{BW}) (MHz)	10	10	7.5	28 ³	2
Power (mW) @ Supply voltage (V)	25@1 ⁵	35.5-53.5@1.2	90@1.1	80@1.2	11@0.7,1.2 ⁴
Architecture	LNA first DDSR	LNTA first DDSR	LNA first DDSR	LNA first DDSR	mixer first receiver
Process	28nm FDSOI	65nm CMOS	40nm CMOS	65nm CMOS	65nm CMOS

1) Blocker offset normalized to BB bandwidth (f_{BW}) 2) Extrapolated value 3) Usable BW with acceptable NF is limited to 4MHz 4) at RF 5) Power consumption of RX excluding quantizer and IDACs 6) Simulated response

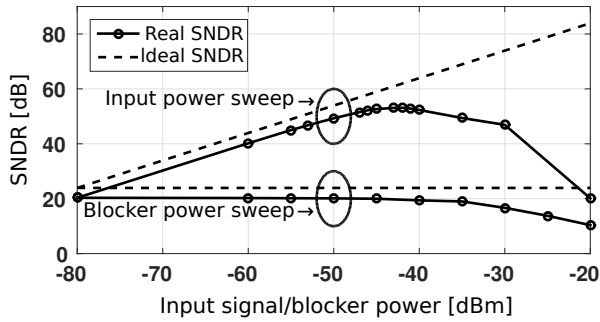


Fig. 4. SNDR vs. input and blocker power sweep for $f_{LO} = 1.5\text{GHz}$

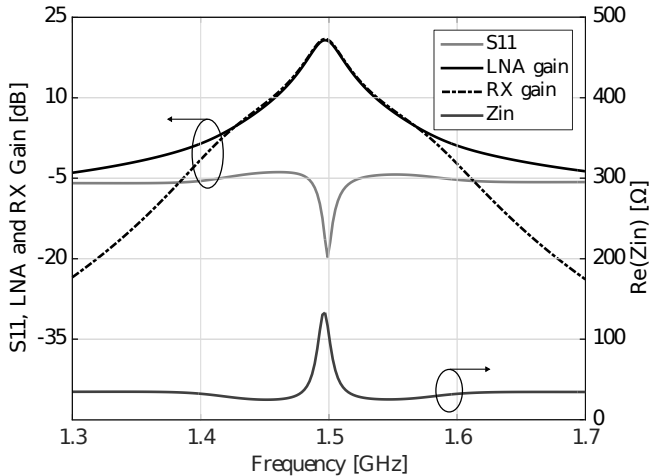


Fig. 5. Simulated S_{11} , LNA and BB gain for $f_{LO} = 1.5\text{GHz}$

through a positive up-converted feedback from BB. Simulated results show a OB-P1dB point of -11.5dBm at 100MHz offset from the desired received frequency, with maximum SNDR of 53dB and maximum NF of 6.2dB. Results collected into Table I indicate the proposed approach is able to achieve state-of-the-art blocker tolerance even with lower supply voltage.

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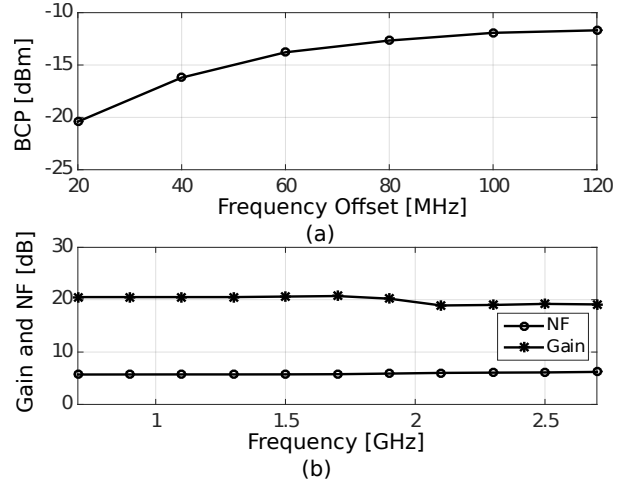


Fig. 6. (a) Blocker compression point (BCP) vs. frequency offset for the proposed receiver at $f_{LO} = 1.5\text{GHz}$. (b) RX gain and noise figure across the 0.7-2.7GHz operating band.

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