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*Published in:*
IEEE Solid State Circuits Letters

*DOI:*
10.1109/LSSC.2018.2875823

*Published: 01/01/2018*

*Document Version*
Peer reviewed version

*Please cite the original version:*
Power-Scalable Dynamic Element Matching for a 3.4-GHz 9-bit ΔΣ RF-DAC in 16-nm FinFET

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Abstract—This letter presents a hardware-efficient technique to scale the power consumption of dynamic element matching (DEM) DACs with the static back-off level of the digital input signal. Unlike previous DEM techniques, the proposed power-scalable approach disables parts of the DEM encoder and DAC elements when the digital signal level is decreased from full-scale, thus resulting in reduced power consumption and lower mismatch noise at the DAC output. Power-scalable DEM is particularly useful in digital-intensive RF transmitters, where 30–50 dB of signal power control may be performed in the digital domain. The concept is demonstrated for a 3.4-GHz 9-bit I/Q RF-DAC, utilizing bandpass delta-sigma modulation and DEM with programmable center frequency. The circuit is fabricated in a 16-nm FinFET process. When changing the digital back-off level of an LTE20 carrier from 0 to −18 dB, measurement results show a 72% reduction in total power consumption and 4.5-dB lower mismatch noise, achieved without performing any bias tuning or gain control in the analog domain. The digital delta-sigma modulator and DEM encoder consume less than 20 mW in full-scale mode.

Index Terms—Delta-sigma modulation, digital gain control, dynamic element matching (DEM), power back-off, RF-DAC.

I. INTRODUCTION

Dynamic element matching (DEM) continues to be a prime choice to improve the static nonlinearity of high-resolution DACs [1], [2]. By scrambling the order of the DAC elements on a sample-by-sample basis, DEM converts the distortion caused by static amplitude, timing, and pulse-shape mismatches into white or spectrally shaped noise. Because DEM is a purely digital algorithm, its implementation becomes increasingly attractive in the latest CMOS technology nodes, where high-speed low-cost digital logic can be successfully exploited to compensate for the larger analog device mismatches.

One important application of high-performance DEM DACs is in radio transmitters for wireless communications [3]–[5], where the aforementioned digitalization trend has strongly emerged during the past two decades. Modern radio standards utilize complex modulation schemes, wide channel bandwidths and stringent out-of-band (OOB) emission limits, thus imposing formidable speed and linearity requirements on the D/A conversion. Moreover, an additional design aspect in radio transmitters is the wide range of static signal power control required at the antenna, which can be as much as 75 dB for 3G user equipment. It is common to distribute such large gain control through the entire transmit signal chain, with 30–50 dB typically implemented in the digital domain [6]–[8]. Hence, in addition to high speed and linearity, the D/A conversion should also be optimized for signals with digital back-off, i.e., amplitude level smaller than the full-scale input range of the DAC.

Although the general idea of controlling a shuffler based on the signal amplitude was recently reported in one patent [9], to the authors’ best knowledge no details have been published on how to optimize an existing DEM algorithm for the scenario of digital back-off. In all previous circuit implementations, the DEM encoder operates always by assuming a full-scale input signal, thus scrambling all DAC elements although only a fraction of them would be required to perform the conversion. As explained in this letter, such non-optimal operation leads to wasted power, reduced effectiveness of the DEM algorithm, as well as higher mismatch noise at the DAC output. To solve these problems, we introduce a new power-scalable DEM technique, based on the segmented tree-structure encoder [10], where parts of the digital logic and DAC elements can be efficiently bypassed and disabled in back-off mode. The concept is experimentally validated for a prototype 9-bit I/Q ΔΣ RF-DAC, with block diagram shown in Fig. 1. Measurement results demonstrate that DEM operates effectively with up to −18 dB of static digital back-off, while achieving a reduction in system power consumption of up to 72% compared to the full-scale scenario. Even though this work discusses power-scalable DEM in the context of digital-intensive RF transmitters, the proposed method can be straightforwardly adopted in any DEM DAC application that utilizes digital gain control.

This letter is organized as follows. Section II introduces the concept of power-scalable DEM and its hardware-efficient realization. Section III describes the circuit-level implementation of the ΔΣ DEM RF-DAC. Measurement results are presented in Section IV, and Section V concludes the letter.

II. POWER-SCALABLE DEM

Fig. 2(a) shows the block diagram of a 6-bit tree-structure DEM encoder with signed data input [5], segmented into 4 unary-weighted MSBs and 2 binary-weighted LSBs. It consists of a cascade of switching blocks (SBs) [Figs. 2(b)–(d)] that iteratively split and switch their input signal $c[n]$ on a sample-by-sample basis, thus steering the data towards a different set of DAC elements at every clock cycle. Scrambling is performed within each SB by a pseudorandom sequence $s[n]$, which must satisfy

$$s[n] = \begin{cases} 0 & \text{if } c[n] \text{ is even} \\ \pm 1 & \text{if } c[n] \text{ is odd} \end{cases}$$

for segmenting and nonsegmenting SBs, and

$$s[n] = \begin{cases} 0 & \text{if } c[n] \text{ is odd} \\ \pm 1 & \text{if } c[n] \text{ is even} \end{cases}$$

for first-layer SBs.

Fig. 1. I/Q ΔΣ RF-DAC with digital gain control and power-scalable DEM.
Thanks to the modularity of the tree encoder, a 5-bit DEM DAC with
3+2 segmentation can be readily reconfigured from the original 6-bit
system, by rerouting the connections like in Fig. 3(a). The resulting 5-
bit tree encoder still operates as explained in [10], thus scrambling the
active DAC elements to ensure conversion of static mismatches into
pseudo-random noise. Furthermore, the excluded SBs can be disabled
by the means of conventional digital power-saving techniques (e.g.,
clock gating), while the unused DAC elements can be also turned
off if their internal circuitry allows it. The described method can be
trivially extended to a digital back-off of –12 dB [Fig. 3(b)] or any
multiple of –6 dB.

In practice, a direct implementation of the approach of Fig. 3
would require inserting multiplexers along the signal path. This is
undesirable because such multiplexers would prevent the synthesis
software to infer a single optimized datapath cell for multiple SB
adders, yielding lower quality-of-results (QoR). Fortunately, the extra
multiplexers can be avoided altogether by utilizing the trick displayed
in Fig. 4. By multiplying the input of a nonsegmenting SB by
\(2^N\), the signal is passed untouched across the following N SBs,
however, all the \(s[n]\) sequences are forced to zero by (1) and the factor
\(2^N\) is compensated by the 1/2 gain blocks. By varying N, the signal
is effectively rerouted to a different SB in the tree according to the
programmed level of digital back-off, like in Fig. 3. Note that the
factor \(2^N\) can be realized by left-shifting the signal by N positions,
thus no high-speed multiplexer is needed on the signal path.

III. CIRCUIT IMPLEMENTATION

Without loss of generality, this work demonstrates the effectiveness
of power-scalable DEM in the context of a 9-bit I/Q ΔΣ RF-DAC,
which is part of an all-digital transmitter [Fig. 1]. In the implemented
system, the ΔΣ modulator and DEM encoder realize a bandstop
transfer function with center frequency programmable over the entire
Nyquist range. The purpose is to create a notch in the OOB spectral
density at a specific frequency offset from the transmit band, in order
to ease coexistence with nearby receivers [3], [5].

Fig. 5 depicts the top-level block diagram of a single quadrature
branch. The 9-bit RF-DAC is segmented into 4 unary-weighted MSBs
(i.e., 16 elements with weight 32) and 5 binary-weighted LSBs.
To reduce complexity of the digital circuitry, only the 6 MSBs are scrambled by the power-scalable DEM encoder, whereas the 3 LSBs directly drive the corresponding RF-DAC elements, since their mismatch-noise contribution has been verified through simulations to be negligible. Pipeline registers are inserted along the signal path, enabling a sample rate equal to 1/4 the carrier frequency. The encoder supports four power-scaling modes for digital back-off levels smaller than 0, −6, −12, and −18 dB, with extensive clock-gating logic used to reduce power consumption of the disabled SBs. Digital power control is performed by adjusting the gain signal \( P_{\text{CTRL}} \) (visible also in Fig. 1) with the wanted resolution, followed by selecting the correct DEM power-scaling mode as shown in Fig. 5. Even though the range of \( P_{\text{CTRL}} \) can be as large as 50 dB [8], no additional modes for back-off levels lower than −18 dB are implemented, since the practical benefits of power-scalable DEM would be negligible at such low signal amplitudes. Because power control in a transmitter system is adjusted between radio frames, when no signal is being transmitted, any transient caused by switching the DEM encoder to a different power-scaling mode (e.g., supply noise) is not critical.

Fig. 6 discloses the implementation details of the sequence generator internal to each SB. It resembles a \( \Sigma \) modulator without signal input, where the special quantizer is designed to satisfy (1) or (2). By modeling the quantizer as additive random error, it can be shown that the circuit generates a pseudorandom sequence shaped by

\[
\text{NTF}(z) = \frac{1 - \alpha z^{-1} + z^{-2}}{1 - r \alpha z^{-1} + r^2 z^{-2}}
\]

which is a bandstop transfer function with programmable coefficients \( \alpha \) and \( r \). The value of \( \alpha = 2 \cos(2\pi f_0/F_s) \) determines the notch offset \( f_0 \) for a given sample rate \( F_s \), while \( r \) mainly affects the stability of the \( \Sigma \) loop through the maximum magnitude of NTF(\( z \)) in the passband [3]. All measurements in this work use \( r = 0.75 \), which is a good compromise between stability, spectral performance, and ease of implementation. Note that (3) is also the noise transfer function implemented by the \( \Sigma \) modulator preceding the DEM encoder, which decreases the signal wordlength from 14 to 9 bits. Thanks to the constraint \( s[n] \in \{-1, 0, +1\} \), the \(- (1 - r) \alpha \) and \( 1 - r^2 \) programmable taps in Fig. 6 are replaced by simple 3-way multiplexers with pre-computed inputs. The remaining arithmetic is arranged into a single multiply-accumulate operation, thus providing the best QoR in terms of propagation delay and hardware complexity.

The 9-bit RF-DAC implements a high-speed current-steering architecture. As shown Fig. 7(a), each unity-weighted conversion element consists of a digital mixing circuit, two AND gates for 25% duty-cycle generation, and two symmetrical current-steering branches built of a current source (CS) in series with a switch [5]. An element with weight \( W_i \) is formed by parallel connection of \( W_i \) units. The operating principle is illustrated by the waveforms in Fig. 7(b), where the 4x relation between sample period \( T_s \) and carrier period \( T_c \) can be observed. Depending on the selected power-scaling mode, the \( i \)-th DEM encoder output \( b_i[n] \) either switches between +1 and −1, or is constant 0 [Fig. 3]. When \( b_i[n] = \pm 1 \), the element is enabled and performs digital-to-RF conversion normally. When \( b_i[n] = 0 \), both current-steering branches are disabled, thus significantly decreasing RF-DAC current consumption in digital back-off.

The I/Q RF-DAC is integrated with an on-chip balun as part of a prototype cellular system-on-chip, targeted for the 3.4–4.9-GHz frequency band. The chip is fabricated in a 16-nm FinFET process, with micrograph shown in Fig. 8. The circuit utilizes three separate supply domains: 0.8 V for the synthesized digital part, 1.0 V for the digital mixers, and 1.2 V for the current-steering RF-DACs. The overall linearity of the transmitter is verified to comply to the specifications of the supported cellular standards. All measurements reported in this letter are performed with an LTE20 carrier at various levels of digital back-off from the full-scale output power of +3 dBm.

Fig. 9 shows the OOB spectra of the I/Q RF-DAC in three configuration modes: linear quantization (both \( \Delta \Sigma \) modulation and DEM bypassed), \( \Delta \Sigma \) modulation without DEM, and \( \Delta \Sigma \) modulation.
RF-DAC utilizing programmable bandpass ΔΣ modulation and DEM, but the results can be straightforwardly extended to any DEM DAC application that utilizes digital gain control.

TABLE I

<table>
<thead>
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<tbody>
<tr>
<td>Active area</td>
<td>65-nm CMOS</td>
<td>130-nm SiGe</td>
<td>16-nm FinFET</td>
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<td>1.2V</td>
<td>1.5V, 1.8V, 2V, 2.5V, 3.3V</td>
<td>0.8V, 1.0V, 1.2V</td>
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<td>Resolution</td>
<td>6.15 bits</td>
<td>3 bits</td>
<td>9 bits</td>
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<td>2.4–2.7 GHz</td>
<td>0.5–2.25 GHz</td>
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<td>ΔΣ modulator</td>
<td>lowpass</td>
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<td>Test signal</td>
<td>@ 2.45GHz</td>
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<td>LTE20</td>
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<td>ΔΣ sample rate</td>
<td>4.9 GS/s</td>
<td>2 GS/s</td>
<td>0.85 GS/s</td>
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<td>Max. P_{out}</td>
<td>+26 dBm</td>
<td>–10 dBm</td>
<td>+3 dBm</td>
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<td>OOB noise</td>
<td>–149 dBm/Hz(3)@ –500MHz</td>
<td>–131 dBm/Hz(4)@ 100MHz</td>
<td>–143 dBm/Hz@ 100MHz</td>
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<tr>
<td>Power cons.</td>
<td>254mW @ 0dB</td>
<td>151mW @ –6dB</td>
<td>170mW @ –6dB</td>
</tr>
</tbody>
</table>

(1) ΔΣ modulators + RF-DACs
(2) 0-dB measurement loss de-embedded
(3) excluding LDVS receivers
(4) only digital back-off

ACKNOWLEDGMENT

The authors are grateful to F. Steininger for his advice on DSP optimization, to P. Stynen for the digital integration, and to K.-F. Bink for the lab support.

REFERENCES


