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A 3-43ps time-delay cell for LO phase-shifting in 1.5-6.5GHz beamsteering receiver

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***Abstract*—This paper describes a digital-friendly passives-less time delay cell that generates programmable phase-shifts for downconverting front-end in LO-based beamsteering receiver. Cell design supports 1.5-6.5GHz broadband receiver operation and cell layout occupies an area of only 15x16.5μm^2 including power supply rails and control logic. Simulated in 28nm CMOS technology, delay cell exhibits 6 distinct delay values {3, 3.5, 17, 19, 24, 43}ps consuming at most 220μW@1V.**

I. Introduction

Next generation receivers will rely on phased-array antennas and beamsteering structures. Nowadays, fifth generation (5G) systems already utilize multiple-input multiple-output (MIMO) architectures, calling for parallel front-ends serving multiple antennas in arrays. Phased-arrays of uniformly spaced antenna elements enable receivers to filter interferers in spacial domain and elevate signal-to-noise ratio (SNR) [1]. Antenna arrays also enable parallel data streams in wireless transmission, therefore, directivity, range, and throughput are enhanced in these architectures.

In the free space beamsteering (modeled in [2] by two antenna elements at a distance d, Fig. 1a) time delay Δt in arrival to the second antenna element from an angle θ does not depend on carrier frequency f:

$$\Delta t = \frac{d \sin\theta}{300\ Km/s} \tag{1}$$

This allows Δt-controlled phase-shift ($\Delta\phi = 2\pi f \times \Delta t$) between the in-beam signals and enables their coherent summation to increase SNR. The mm-wave phase-shifters can be applied at either RF [3] or LO [4] parts of generic receiver (Fig. 1b) and exploit passive structures, summarized in [5]. While such components impede scaling, consume area and introduce additional RF losses, in a low-GHz range new active and scaling-friendly techniques deserve exploration. CMOS scaling, where transistor speed f_T has increased from 16GHz at 0.5μm to 400GHz at 22nm process node, potentially enables wide frequency range delaying (Δt in (1)) and might serve as a feasible alternative to traditional phase-shifters.

In this work we propose a concept, analysis and implementation of a wideband digital-friendly passives-less time-delay cell to generate a range of programmable fine delays for LO-based beamsteering receiver. Specifically, chaining the proposed delay cells makes the total phase-shift sufficient

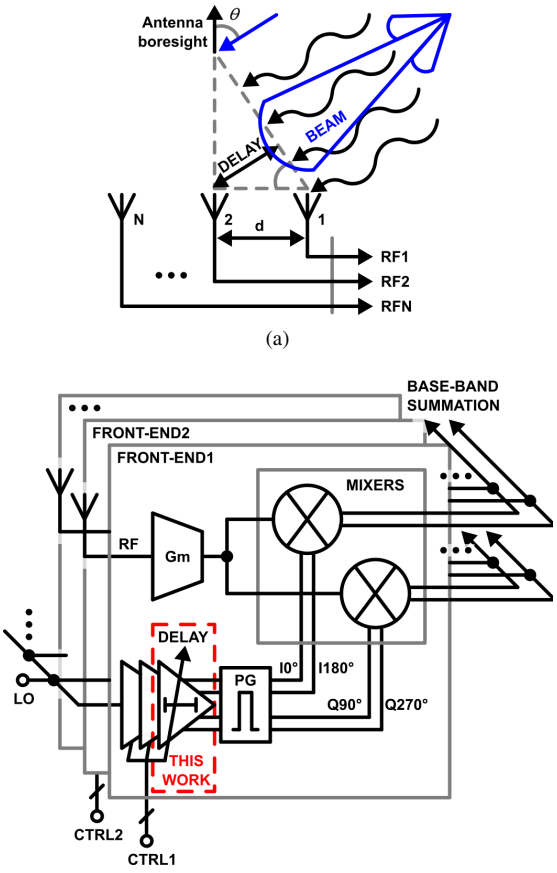


Fig. 1. (a) Concept of beamsteering; (b) conceptual diagram of the receiver.

for practical beamsteering applications. When coupled with pulse generation circuitry (PG), such delay line can drive the quadrature passive mixer in a low-GHz downconverting front-end. Unlike published works [6], [7], the code-controlled delay is produced a) without explicit passives array b) by minor change of the waveform shape in asymmetrical multiplexers or/and c) by blending waveform copies at common nodes of these multiplexers.

In the section II of the paper delay cell circuitry is presented along with analysis of its idealized model. Delay cell simulation results in 28nm process are given in section III for the circuit with physical device models and cell layout with RC-extracted parasitics. Section IV concludes the paper.

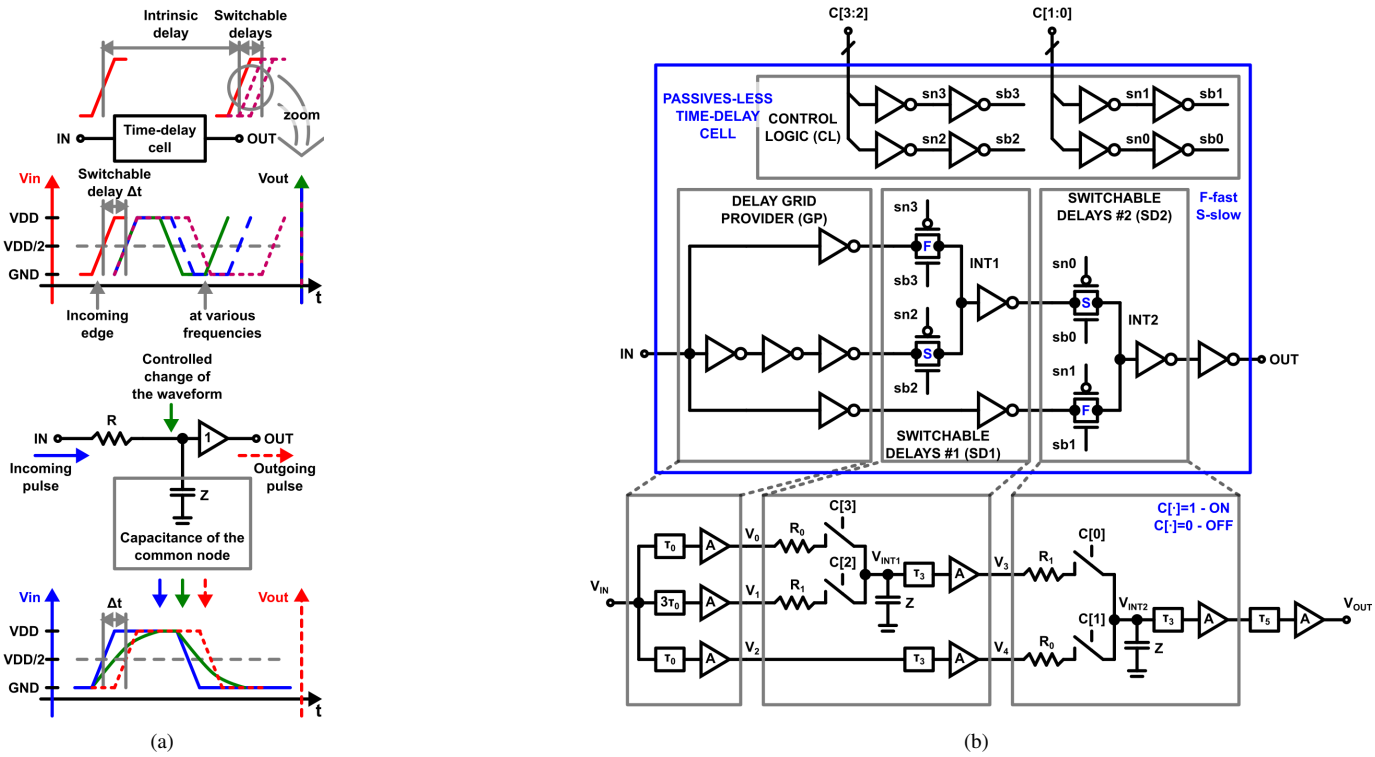


Fig. 2. (a) Definition of delays in this work and proposed delaying principle; (b) implemented delay cell schematic with its idealized model.

II. Proposed Delay Cell

A. Delaying principle

Outlined in Fig. 2a, a digital-friendly delaying method of this work relies on 1) removing amplitude information from delayed waveform to create sharp rail-to-rail edges, 2) controlled distortion of the waveform at the intermediate stages to create time-lag and 3) reinforcement of the edges steepness at subsequent stages for further processing. The latter enables chaining of the cells into the delay line.

B. Delay cell circuit

The main motivation behind the presented cell design is to enable passives-less delaying with code-controlled tunability in a wide frequency range. Proposed delay cell structure (Fig. 2b) includes delay grid provider (GP), interconnected switchable delays (SD) and associated control logic (CL). The delay grid replicates the incoming pulse to create multiple copies that will be subject to delaying and multiplexing. Note that the delaying core is fully compatible with the digital-flow, since switchable delays are essentially multiplexers with asymmetrical (slow and fast) and independently controlled input-output paths. Different from known approach of multiplexing various chains of inverters, in the proposed design controlled delay originates in the asymmetrical multiplexer itself which facilitates compact design, reduces intrinsic delay of the entire cell and increases its operation frequency. Control options, activated by bits C[3:0], enable independent passage as well as blending of the delayed waveforms at common nodes INT1 and INT2.

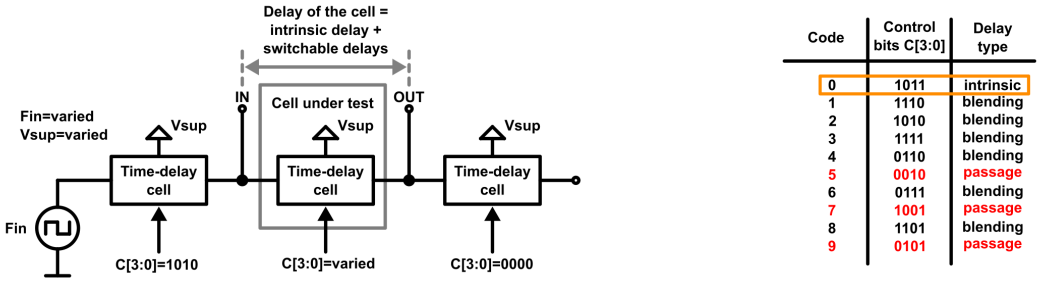
C. Delay cell model

To quantify waveform distortion and yield insight into the corresponding delay a mathematically-simple model is provided. The model includes charge storage elements representing capacitance of the common nodes INT1,2 and current limiting resistors representing drain-to-source channels of transmissions gates. Inverting and switching functions are assumed to be ideal (i.e. frequency independent with zero current leakage).

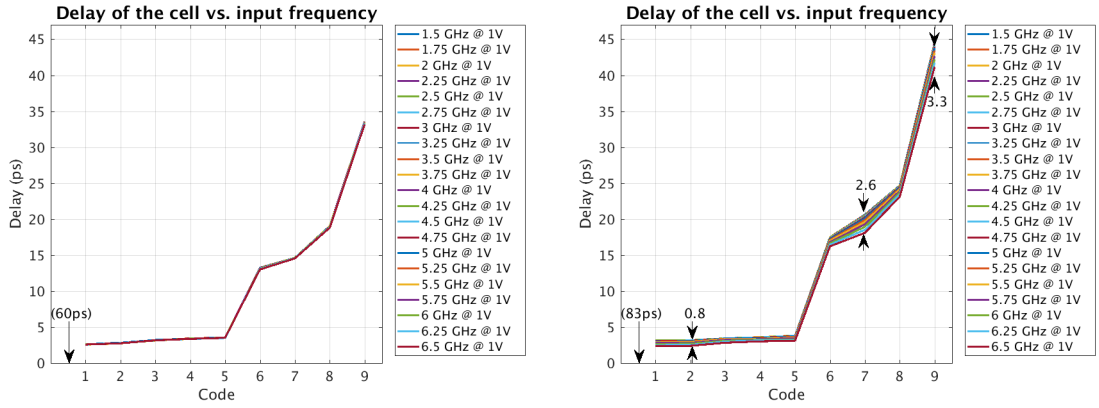
Going through the nodes of the delay cell model in Fig. 2b it is possible to obtain system of equations describing the cell:

$$\begin{cases} V_0 = V_{IN} \times e^{-s\tau_0} \times A \\ V_1 = V_{IN} \times e^{-s3\tau_0} \times A \\ V_2 = V_{IN} \times e^{-s\tau_0} \times A \\ V_{INT1}\left(\frac{C[3]}{R_0} + \frac{C[2]}{R_1} + \frac{1}{Z}\right) = \frac{C[3]V_0}{R_0} + \frac{C[2]V_1}{R_1} \\ V_3 = V_{INT1} \times e^{-s\tau_3} \times A \\ V_4 = V_2 \times e^{-s\tau_3} \times A \\ V_{INT2}\left(\frac{C[1]}{R_0} + \frac{C[0]}{R_1} + \frac{1}{Z}\right) = \frac{C[0]V_3}{R_1} + \frac{C[1]V_4}{R_0} \\ V_{OUT} = V_{INT2} \times e^{-s\tau_3} \times A \times e^{-s\tau_5} \times A, \end{cases} \tag{2}$$

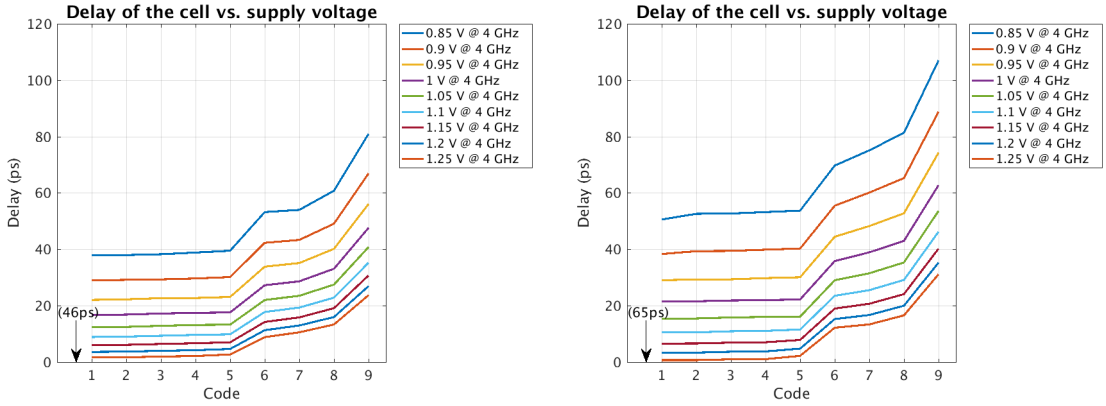
where $Z = \frac{1}{j\omega C}$ and $A = -1$. By specifying $C[\cdot] \in \{0; 1\}$ one can solve above set of equations for transfer function $\frac{V_{OUT}}{V_{IN}}$ of the delay cell corresponding to chosen code.



(a)



(b)



(c)

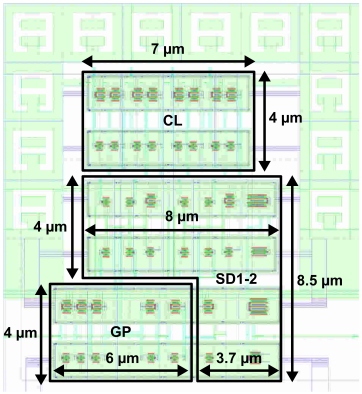
Fig. 3. (a) Simulation testbench with exercised codes and (b)-(c) simulation results for the cell circuit with physical device models (left column) and cell layout with RC-extracted parasitics (right column). Shown in parenthesis is the smallest intrinsic delay of the cell; bounded with arrows is the delay spread.

Three illustrative codes, for which transfer functions are obtained in closed analytic form, are collected in Table I. Actual delays between decision threshold crossings (i.e. Vin=Vout=VDD/2 in Fig. 2a) are obtained by applying a step excitation $\mathcal{L}^{-1}(u(t)) = U(s) = 1/s$ to the delay cell transfer functions and then returning to the time domain with inverse Laplace transform $\mathcal{L}^{-1}$ [8].

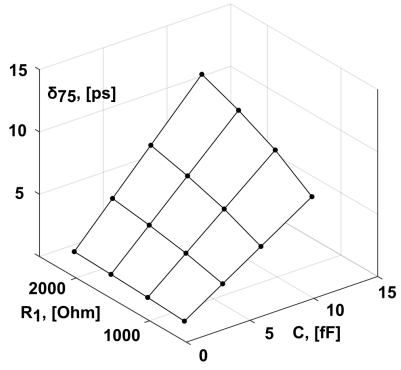
In order to illustrate dependencies in the model, parameterized waveforms of the responses from Table I are plotted in MATLAB with the values of parameters: $\tau_0 = 11$ps@1V, $\tau_3 = 12$ps@1V, $\tau_5 = 14$ps@1V, $R0 = 600$Ohm, $R1 = 700$Ohm and $C = 1$fF. Additionally, switchable delay δ_{75} (enabled with code 7 to code 5 transition) is exhibited in Fig. 4b as a function of R_1 and C values in the delay cell model.

III. Circuit- and Layout Simulation Results

To demonstrate wide range frequency independent delay, a complete design has been simulated in Eldo under different supply voltages with a range of input frequencies. Simulation results for the circuit with physical device models and full cell layout with RC-extracted parasitics are given in Fig. 3. Power consumption of the laid out cell ranges from 50μW@1.5GHz to 220μW@6.5GHz with supply of 1V.



(a)

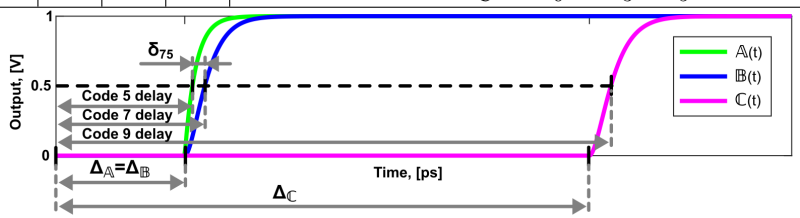


(b)

Fig. 4. (a) Implemented delay cell layout; (b) code 7 and code 5 delays difference δ_{75} for changing R_1, C values in the model.

TABLE I
ILLUSTRATIVE OUTPUT RESPONSES OF THE DELAY CELL MODEL TO APPLIED UNIT STEP EXCITATION

Code	Control bits C[·]				3 distinct code-enabled input-to-output passage delays
	[3]	[2]	[1]	[0]	
5	0	0	1	0	$(1-e^{-\frac{t-\Delta_{\mathbb{A}}}{R_0C}})u(t-\Delta_{\mathbb{A}}) = \mathbb{A}(t)$ $\Delta_{\mathbb{A}} = \tau_0 + 2\tau_3 + \tau_5$
7	1	0	0	1	$\left(1-\frac{1}{R_0-R_1}\left(R_0e^{-\frac{t-\Delta_{\mathbb{A}}}{R_0C}} - R_1e^{-\frac{t-\Delta_{\mathbb{A}}}{R_1C}}\right)\right)u(t-\Delta_{\mathbb{A}}) = \mathbb{B}(t)$ $\Delta_{\mathbb{B}} = \Delta_{\mathbb{A}} = \tau_0 + 2\tau_3 + \tau_5$
9	0	1	0	1	$(1-e^{-\frac{t-\Delta_{\mathbb{C}}}{R_1C}}(1+\frac{t-\Delta_{\mathbb{C}}}{R_1C}))u(t-\Delta_{\mathbb{C}}) = \mathbb{C}(t)$ $\Delta_{\mathbb{C}} = 3\tau_0 + 2\tau_3 + \tau_5$



The delay cell is implemented in 28nm 1P8M CMOS and occupies an area of 15x16.5μm^2. The layout is shown in Fig. 4a with block acronyms and corresponding dimensions. Functional blocks are floorplaned to allow vertical and horizontal mirroring of the cell layout for convenient chaining.

IV. Conclusion

In this work we introduced a concept and implementation of wideband digital-friendly passives-less time-delay cell. Mathematical analysis demonstrated that the cell exhibited 6 distinct delay values and extracted layout simulations in 28 nm CMOS showed these values to be {3, 3.5, 17, 19, 24, 43}ps in 1.5-6.5GHz range from nominal supply of 1V.

In the context of low-GHz beamsteering, proposed wideband delay cell might serve as a scaling-friendly alternative to traditional phase-shifters.

Acknowledgment

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