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A Configurable Hysteresis Comparator for Asynchronous Sigma-Delta Modulators

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***Abstract*—This paper describes a configurable hysteresis comparator for asynchronous sigma-delta modulators (ASDM). The proposed comparator provides coarse and fine tuning options for configuring the loop delay and hence the frequency of an ASDM. The post-layout simulation of the comparator implemented in a 28 nm FDSOI process shows that the comparator provides hysteresis voltage range of ±(1 to 15.3) mV while consuming 36.8 nW to 4.4 μW from 0.7 V supply, which enables configurable ASDM center-frequency in the range of 100 kHz to 6 MHz.**

I. Introduction

Asynchronous sigma-delta modulator (ASDM) has recently gathered interest as an analog-to-digital converter and as a pulse encoder for analog signals, which improves the properties of analog-to-digital conversion [1], [2]. Asynchronous sigma-delta modulators were first introduced in 1981 as a technique for generating frequency modulation in communication systems [3]. The design of ASDMs has since evolved even though it is under-explored compared to the well known synchronous sigma-delta modulators. The main advantage of asynchronous sigma-delta modulators over synchronous sigma-delta modulators is that there is no need of additional sampling clock for the quantizer [1], [4]. Instead in an ASDM, sampling occurs during digital signal processing of the modulator output. As a result, the quantizer is replaced with a comparator that exhibits hysteresis, which makes the comparator an important component in the design of ASDMs.

One of the key design parameters of ASDMs is the delay in the sigma-delta modulator loop because it determines the center frequency of an ASDM. The design requirements of the comparator used in an ASDM is typically determined by the structure of the ASDM. The fully differential ASDM presented in Fig. 1 uses the comparator as a quantizer and delay-tuning block. The comparator converts the continuous-time modulated signal from the integrator (INT) to variation in the pulse-width and duty-cycle of the generated pulse train. In addition, the comparator is used to adjust the delay within the ASDM loop by controlling the switching times of the generated pulse edges based on the hysteresis voltage of the comparator.

Further, the resolution of the ASDM is determined by the center frequency of the modulator in relation to the input signal frequency [2]. Hence, it is desirable to keep the center frequency of the ASDM far from the signal frequency in order to prevent aliasing of the center frequency and its harmonics within the signal bandwidth. On the other hand, using high center frequencies for the ASDM comes at the cost of high power consumption. In addition, using high center frequencies puts higher constraints on further processing of the ASDM output in digital domain. For instance, the sampling rate

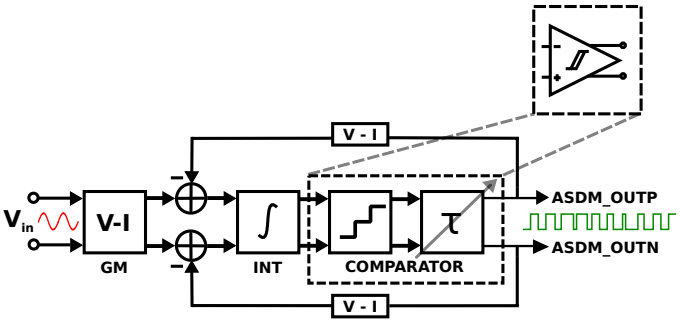

Fig. 1. A fully differential asynchronous sigma-delta modulator with configurable hysteresis comparator for controlling the loop delay of the modulator.

required during digital signal processing increases as the center frequency increases, which results in considerable high power consumption from the required digital logic. Thus, there is a need to be able to configure appropriate center frequency for optimized performance of the ASDM. This flexibility is achieved in the ASDM shown in Fig. 1 by controlling the hysteresis voltage of the comparator which results in configurable loop delay.

In this paper, we present a fine resolution configurable hysteresis comparator with coarse-fine tuning scheme. The tuning scheme is used to control the center frequency and loop delay of the ASDM in Fig. 1. The designed comparator enables a tuning range of 100 kHz to 6 MHz for the center frequency of the ASDM and loop delay tuning range of 14.4 ns to 5.1 μs. The paper is organized as follows: Section II describes the main design parameters for achieving the configurability of the comparator and the circuit implementation. Section III presents post-layout simulation results and the performance of the proposed circuit is summarized in Section IV.

II. Proposed Design

Hysteresis comparators are widely used in analog design to mitigate false threshold detections from small and noisy input signals. In ASDMs, the hysteresis property can also be used to control the propagation delay of the comparator, which in turn provides control over the ASDM center frequency. Tuneable delays can also be achieved with delay lines, inverter chains and phase locked loops (PLLs) [5]. However, using a comparator for the target ASDM application provides a power- and area-efficient solution when compared to inverter chain solutions. In addition, by using the comparator to achieve tuneable delay, we are able to use a single circuit as a quantizer

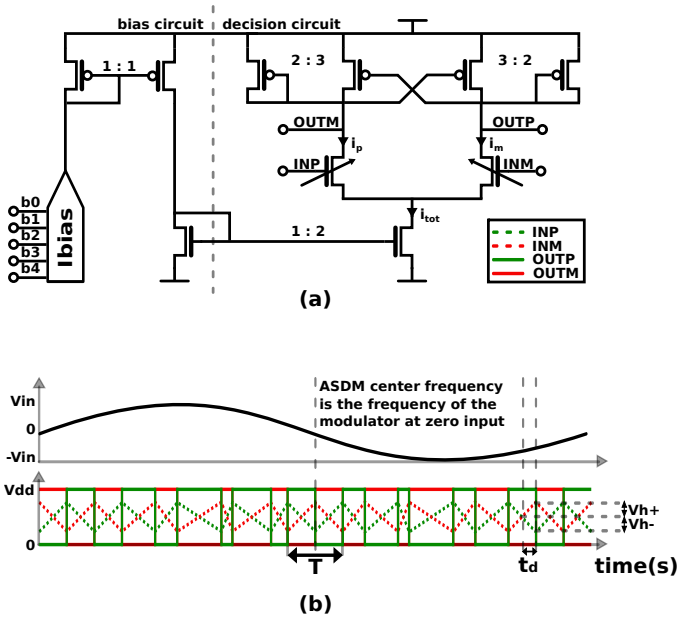

Fig. 2. (a) Schematic of the configurable hysteresis comparator (b) Diagram showing key design parameters from the input and output waveforms of the comparator, which also represents the output of the ASDM.

for decision making and delay tuning, which results in reduced design complexity, power consumption and the required area.

A. Design parameters

The design of the proposed configurable hysteresis comparator is optimized to provide a wide delay tuning range for controlling the center frequency of asynchronous sigma-delta modulators. The proposed configurable hysteresis comparator is presented in Fig. 2. The proposed design utilizes two main control parameters for providing coarse and fine tuning of the ASDM loop delay. These two control parameters are the bias current of the comparator (I_{bias}) and the width of the input transistors (W_{in}). Both parameters are used to adjust the hysteresis voltage (Vh) by controlling the tail current (i_{tot}) and transconductance ($g_m(in)$) of the input differential pair. The adjustable hysteresis voltage changes the propagation delay of the comparator (t_d), which in turn changes the loop delay (τ_{delay}) and the center frequency of the ASDM (F_{center}). The center frequency of the ASDM is the frequency when the input voltage (V_{in}) of the modulator is zero.

The configurable bias current (I_{bias}) is responsible for the coarse tuning of the comparator hysteresis while fine tuning of the comparator hysteresis is achieved by the configurable input transistor width (W_{in}). The relationship between I_{bias}, W_{in} and the hysteresis voltage (Vh) at the switching point of the comparator can be derived [6] from:

$$Vh_{-} = -Vh_{+} = \frac{i_{tot}}{g_m(in)} \cdot \frac{\delta - 1}{\delta + 1} \tag{1}$$

$$g_m(in) \approx \sqrt{\frac{i_{tot} \cdot \mu C_{ox} \cdot W_{in}}{L_{in}}} \ , \tag{2}$$

where δ represents the ratio between the widths of the cross-coupled PMOS transistors and the diode-connected PMOS transistors of the comparator. The comparator exhibits feedback, when the cross-coupled PMOS transistors in parallel with the diode-connected load transistors create a positive feedback loop. This is fulfilled when δ is chosen to be > 1, causing the PMOS load to effectively act as a negative resistance. Ideally $\delta = 1$ in a comparator without hysteresis, where switching occurs at the comparator ouputs (OUTP, OUTM) when the comparator inputs (INP, INM) become equal and i_p and i_m currents are equal. On the other hand, $\delta > 1$ introduces an imbalance between i_p and i_m currents when the comparator inputs (INP, INM) are equal, given as:

$$i_p = \frac{1}{\delta} i_m \ . \tag{3}$$

The difference between i_p and i_m currents is compensated as the comparator input voltages (INP, INM) increase/decrease from the initial switching point when both comparator inputs were equal. This additional voltage compensation is the hysteresis voltage ($\pm Vh$), which causes the switching point of the comparator to be shifted in order to balance i_p and i_m currents as depicted in Fig 2. For this implementation, $\delta = 3/2$ has been chosen because it provides sufficient imbalance between i_p and i_m currents, and thus hysteresis. Hence, the propagation delay (t_d) of the comparator is extended by the time required for i_p and i_m currents to become equal, in order for the logic state at the comparator output to change as illustrated in Fig 2. Thus, the propagation delay (t_d) of the comparator is controlled by changing the hysteresis voltage (Vh), which is derived by substituting (2) in (1)

$$\pm Vh \approx \frac{i_{tot}}{\sqrt{\frac{i_{tot} \cdot \mu C_{ox} \cdot W_{in}}{L_{in}}}} \cdot \frac{\delta - 1}{\delta + 1} \ . \tag{4}$$

Further, the ASDM loop delay (τ_{delay}) is the total time delay in the modulator loop which is determined mainly by the propagation delay (t_d) of the comparator and the total RC-delay (τ_{RC}) in the loop. In addition, the instantaneous period of the modulator output (T_{asdm}) depends on the ASDM loop delay as presented in equation (5b), where K_{int} represents the effect of the integrator gain [7], [8]

$$\tau_{delay} \approx t_d + \tau_{RC} \ , \ t_d \propto |Vh| \tag{5a}$$

$$\Rightarrow T_{asdm} \approx K_{int} \cdot \tau_{delay} \ . \tag{5b}$$

The hysteresis voltage of the comparator has an inverse relationship with the center frequency of an ASDM [1], [8]. Hence, the relationship between the comparator hysteresis voltage, loop delay and center frequency of the ASDM can be expressed as:

$$F_{center} = \frac{\pi f_{int}}{2|Vh|} = \frac{1}{T_{asdm}} \propto \frac{1}{\tau_{delay}} \tag{6a}$$

$$\Rightarrow F_{center} \propto \frac{\sqrt{I_{bias} W_{in}}}{I_{bias}} \ , \tag{6b}$$

where f_{int} is the unity gain frequency of the integrator. This implies that, the resolution of the ASDM can be maximized based on equation (6b) by using the bias current and input width of the proposed comparator to optimize key design parameters as follows:

- Hysteresis voltage (Vh) should be minimized.

- Loop delay (τ_{delay}) should be minimized.
- Center frequency (F_{center}) should be maximized.

B. Circuit Implementation

The complete schematic of the proposed configurable hysteresis comparator is presented in Fig. 3 showing the fine and coarse tuning configuration options. The comparator utilizes positive feedback to boost the gain of the decision making circuit. The feedback coefficient is the δ ratio between the widths of the cross-coupled transistor and the diode-connected transistor. Furthermore, the integrator preceding the comparator stage within the ASDM loop serves as as a pre-amplifier for the comparator stage as illustrated in Fig. 1. In addition, a chain of inverters are connected at the ouput of the comparator to further boost the ouput voltages (OUTP, OUTM) for subsequent processing in the DSP module.

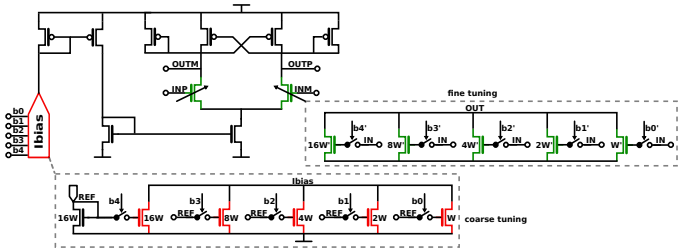

Fig. 3. Full schematic of the proposed comparator with all configuration options (Ibias, Win) for coarse and fine tuning of the comparator.

The proposed configurable hysteresis comparator is designed based on the design parameters discussed in Section II-A for achieving coarse and fine tuning of the ASDM. Fig. 3 presents the circuit implementation of the configurable bias current (I_{bias}) for coarse tuning of the ASDM. The bias current is configured with dedicated 5-bits digital control (b_0, b_1, b_2, b_3, b_4). Each control bit is assigned to dedicated switches at the input of differently sized current mirror transistors (W, $2W$, $4W$, $8W$, $16W$). Thus, a wide range of bias currents can be provided by enabling a set of control bits based on the desired center frequency of the ASDM. This method of implementing a digitally controlled current source is also known as current-steering digital-to-analog current source (IDAC) [6].

The circuit implementation of the configurable input transistor widths (W_{in}) for fine-tuning of the ASDM is also shown in Fig. 3. The input transistor width is configured with dedicated 5-bits digital control ($b_0^{'}$, $b_1^{'}$, $b_2^{'}$, $b_3^{'}$, $b_4^{'}$). Each control bit is connected to a dedicated switch at the input gate of differently-sized transistor widths ($W^{'}$, $2W^{'}$, $4W^{'}$, $8W^{'}$, $16W^{'}$). Hence, a wide range of transistor width and input capacitance can be configured by enabling a set of digital control bits based on the desired loop delay and center frequency of the ASDM.

III. Post-Layout Simulation Results

The proposed configurable hysteresis comparator was implemented in a 28 nm FDSOI process. Fig. 4 shows the layout of the proposed comparator circuit with an area of 0.00135mm^2. The performance of the comparator was evaluated within the asynchronous sigma-delta modulator loop in order to demonstrate the effect of the comparator coarse-fine

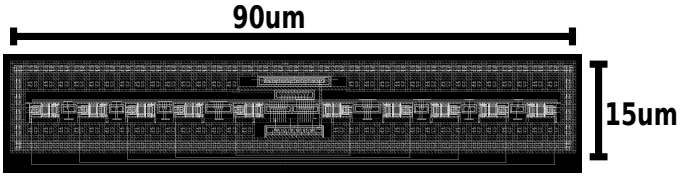

Fig. 4. Layout of the configurable hysteresis comparator implemented in a 28 nm FDSOI process

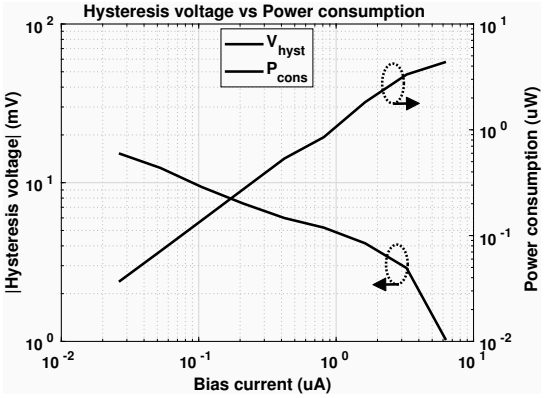

Fig. 5. Coarse tuning range of the comparator hysteresis and the corresponding power consumption of the comparator.

tuning configurations on the ASDM loop delay and center frequency.

The main configurable parameters (I_{bias}, W_{in}) of the comparator are varied independently with dedicated digital control bits and the effect of each parameter on the hysteresis voltage (V_{hyst}) and power consumption (P_{cons}) of the comparator is studied. Fig. 5 presents the comparator hysteresis voltage range and corresponding power consumption of the comparator over the configurable bias current range, where it can be observed that the power consumption of the comparator increases as hysteresis voltage decreases as a result of increase in I_{bias}. In addition, coarse tuning of the ASDM center frequency is achieved by varying the bias current (I_{bias}) around a fixed input transistor width configuration ($W_{in} = 4W^{'}$). Fig. 6 shows that the loop delay (τ_{delay}) decreases as the bias current I_{bias} increases, while the center frequency of the ASDM (F_{center}) increases with increase in I_{bias}. The comparator consumes 36.8 nW for the minimum center frequency of 100 kHz as observed from Fig. 5 and Fig. 6.

The effect of varying the comparator input transistor width (W_{in}) on the hysteresis voltage (V_{hyst}) and power consumption (P_{cons}) of the comparator is presented in Fig. 7. It can be observed from Fig. 7 that the proposed comparator is able to provide fine hysteresis voltage steps which enables fine tuning of the ASDM loop delay and center frequency, by varying W_{in} around a fixed bias current configuration. Fig. 8 shows the fine tuning range of the ASDM loop delay and center frequency around 900 kHz which is set by the fixed bias current configuration (I_{bias} = 200 nA). The proposed comparator achieves fine tuning delay steps of 1 ns and center frequency tuning steps of 1 kHz which corresponds to about 1 mV change in hysteresis voltage and sub-nW change in power consumption per fine-tuned delay step.

In summary, varying the input transistor width of the pro-

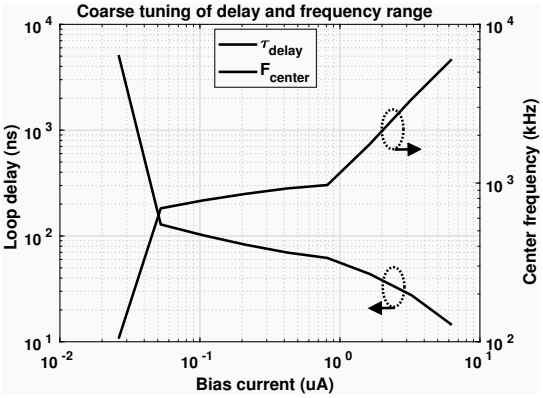

Fig. 6. Coarse tuning range of the ASDM loop delay and center frequency range by changing the bias current of the configurable hysteresis comparator.

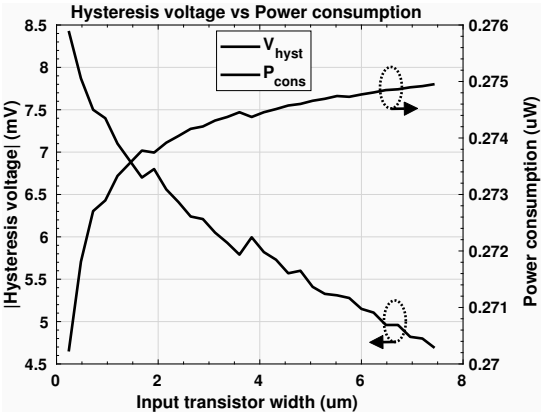

Fig. 7. Fine tuning range of the comparator hysteresis and the corresponding power consumption of the comparator around F_{center} = 900 kHz.

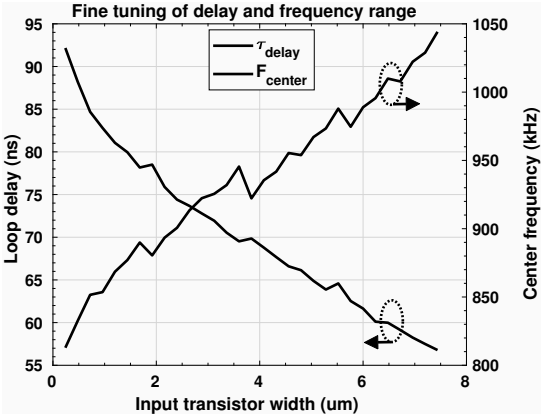

Fig. 8. Fine tuning range of the ASDM loop delay and center frequency range around 900 kHz, by controlling W_{in}.

posed comparator provides small delay steps while varying the bias current of the comparator provides significant change in delay steps. The combination of both configurable parameters makes the proposed comparator a useful circuit in the design of configurable ASDMs. The performance of the proposed comparator is summarized in Table I.

TABLE I. PERFORMANCE SUMMARY

Parameters	Values
Technology (CMOS)	**28 nm FDSOI**
Supply voltage	**0.7 V**
Area	**0.00135mm^2**
Hysteresis voltage range	**$\pm$ 1 mV - 15.3 mV**
Loop delay tuning range	**14.4 ns - 5.1 us**
Center frequency range	**100 kHz - 6 MHz**
Current consumption range	**52.5 nA - 6.3 uA**
Power consumption range	**36.8 nW - 4.4 uW**

IV. CONCLUSION

In this paper, we presented a configurable hysteresis comparator for asynchronous sigma-delta modulators. The proposed comparator provides coarse and fine tuning of the ASDM loop delay and center frequency which are important design parameters. Post-layout simulation of the configurable hysteresis comparator shows that the comparator is able to provide hysteresis voltage range of $\pm$(1 to 15.3) mV while consuming 36.8 nW to 4.4 μW of power from 0.7 V supply. In addition, the comparator enables ASDM loop delay tuning range of 14.4 ns to 5.1 μs and center frequency tuning range of 100 kHz to 6 MHz. Although the comparator is optimized for ASDMs, the proposed circuit can also be used in applications where there is a need to configure the hysteresis voltage and propagation delay of the comparator. The achieved flexibility in the proposed comparator design provides a simple, compact and power-efficient solution for implementing decision making circuits in analog-to-digital converters.

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