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# Common Mode Noise Analysis for a High Step-Up Converter with GaN Devices

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**Abstract**— High Step-up converters have numerous applications in renewable energy systems and electric automotive industry. To improve the power density, an interleaved high step-up boost converter with coupled inductor was proposed. However, for practical applications it is compulsory that this topology must comply with the CISPR standards. Therefore, to identify the noise sources in the analyzed converter, an equivalent noise modelling is conducted. These models revealed the dependency of inductor windings on different noise sources. For experimental analysis of the conducted emissions of this topology, GaN FETs based prototype is designed. Several tests were carried out to find the effect of various factors on noise emission. As results of tests, 1) Increasing the switching frequency generates increase in the noise spikes 2) Noise emissions from the converter do depend on its mode of operation 3) High peaks of noise are generated at low frequency range by reducing the voltage transition time across the switch.

**Keywords**—EMI Noise, High Step-Up, DC-DC Converter, Coupled-Inductor, CM Noise, GaN FETs.

## I. INTRODUCTION

Various applications including Uninterruptable power supplies (UPS), electrically propelled vehicles (EV), renewable energy systems etc. require power converters to boost the voltage level [1], [2]. Conventional boost converters are not efficient for the applications where voltage gain of five or higher is required [3]. Applications that require high voltage gain employ high step-up (HSU) converters [4]. Authors of [5] reviewed various topologies of such converters. However, most of the topologies suffer from low power density. Reference [6] introduced an interleaved HSU converter topology with high voltage gain and power density.

One way to increase the power density of power converter in [6] is by size reduction of magnetic components and cooling systems. At high switching frequencies, required size of the magnetic components is reduced. This can be achieved by replacing silicon switches by Gallium-Nitride (GaN) FET. GaN FETs can be switched at high frequencies as they have low junction capacitance as compared to silicon switches [7] [8]. These switches also have low ON resistance that reduces the heating losses and hence the size of cooling requirements is reduced [9].

However, large  $dv/dt$  and  $di/dt$  in GaN-FET based converters act as primary sources for conducted and radiated electromagnetic interference (EMI) [10], [11]. In such converters, parasitic capacitances in the circuit layout become critical at fast switching transitions (typically 5-20 ns) [12]. This capacitance provides a path to conduct common mode

(CM) noise from the power stage to the ground. In industrial environment, conducted emissions from converters can result in EM interference with surrounding devices [13]. For compliance with various international EMI standards, it is very critical to suppress the emissions below the standard limits [14]. Therefore, study of EMI emissions and suppression of HSU converters is quite relevant.

To design an effective EMI filter, it is important to identify the noise sources in the circuit topology. Researchers have conducted various studies to develop common mode noise models of different converter topologies. A recent publication [12] discusses the conducted emissions of WBG based motor drives. Various publications [10], [13], [15], [16] discuss conducted noise models for different DC-DC converter topologies. The fact that these publications address different topologies signifies the importance of identifying noise sources in novel topologies as well.

Circuit topology of novel interleaved HSU converter proposed in [6] is shown in Fig. 1.

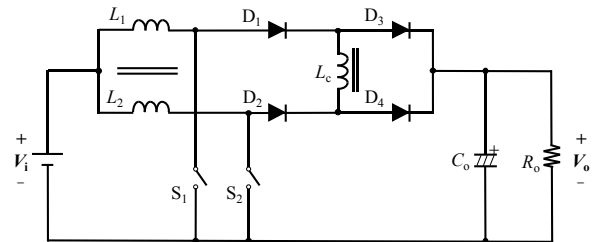


Fig. 1. HSU Converter Topology.

This topology requires three coupled windings that introduces parasitic inter-winding capacitance. In addition to the two external windings, as in conventional two phase interleaved boost converter, a third central winding  $L_c$  is required to achieve high gain. Presence of this central winding also introduces additional parasitic capacitances into the circuit. Winding configuration of the coupled inductor is shown in Fig. 2.

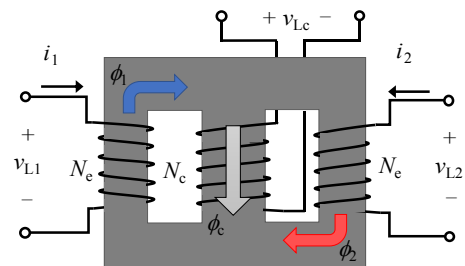


Fig. 2. Winding Configuration of the analyzed HSU Converter.

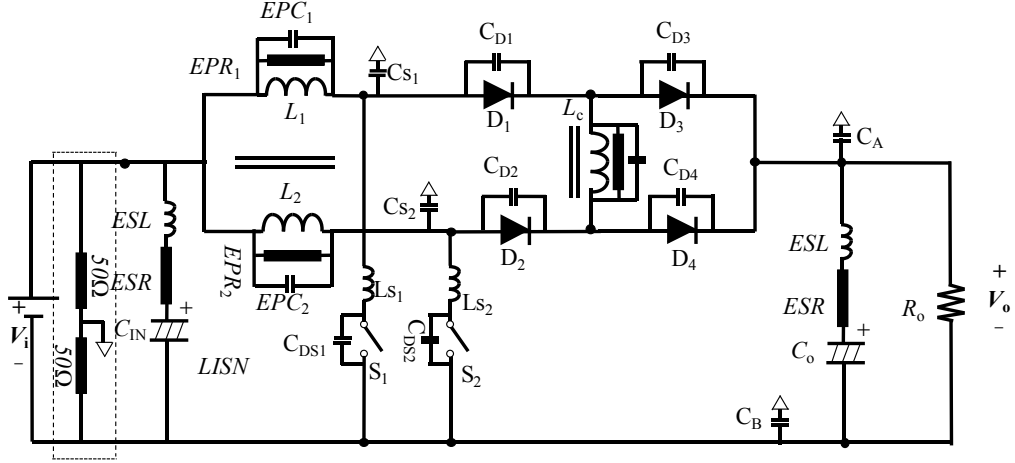


Fig. 3. Parasitic Elements in HSU Converter.

This paper presents the CM noise model of a HSU converter topology. GaN based practical prototype is built to operate the converter at high switching frequencies. Conducted emissions of the converter are recorded at different switching frequencies. Converter is operated in three different modes of operation to study the noise emissions. Gate driving circuit is modified to study the effect of different switching turn ON times on noise emissions.

This paper is organized as follows Section II describes different modes of operation and noise sources in the converter. Section III includes the equivalent noise model of the circuit. Experimental results are presented in section IV. Conclusions are drawn in section V.

## II. HSU CONVERTER ANALYSIS

This section discusses the parasitic elements and different modes of operation of the analyzed converter.

### A. Parasitic Elements in the HSU Converter

Fig. 3 shows the converter topology with high frequency parasitic elements. These parasitics are also responsible for the ringing in drain-source voltages of the MOSFET that also generates high frequency common mode noise [17]. In Fig. 3 EPR and EPC stands for equivalent parallel resistance and equivalent parallel capacitance of each inductor, respectively. Junction capacitance of the diodes is shown as CD, whereas CDs shows the drain-source capacitance of the switches. CS1 and CS2, in Fig. 3, represent the parasitic capacitance from the switching nodes to the ground. At high switching frequencies and especially for WBG devices where voltage transition times are very fast, parasitic capacitance from the switching nodes become very critical. Therefore, careful design of layout can minimize this capacitance.

Moreover, inter-winding parasitic capacitances of the inductor are shown in Fig. 4.  $L_1$  and  $L_2$  represents the mutually coupled external windings, whereas  $L_c$  is the central winding coupled with both external windings.

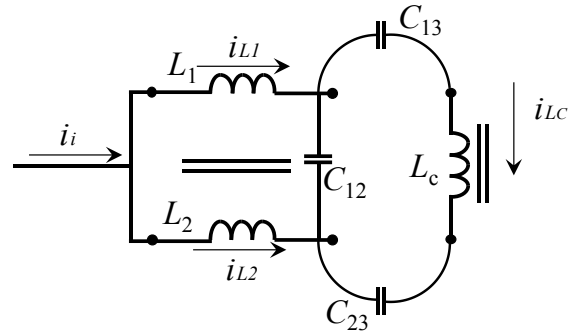


Fig. 4. Inter-winding Capacitances.

### B. Modes of operation

This converter can operate in four different modes of operation depending on the duty ratio of switches [18]. Current waveforms for all modes of operation are presented in Fig. 5.

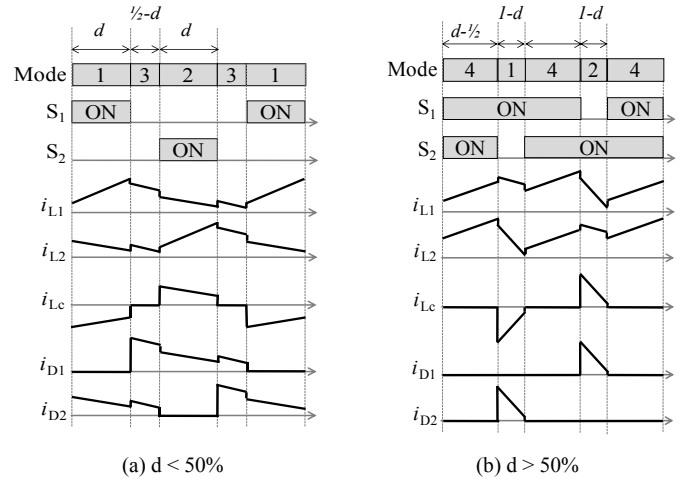


Fig. 5. Duty Cycle cases.

Fig. 5(a) presents the waveforms when duty ratio is less than 50% while Fig. 5(b) is for the cases when duty cycle is greater than 50%. Circuit diagrams for all modes of operation are given in Fig. 6.

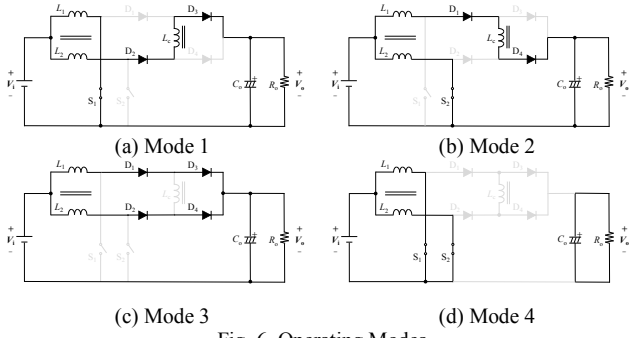


Fig. 6. Operating Modes.

During Mode 1, switch  $S_1$  is switched ON and  $S_2$  is switched OFF. As the voltage,  $V_{DS}$  across the switch  $S_1$  collapses, capacitance  $C_{DS1}$  and  $C_{S1}$  are discharged while  $C_{DS2}$  and  $C_{S2}$  are charged. Similarly, during mode 2,  $C_{DS1}$  and  $C_{S1}$  are charged while  $C_{DS2}$  and  $C_{S2}$  are discharged. Following the same principle, parasitic capacitances and switch capacitances are charged and discharged at different switching transitions. Comprehensive steady state analysis of all modes of operation and voltage gain of the converter is given in [6].

### III. COMMON MODE NOISE MODEL

Common mode chokes usually reduce the conducted common mode emissions in power converters. However, these chokes increase the weight of the converter and introduce additional losses. Impedance balancing of power and neutral line can provide satisfactory noise cancellation results without application of any additional chokes [10]. However, it is critical to develop an equivalent noise model of the converter for impedance balancing.

Fig. 7(a) presents the equivalent noise model of the HSU converter. Switches  $S_1$  and  $S_2$  are categorized as the major noise sources in the circuit. In order to develop an equivalent noise model, it is possible to replace the switches with voltage sources. These voltage sources have the same voltage waveform as  $V_{DS}$  of the switches. Input capacitor  $C_{IN}$  and output capacitor  $C_{OUT}$  are also replaced with voltage sources. Moreover, parasitic series inductance and resistance of these capacitors will generate high frequency voltage ripples. This voltage ripples will also act as noise sources. Reverse recovery current and charge stored across the parasitic capacitance of the diodes will generate high frequency current ripples as well. These diodes with all their parasitic components can be replaced by an equivalent current source [10], [15]. This current source has the same waveform as the current through each diode.

Various noise sources, shown in Fig. 7(a), contribute collectively in the emissions of the converter. However, it is difficult to analyze the circuit collectively with all the sources. In order to simplify the analysis, it can be assumed that all these sources are decoupled and hence they can be analyzed individually without affecting the performance of the circuit. By principle of superposition, it is possible to analyze the circuit for each individual noise source [10], [15], [16], [19], [20].

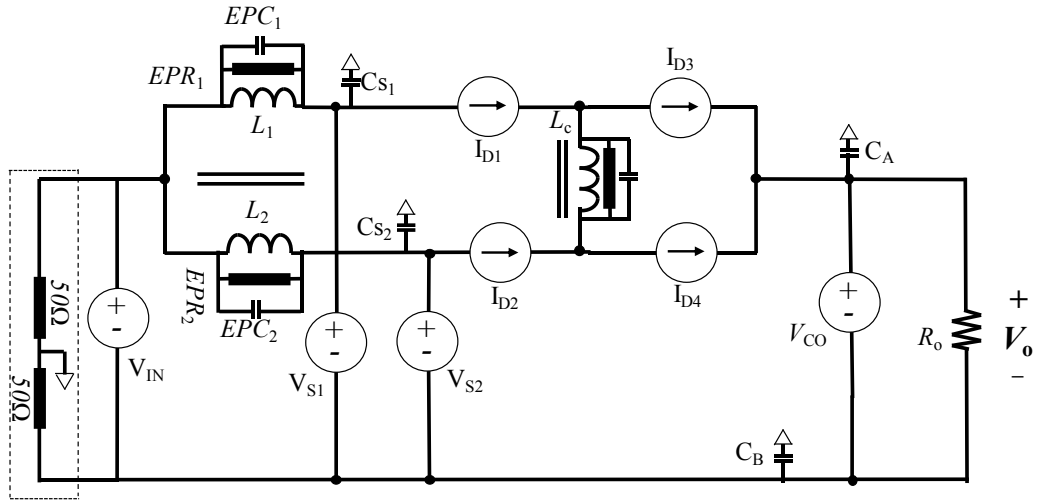
Fig. 7(b) shows the equivalent circuit for noise source  $V_{IN}$ . This voltage source represents the input capacitor and all branch parasitics. Because of the high impedance of the current sources, they can be replaced with an open circuit and all remaining voltage sources are replaced with a short circuit to analyze the effect of  $V_{IN}$ . Then, voltage at switching nodes

are maintained by the sources  $V_{S1}$  and  $V_{S2}$ , while the voltage at the output capacitor is also fixed by the source  $V_{CO}$ . Hence, the central winding  $L_C$  will not affect the noise generated because of this source. Switching capacitances  $C_{S1}$ ,  $C_{S2}$  and line capacitance  $C_A$ ,  $C_B$  will provide a path to high frequency common mode current component to follow into the ground and back through the LISN resistance.

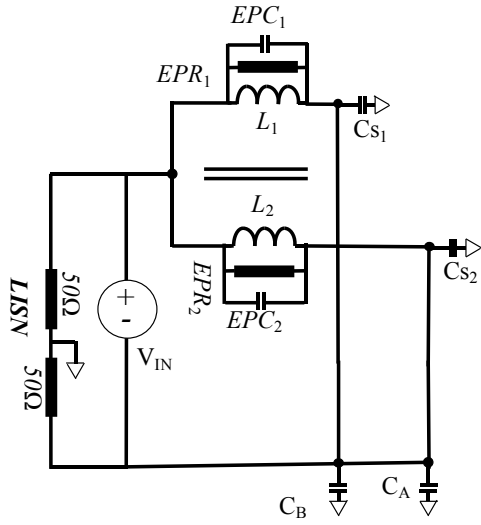
Voltage across the switch changes with switching frequency. Every time the switch is switched ON, drain to source capacitance of the switch along with parasitic capacitance from switching node to ground is discharged. This capacitance provides a path to common mode current. However, an important aspect is the rate at which the voltage is changed across the switch. This depends on the structure of the switch. As previously mentioned GaN FETs have low junction capacitance as compared to the Si FETs, hence the voltage across the GaN switch will drop to zero at a faster rate than in silicon switches. As the current through the capacitance is directly proportional to the rate of change of voltage across it, a faster turn-on time will generate more leakage current. Similarly, when the switch is turned off, drain to source capacitances of the switch and parasitic capacitances are charged. Low junction capacitances of GaN FETs also ensure fast switching of the switch and affect the leakage current through the parasitic capacitance. Hence, it is important to pay extra attention to the layout design to minimize the parasitic capacitances [21].

Fig. 7(c) and 7(d) show the equivalent noise model for switching devices  $S_1$  and  $S_2$  respectively. This voltage source includes all the parasitics of the branch. The rate of change of voltage  $dv/dt$  is the highest on both switching nodes and hence these sources serve as major noise sources in the converter. After substitution using the superposition principle, it can be seen that the central winding  $L_C$  does not affect the noise from switching devices. Fig. 7(c) shows the equivalent model for voltage source  $V_{CO}$ . This voltage source represents the noise signal generated from the output capacitor and its branch parasitics.

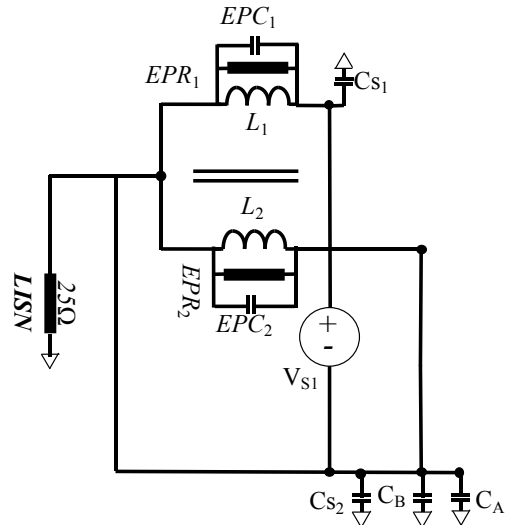
This analysis provides a base to design circuit modifications in order to reduce the conducted emissions. By the concept of impedance balancing, if the impedance of positive and negative lines is balanced, theoretically no common mode current will flow through the converter. This is usually achieved by designing an inductor for the current return path that is coupled with the boost inductor in the positive path. Authors of [16] and [17] have discussed impedance balancing for interleaved boost and conventional boost converter respectively. However, both windings of the boost inductor in the converter discussed by [16] are not coupled. Nevertheless, it is critical for the operation of HSU converter that all three windings of boost converter should be coupled with each other. It is a challenge to design an inductor with three windings for return path in order to reduce the common mode conducted emissions and it will be addressed in future studies.



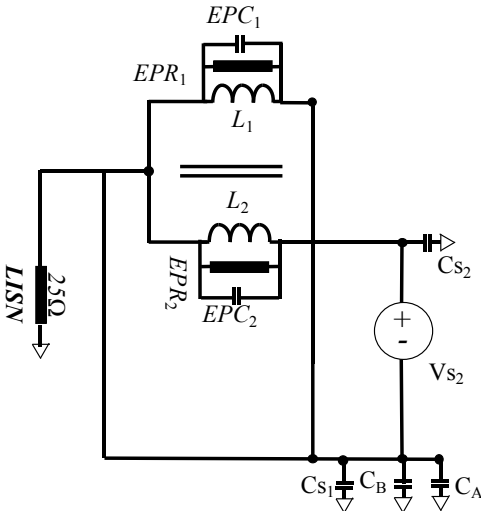
(a) Noise Sources in HSU Converter



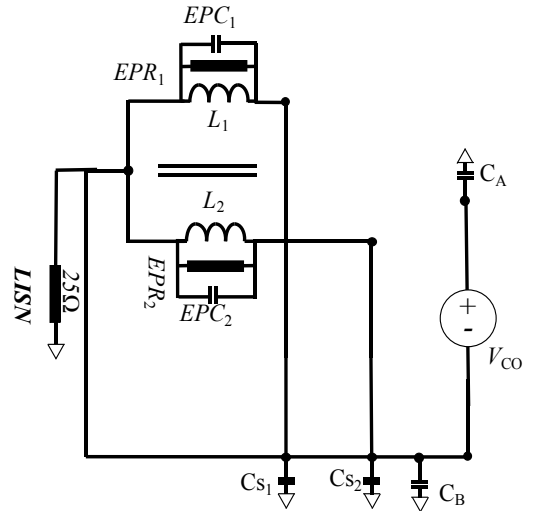
(b) Equivalent Noise Model for  $V_{IN}$



(c) Equivalent Noise Model for  $V_{S1}$



(d) Equivalent Noise Model for  $V_{S2}$



(e) Equivalent Noise Model for  $V_{CO}$

Fig. 7. Equivalent Common Mode Noise Models of HSU Converter.

#### IV. EXPERIMENTAL ANALYSIS

To perform experimental validation of the analysis presented above, GaN based prototype of the HSU converter was built. Table I shows the parameters of the experimental setup.

TABLE I PARAMETERS OF PROTOTYPE

Parameter	Value
Input Voltage $V_{IN}$	20-50 VDC
Output Voltage $V_{OUT}$	100 VDC
Output Current	1 A
Switching Frequency	100-500 kHz
Duty Ratio $D$	0.3 – 0.7
Switching Device	TPH3206
Inductor Core Material	Ferrite PC40
External Winding Inductance $L_1=L_2$	720 $\mu$ H
Central Winding Inductance $L_C$	3mH

In order to minimize the parasitics, a double layer printed circuit board is designed. Fig. 8 shows the practical prototype of the HSU converter.

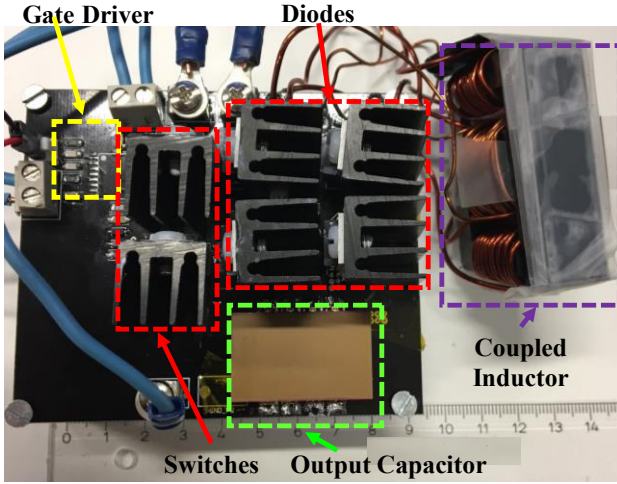


Fig. 8. HSU Prototype.

The test setup to measure the conducted emissions of the converter is shown in Fig. 9. In this setup, the equipment under test (EUT) is the HSU converter and it is being fed with DC power through a LISN. The LISN used in measuring the setup is 50 $\Omega$ /50 $\mu$ H. The purpose of this LISN is to provide repeatability in the measurements. The EUT acts as a noise source in the setup and a spectrum analyzer is connected across the 50 $\Omega$  resistor in LISN. Noise emissions from the

converter depend on numerous factors. Hence, to analyze the emissions of this HSU converter, various tests have been carried out under various operating conditions.

As discussed earlier, switching frequency is critical to increase the power density. GaN devices make it possible to switch them at high frequencies. To study the conducted emissions from the HSU converter, tests were carried out at three different switching frequencies (100kHz, 300kHz, 500kHz). Fig. 10 shows the results of those tests. To study the effect of switching frequency on noise emission, all other circuit parameters were kept same.

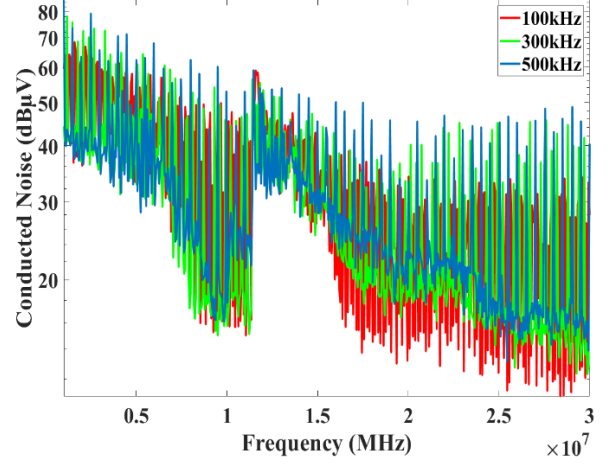


Fig. 10. Experimental Result (Switching Frequency).

To comply with CISPR standards, emissions should be under specified limit for the frequency range of 0.15MHz – 30MHz. Hence, results are shown for this frequency limit. Fig. 10 shows high noise peaks in high frequency range. In the range of 10MHz – 30MHz, a difference of almost 20dB $\mu$ V exists between the noise peaks at 100kHz and 500 kHz.

This HSU converter can operate in three different operating modes. In previous section of this paper, it has been discussed that windings of the inductor behave differently in each operating mode. Hence, it is important to analyze the noise emissions in all operating modes. Tests were carried out at duty ratios of 30%, 50% and 70%. These three duty ratios cover all operating modes of the converter. Fig. 11 shows the results of the tests.



Fig. 9. Test Setup.

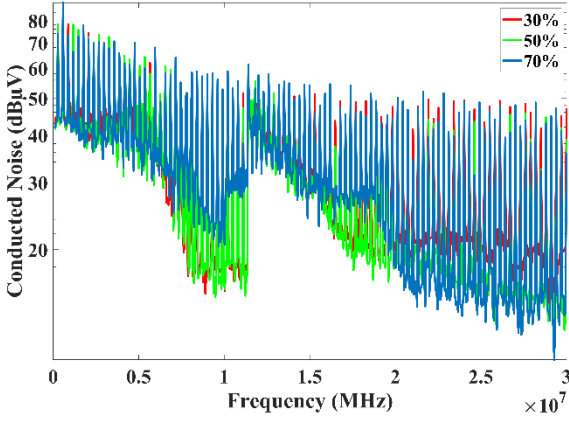


Fig. 11. Experimental Result (Operating Modes).

All the tests were performed at switching frequency of 300 kHz with output voltage of 100 VDC. It can be seen that noise difference of almost 40 dBμV exists between modes of operation around frequency range of 5MHz-10MHz.

One important feature of GaN switches is their ability to turn-on and turn-off at extremely fast speed. To study the behavior of the converter at different switching transition times, conducted emissions are recorded for switch turn-on times of 11.2ns and 14ns. Fig. 12 shows the results of the tests.

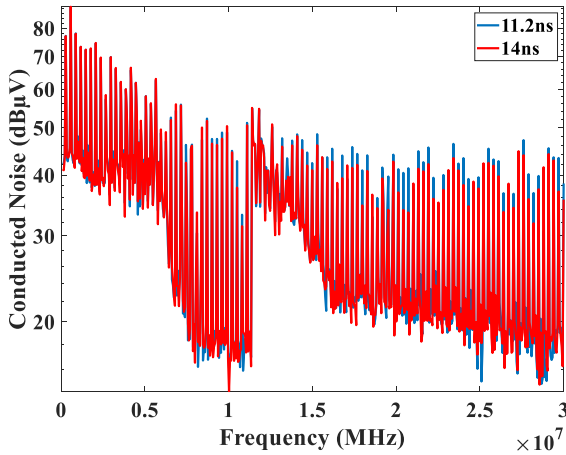


Fig. 12. Experimental Result (Turn-On Times).

Results show high noise peaks in low frequency range for turn-on time of 14ns. Gate resistance was reduced to reduce the switching time. For turn on time of 11.2ns, noise is reduced in low frequency range, however for high frequency range of 10-30 MHz, difference of almost 5dBμV is observed.

During the experimental analysis, collapsing of drain to source voltage is observed. Fig. 13 shows these phenomena. It has been observed that voltage across the switch collapses and oscillates at high frequency, even though gate-source voltage of the switch was in negative region (to avoid false turn-on of the switches, negative  $V_{GS}$  is used). This topology has been proposed recently and requires more detailed analysis to find the cause of this phenomena. It is important to mitigate this as high frequency oscillation in  $V_{DS}$  will generate high leakage current.

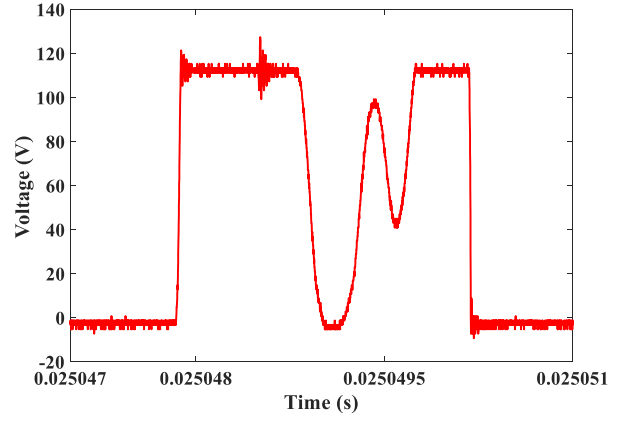


Fig. 13. VDS Collapse.

## V. CONCLUSION

In this paper, detailed analysis on conducted emissions of a HSU converter is made. Theoretical background of the topology and its operating principle has been presented. To identify the different noise sources in the converter, equivalent common mode noise model has been developed. Analysis of the noise model showed that the central winding of the inductor does not impact the noise emissions from switches. Moreover, experimental analyses were carried out with GaN based switches as a validation of the CM modeling presented. Experimental results showed that emissions from the converter does depend on the switching frequency, modes of operation, and voltage transition time across the switch.

Design of the inductor for impedance balancing to mitigate the noise emissions will be presented as future work. Voltage collapse phenomena and its detailed impact on noise will also be addressed in future studies.

## VI. ACKNOWLEDGMENTS

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