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A Systematic Design Method for Direct Delta-Sigma Receivers

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Abstract—Next generation receivers, such as the direct $\Delta\Sigma$ receiver (DDSR), shift the boundary between analog and digital closer to the antenna by merging the functionalities of different sub-blocks. In the DDSR, the analog components are used to their maximum potential as each stage participates in amplification, blocker filtering, anti-aliasing, and quantization noise shaping simultaneously, resulting in a compact design. To overcome the increased design complexity, the implemented DDSRs rely on common practices in receiver and $\Delta\Sigma$ modulator design. In this paper, we will show that the common design practices for neither receivers nor $\Delta\Sigma$ modulators yield optimal performance for the DDSR, and propose a systematic design method for g_mC based DDSRs. The method enables improved performance and straightforward design flow by combining the gain partitioning, noise considerations and loop-filter design. The developed method is demonstrated by designing a g_mC based DDSR using a 28 nm FDSOI CMOS process. Simulations of the DDSR indicate state-of-the-art performance.

I. INTRODUCTION

THE software defined radio concept has been the driving force of hardware digitalization in both receivers (RX) and transmitters (TX). Digital circuits have been replacing analog circuits due to their scalability and insensitivity to processing variations. Ultimately, the goal is that the TX and the RX will be entirely digital with the exception of the analog-to-digital converter (ADC) and digital to analog converter (DAC), which act as the translators between the analog and digital domains. Such converters can be referred to as direct RF-to-digital converters or direct digital-to-RF converters, respectively. The trend of moving the boundary between analog and digital closer to the antenna by combining functionalities of the receiver and ADC is evident in recent publications featuring RF band-pass [1]–[5] and downconverting low-pass [6]–[9] $\Delta\Sigma$ ADCs.

The direct $\Delta\Sigma$ receiver (DDSR) concept, originally introduced in [6], has been an important step towards direct RF-to-digital converters, combining the functionalities of a direct conversion receiver and a continuous-time (CT) $\Delta\Sigma$ ADC. The RF stages and the baseband (BB) channel select filter are incorporated into the $\Delta\Sigma$ loop-filter. As a consequence, the loop-filter contains one or more hybrid RF/BB stages, in

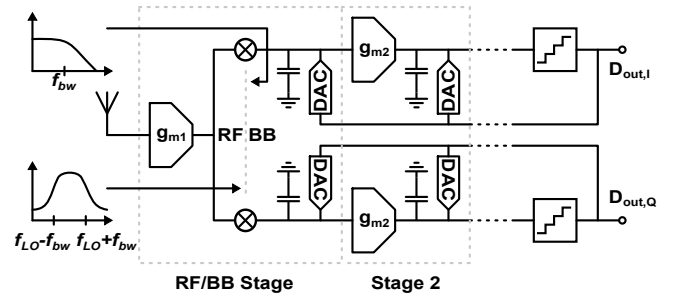


Figure 1. A g_mC based DDSR.

which a mixer translates the frequencies between RF and BB. When inspected in the vicinity of DC or the local oscillator (LO) frequency, a low-pass impedance profile is seen on the BB side of the mixer, while a band-pass response is observed on the RF side of the mixer, as illustrated in Fig. 1. As an advantage of the DDSR, the analog components are used to their maximum potential as each stage participates in amplification, blocker filtering, anti-aliasing, and quantization noise shaping simultaneously, resulting in a compact design. In addition, the digital feedback enables the use of advanced blocker cancellation techniques [10].

Since its introduction, the DDSR has received an increasing amount of research interest [11]–[14]. The research has concentrated on the modeling of the N-path filter, a key part of the DDSR. However, the overall performance of the measured DDSRs is not yet up to par with traditional $\Delta\Sigma$ implementations. For example, the maximum signal-to-noise and distortion ratio (SNDR) in a DDSR is limited by the gain that is applied in the loop-filter. While lower gain can be beneficial, a unity gain implementation that is common in traditional $\Delta\Sigma$ designs [15] is not feasible as the receiver sensitivity is endangered. The total amount of applied gain and the gain partitioning in the DDSRs and similar implementations have been based on common practices in either receiver [12] or $\Delta\Sigma$ modulator [7] design. However, as we have argued in the limited case of low noise amplifier design for DDSRs [16], such practices may not result in optimal performance.

In this paper, we will demonstrate that the common system design practices for neither receivers nor $\Delta\Sigma$ modulators yield optimal performance for the DDSR, and propose a systematic design method for g_mC -based DDSRs. The method improves

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performance and creates a straightforward design flow by combining the gain partitioning, noise considerations and loop-filter design. By analytical means, we are able to

- Obtain improved maximum SNDR and blocker resilience
- Simplify the loop-filter design process by utilizing the CT domain and coefficient pre-distortion
- Obtain scaled loop-filter coefficients without the need for iterative processes
- Define the gain and noise specifications of each stage
- Use a variable sampling frequency to avoid quantization noise folding

In order to thoroughly showcase the design method, we will use the attained knowledge to design a g_mC based DDSR using a 28 nm CMOS FDSOI process. Steady-state AC and noise transient simulations of the designed DDSR indicate state-of-the-art performance.

The paper is organized as follows. Section II introduces the design targets and illustrates alternative design approaches. One of the design approaches is selected and used in the system design of the DDSR. Section III continues with loop-filter and component design, containing all the necessary design equations. Analytical and behavioral simulations are used to verify the design so far. The circuit implementation considerations and transistor-level simulations are presented in Section IV, followed by conclusions in Section V.

II. SYSTEMATIC DESIGN OF A DDSR

There are many aspects that need to be considered when designing a DDSR. In order to keep focus on the key points, we will start with an overly simplistic view of the DDSR and then add complexity when necessary. In this section we will first introduce the design targets and then design the first two stages of the DDSR by using a gain/pole model. Using this approach we can design the gain partitioning and approximate pole positions for the loop filter based on target requirements. As there are several possibilities that can meet the design targets, we will introduce three main design alternatives and select one of them, which is then used as a basis of the implementation. Once the gains and approximate location of the first two poles have been determined, we can use the information obtained to find the total number of stages and then finalize the gain partitioning and pole positioning.

A. Design objectives

The design objectives for the DDSR can be specified using parameters listed in Table I. The design parameter values vary depending on the communication standard that the DDSR is being designed for. While the parameter values listed are not directly linked to any specific standard, they provide an insight on what is typically required. In total there are seven parameters that will be used to set up the optimization boundaries for the design. The receiver noise figure NF_{RX} fixes the bottom boundary, determining the weakest in-band input signal which can be detected. The top boundary, i.e., the strongest input signal that the receiver can handle without saturation, is defined

by the maximum in-band signal power $P_{in,max}$, the maximum power of the most demanding blocker $P_{blocker,max}$, and P_{max} , the maximum power that the internal nodes of the DDSR are able to handle. Stronger input signals can be tolerated out-of-band due to filtering, and thus the BB bandwidth f_{bw} and the offset frequency of the most challenging blocker $f_{blocker,max}$ are necessary in order to define the spectral mask. These design objectives should be met across the receiver bandwidth f_{RX} .

Table I. DDSR DESIGN OBJECTIVES.

	Value
Noise figure (NF_{RX}) [dB]	<5
Carrier frequency (f_{RX}) [MHz]	700 to 2800
BB bandwidth (f_{bw}) [MHz]	10
Blocker offset frequency ($f_{blocker,max}$) [MHz]	100
Blocker power to 50Ω ($P_{blocker,max}$) [dBm]	-15
Maximum in-band power to 50Ω ($P_{in,max}$) [dBm]	-30
Maximum internal node power to 50Ω (P_{max}) [dBm]	-20

The first six design parameters are commonly used in the design of any receiver, but P_{max} requires a brief explanation. As the receiver specifications are defined in power, we will normalize the internal node voltages to equivalent power referred to the 50Ω source impedance. A power limit, after which non-linear components begin to degrade the sensitivity of the receiver, can then be defined for each internal node. The linear operation range of the internal voltage nodes of the DDSR is limited by the input and output transistors of the amplifiers. In order to avoid excessive non-linearity, MOS transistor should be operated well within saturation limits. The amplitude of the AC signal at the gate should not exceed $V_{eff} = V_{GS} - V_t$, while the amplitude of the AC signal at the drain should be below the saturation margin $V_{satmarg} = V_{DS} - V_{eff}$. Of these limits, V_{eff} is more demanding, as distortion components begin to arise above the thermal noise floor far before V_{eff} limit is reached. The main limitation for the linearity is therefore the change in the gate voltage, which is reflected to a change in transistor transconductance. In order to maximize the linearity we can minimize the voltage swing at the gate with feedback, or linearize the g_m by using push-pull circuit topologies or source degeneration.

In a g_mC implementation, the transistor gates are driven by the internal voltage nodes. The voltage swings should be limited to V_{eff} with added margin. In modern processes, the low supply voltages limit the maximum V_{eff} to between 100 mV and 200 mV. For simplicity, we have used only one voltage limit for all internal nodes. The selected limit is based on the effective gate voltage $V_{eff} \approx 150$ mV, which is achievable in a 28 nm FDSOI CMOS process. According to simulations, the power level of $P_{max} = -20$ dBm, equal to 32 mV in a 50Ω system, still keeps the third order harmonic component below the integrated thermal noise ($-174 + 70 + 5 = -99$ dBm), when push-pull circuit topologies with unity gain loading are used.

B. Design approaches

The maximum internal node power P_{max} and the maximum power of the dominant blocker $P_{blocker,max}$ are important when

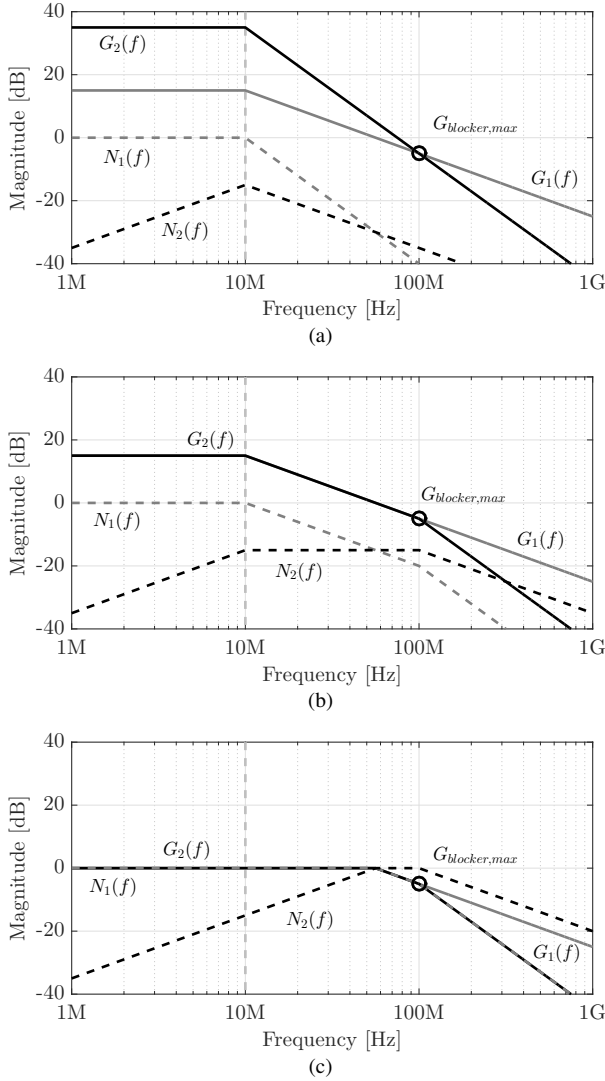


Figure 2. Different gain partition and filtering configurations for the DDSR: (a) maximum gain, (b) gain only in the first stage, (c) unity gain. The gains from input to the first stage and second stage outputs are marked with $G_1(f)$ and $G_2(f)$, respectively. The functions $N_1(f)$ and $N_2(f)$ define how the input noise sources of the corresponding stages are seen at the output of the receiver in relation to the input.

designing the gain partitioning and signal filtering responses for the DDSR. The gain is needed to maintain sufficient SNDR even for weak input signals in the presence of circuit noise and other non-idealities, while filtering is required to avoid applying gain to the out-of-band blockers. In the worst case, the non-linear mixing products of the blocker and the inherently high out-of-band quantization noise can fold to in-band frequencies, desensitizing the receiver. In order to receive even the weakest input signal, the receiver must be able to withstand the maximum blocker power with the maximum receiver gain. From this, we can calculate the maximum gain at the blocker frequency to be

$$G_{\text{blocker,max}} = P_{\text{max}} - P_{\text{blocker,max}}, \quad (1)$$

which gives $G_{\text{blocker,max}} = -5$ dB in this case.

In Fig. 2 the $G_{\text{blocker,max}}$ limitation is utilized to find three different design alternatives for the DDSR. The first design alternative resembles what could be the case when common practices in the receiver design are used, while the third alternative follows common practices in $\Delta\Sigma$ design. In these design alternatives, we concentrate on the first and second stage of the receiver, since these dominate the overall performance. In each case, the gains from the input to the first stage and second stage outputs are marked with $G_1(f)$ and $G_2(f)$, respectively. The functions $N_1(f)$ and $N_2(f)$ define how the input noise sources of the corresponding stages are seen at the output of the receiver in relation to the input, while the blocker gain is marked with a circle. For each case, we can obtain the receiver gain G_{RX} based on the pole placement and blocker gain limitation, and calculate the maximum SNDR

$$\text{SNDR}_{\text{max}} = P_{\text{max}} - G_{\text{RX}} - (10 \log_{10}(1000 k_B T f_{\text{bw}}) + N_{\text{FRX}}), \quad (2)$$

where the thermal noise is considered in dBm for convenience, k_B is the Boltzmann constant and T is the temperature in Kelvins ($T = 300$ K is used throughout this paper). The required maximum SNDR is relatively modest in a typical receiver, as it should only meet the (usually relatively low) SNDR requirement of the used modulation.

The first design alternative, shown in Fig. 2(a), applies the maximum gain allowed by the $G_{\text{blocker,max}}$ limitation in both stages. As each stage has a first order behavior, maximum in-band gain is obtained when both poles are at $f_{\text{bw}} = 10$ MHz. The in-band gains from the input of the receiver to the output of the first and the second stage, $G_1(f)$ and $G_2(f)$, are limited to 15 dB and 35 dB due to the required blocker attenuation. As $N_1(f)$ suggests, any in-band noise at the input of the first stage will appear at the output of the receiver unattenuated, and will ultimately be the limiting factor for the noise performance of the receiver. The noise sources at the input of the second stage will contribute at the receiver output attenuated by the gain in the first stage, as per Friis' equation. In addition, because of the feedback, $N_2(f)$ behaves as a single-pole high-pass function at the in-band, shaping the device noise of the succeeding components. Note that the noise shaping effect does not apply to the noise of the feedback device itself, which is only affected by the gain of the first stage. If no further gain is applied in the receiver, the maximum in-band input power we can receive without significant distortion components is $P_{\text{max}} - G_{\text{RX}} = -55$ dBm. Thus, gain control of $P_{\text{in,max}} - (P_{\text{max}} - G_{\text{RX}}) = 25$ dB is necessary to fulfil the specifications. The maximum SNDR we can achieve with the maximum gain can be calculated from (2) and is 43.8 dB.

The second design alternative is shown in Fig. 2(b). In this case, gain is only applied in the first stage. In theory, as no gain is applied in the second stage, we can move the second pole freely without increasing the blocker gain. To maximize the in-band attenuation of different noise sources after the second stage, it is beneficial to position the pole to as high frequency as possible. The limiting factor will be the sampling frequency f_s . The higher the pole frequency, the higher the f_s required to maintain stability. In our experience, the minimum stable $f_s \approx 4f_{\text{ns}}$, depending on the loop-filter order and feedback

loop delay. To balance between noise shaping and minimum f_s requirement, we select 100 MHz as the initial pole frequency. The total gain in the receiver is now the gain of the first stage, $G_{RX} = 15$ dB. This leads to maximum in-band input power $P_{max} - G_{RX} = -35$ dBm, which means that gain control of 5 dB is required. The maximum SNDR has been increased by the amount that the gain has been reduced, and is thus 63.8 dB.

The third design alternative, shown in Fig. 2(c), resembles more the typical $\Delta\Sigma$ unity-gain implementations. The first pole position is set so that the attenuation at the blocker frequency is the required 5 dB. Again, the position of the second pole can be selected freely, within the limits set by the stability requirements. Since no gain is applied in either of the stages, we are relying purely on noise shaping rather than gain to reduce the contribution of noise sources at the input of the stages. The in-band noise responses remain identical to previous two alternatives. Noise sources at the input of the receiver will appear at the output as they are, while the noise sources of the second stage will be attenuated by the noise shaping of the first stage. The gain of the receiver is now $G_{RX} = 0$ dB and thus the maximum SNDR is ideally 78.8 dB. However, the receiver now has two major noise contributors, the input device and the first feedback device, rendering it difficult to reach the sub-5 dB noise figure target, and subsequently, the maximum SNDR.

Based on the analysis presented above, we have chosen the second alternative. The first alternative would also be a valid choice, but since it relies on gain rather than noise shaping to relax the noise requirements of the later stages, a wider gain control range would be required. Furthermore, the gain applied for the potential near-band blockers is higher in the first alternative.

C. Finalizing system design

After determining the gain/pole configuration of the first two stages, we can proceed with DDSR system design. The quantizer resolution and the total order of the DDSR need to be selected such that only a minor part of the in-band noise is due to the quantization noise. In order to maintain a solid presentation flow, we will consider the quantizer resolution separately and then calculate the required DDSR order based on the selected resolution.

A low-resolution quantizer is ideal for high-frequency designs due to the low complexity and small circuit area. However, as we move towards a single-bit quantizer, the non-idealities of the sampling clock become more significant factors in the overall performance. Multi-bit quantization or FIR feedback DACs [17] offer increased jitter resilience, which is especially important here in order not to degrade the receiver sensitivity. For this design we have selected a 3-bit quantizer, as it is still relatively simple to implement even at higher sampling frequencies. The input voltage range of the quantizer should be selected so that it will not limit the maximum input signal level, which means minimum single-ended full-scale of $P_{max} = -20$ dBm, or 32 mV is necessary. We have chosen a single-ended full-scale peak-to-peak amplitude of

$V_{FS} = 100$ mV to ensure that it will not be the limiting factor in the overall performance. Thus, the quantization step is $\Delta = V_{FS} / (2^B - 1) = 14.3$ mV, where B is the number of bits.

Next, the order of the DDSR has to be selected. As a simplification, we have divided the loop filter poles into two groups, ¹) filtering poles and ²) noise shaping poles. The filtering poles are mainly used for attenuating the blockers, and have only minor noise shaping benefits due to their position near f_{bw} . The noise shaping poles are located at a much higher frequency f_{ns} , and thus they are primarily responsible for the noise shaping. In the selected design alternative, there is only one filtering pole, which is located at f_{bw} . The second pole at $f_{ns} = 100$ MHz does not provide sufficient quantization noise shaping, and thus extra noise shaping poles will be added.

If we separate the quantization noise from the other noise sources, we can calculate the required number of noise shaping poles N by matching the output noise densities at f_{bw}

$$N = \frac{\log_n \left(\frac{\Delta^2}{6f_s k_B T G_{RX} F_{DEV}} \right)}{2 \log_n \left(\frac{f_{ns}}{f_{bw}} \right)}, \quad (3)$$

where G_{RX} is the receiver power gain, and F_{DEV} is the noise factor of the receiver excluding the quantization noise [13]. In order to avoid quantization noise folding in the mixer [6], we tie the f_s to the LO frequency f_{LO} , so that the f_s and f_{LO} vary from 0.7 GHz to 2.8 GHz. Nominal $f_s = 1.4$ GHz is used in the calculations. If we reserve 4 dB of the total noise figure to other noise sources than the quantization noise, i.e. $F_{DEV} = 2.5$, we can calculate the required number of noise shaping poles to be $N = 2.44$. This suggests that we can either use three noise shaping poles at lower f_{ns} , or alternatively, two noise shaping poles at higher f_{ns} . We choose the latter alternative to minimize the number of stages. From (3) we can solve the required noise shaping pole frequency to be

$$f_{ns} = f_{bw} \left(\frac{\Delta^2}{6f_s k_B T G_{RX} F_{DEV}} \right)^{\frac{1}{2N}}, \quad (4)$$

which leads to $f_{ns} = 166$ MHz. The noise shaping and filtering poles reduce the amount of in-band quantization noise. Thus as long as the required amount of noise shaping poles is met and the open-loop gain of the loop-filter amplifiers is sufficient, the quantization noise contribution to the receiver noise figure is limited to

$$NF_{QN} < 10 \log_{10} \left(\frac{2(M + N) + 2}{2(M + N) + 1} \right), \quad (5)$$

where M is the number of filtering poles.

A conceptual output spectrum of the current design state is shown in Fig. 3. Gain of 15 dB is applied to the -35 dBm in-band input signal at $f_{LO} + 2$ MHz. One filtering pole is located at $f_{bw} = 10$ MHz, which attenuates the incoming -15 dBm blocker at $f_{LO} + 100$ MHz by 5 dB, while two noise shaping poles at $f_{ns} = 166$ MHz ensure that the in-band noise is not dominated by quantization noise. The single-ended internal voltage swings of both the in-band input signal and blocker are

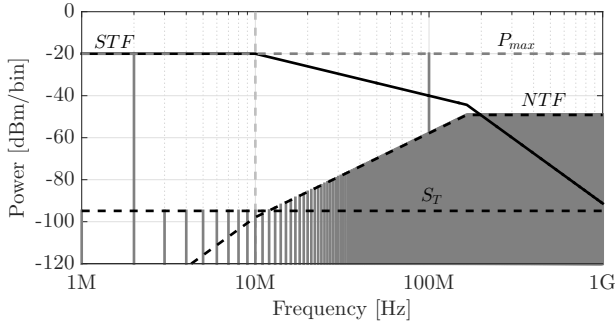


Figure 3. Conceptual output spectrum of the designed DDSR with -35 dBm and -15 dBm input tones at $f_{LO} + 2$ MHz and $f_{LO} + 100$ MHz, respectively. P_{max} signifies the maximum output level without significant distortion components and S_T marks the in-band noise floor (excluding quantization noise) at the output when gain is applied.

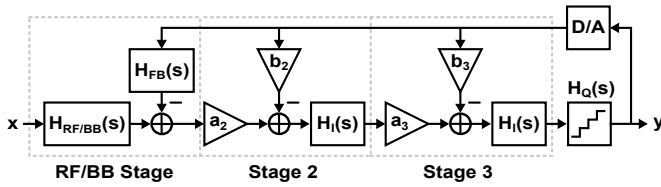


Figure 4. Simplified signal flow diagram of the DDSR.

limited to 31.5 mV ($P_{max} = -20$ dBm referred to 50Ω). Larger input powers will lead to increased distortion that degrades the sensitivity and SNDR of the receiver.

III. LOOP-FILTER DESIGN

In this section, we describe the design of the loop-filter and its components. A target signal transfer function (STF) is first formulated based on the results in Section II, which is then compared to the non-ideal STF of the DDSR, in order to obtain the loop-filter coefficients. The noise transfer function (NTF) is synthesized as a side product due to the shared nature of the poles. Then we will introduce non-idealities, such as the limited amplifier gain, device noise and the N-path filter, which allows us to obtain design specifications for the loop filter components. Analytical and behavioral simulations are used to verify the design.

A. Loop-filter coefficients

The STF of the DDSR should have minimal peaking. Thus, we will design the STF using two Butterworth filters in series, one filter for the filtering pole group and the other for the noise shaping pole group. As we want the filter responses to remain constant regardless of the varying f_s , the coefficients are referred to f_{bw} and f_{ns} based on to which pole group they belong to. The initial coefficients are thus $a_1 = 1$, $b_1 = 1$, $a_2 = 1$, $b_2 = 1$, $a_3 = 1$ and $b_3 = \sqrt{2}$. The first filter has a gain of $G_1 = G_{RX}$ and a pole at $\omega_{bw} = 2\pi f_{bw}$, which is followed by a second order filter with unity gain and bandwidth of $\alpha\omega_{bw}$,

where $\alpha = f_{ns}/f_{bw}$. The target STF is thus

$$H_T(s) = \frac{G_1}{\frac{s}{\omega_{bw}} + 1} \frac{1}{\frac{s^2}{\alpha^2 \omega_{bw}^2} + \sqrt{2} \frac{s}{\alpha \omega_{bw}} + 1}, \quad (6)$$

which can be re-arranged to

$$H_T(s) = \frac{G_1 \alpha^2}{\frac{s^3}{\omega_{bw}^3} + (1 + \sqrt{2}\alpha) \frac{s^2}{\omega_{bw}^2} + (\sqrt{2}\alpha + \alpha^2) \frac{s}{\omega_{bw}} + \alpha^2}. \quad (7)$$

The signal flow diagram of the DDSR with which we aim to implement the target STF is shown in Fig. 4. The transfer functions $H_{RF/BB}(s)$ and $H_{FB}(s)$ are BB referred transfer functions, which model the frequency translational properties of the first integration stage. $H_{RF}(s)$ defines the transfer function from the input of the first stage to the RF side of the mixer, whereas $H_{BB}(s)$ defines the transfer function to the BB side of the mixer. The feedback transfer function $H_{FB}(s)$ is defined at the RF or BB side of the mixer, depending on whether the input node of the second stage is at RF or, as in this case, BB. In zero-pole-gain form we have

$$H_{RF}(s) = G_{RF} \frac{\frac{s}{\omega_z} + 1}{\frac{s}{\omega_p} + 1}, \quad (8)$$

$$H_{BB}(s) = G_{BB} \frac{1}{\frac{s}{\omega_p} + 1}, \quad (9)$$

and

$$H_{FB}(s) = G_{FB} \frac{1}{\frac{s}{\omega_p} + 1}, \quad (10)$$

where G_{RF} is the gain from input to the RF side of the mixer ($f_{LO} \rightarrow f_{LO}$), G_{BB} is the gain from the input to the BB side of the mixer ($f_{LO} \rightarrow DC$), G_{FB} is the gain from the output to the BB side of the mixer, ω_p is the dominant pole frequency, and ω_z the zero frequency. The transfer function $H_I(s)$ models the limited gain of the BB integration stages, which becomes

$$H_I(s) = G_1 \frac{1}{\frac{s}{\alpha\omega_{bw}/G_1} + 1}, \quad (11)$$

when the unity gain frequency is $\alpha\omega_{bw}$. The quantizer with gain G_Q , sampling period t_s , delay t_q and zero-order hold operation (assuming a non-return-to-zero (NRZ) DAC) can be expressed as

$$H_Q(s) = G_Q \frac{1 - e^{-st_s}}{st_s} e^{-st_q}. \quad (12)$$

The STF of the DDSR in Fig. 4 can be calculated to be

$$H(s) = \frac{a_2 a_3 H_{BB} H_1^2}{\frac{1}{H_Q} + a_2 a_3 H_{FB} H_1^2 + b_2 a_3 H_1^2 + b_3 H_1}. \quad (13)$$

To gain insight on the behavior of the transfer function, we will first simplify the equations as follows:

- $H_Q = 1$. We will analyze the effects of the quantizer in section III-B.
- $a_k = G_k b_k$. This will effectively implement dynamic range scaling so that the dc gain of each stage is equal to the designed closed-loop gain of that stage.
- $G_1 = \infty$. We assume that the dc gain of the BB stages is sufficiently high.
- $\omega_p = \beta\omega_{bw}$.

Comparing the resulting $H(s)$ and $H_T(s)$ we obtain

$$\begin{cases} G_1\alpha^2 = \beta b_2 b_3 G_{BB}\alpha^2 \\ \beta + \alpha b_3 = 1 + \sqrt{2}\alpha \\ b_2 b_3 \alpha^2 + \beta b_3 \alpha = \sqrt{2}\alpha + \alpha^2 \\ \alpha^2 \beta b_2 b_3 + \alpha^2 \beta b_2 b_3 G_{FB} = \alpha^2 \end{cases} \quad (14)$$

which can be arranged to

$$\begin{cases} G_1 = \beta b_2 b_3 G_{BB} \\ \frac{\beta}{\alpha} + b_3 = \frac{1}{\alpha} + \sqrt{2} \\ b_2 b_3 + \frac{\beta b_3}{\alpha} = \frac{\sqrt{2}}{\alpha} + 1 \\ \beta b_2 b_3 + \beta b_2 b_3 G_{FB} = 1 \end{cases} \quad (15)$$

In a practical case $\alpha \gg 1 > \beta$, which leads to

$$b_3 \approx \sqrt{2}, \quad b_2 \approx \frac{1}{\sqrt{2}}, \quad \beta \approx \frac{G_1}{G_{BB}}, \quad G_{FB} \approx \frac{G_{BB}}{G_1} - 1. \quad (16)$$

From the above result we can conclude that if $f_{ns} \gg f_{bw}$ the two filters can be designed separately without significant error, even if they share the same feedback loop.

B. Quantizer effects

The quantizer has three significant qualities that affect the overall transfer function of the DDSR when it is added to the feedback loop. First, the quantizer samples and holds the input signal, which is effectively a zero-order hold function. Second, the quantizer gain is signal dependent. Third, a quantizer always has delay between its input and output. Although these qualities have been extensively studied [15], we would like to emphasize them in the context of the DDSR for two reasons. By taking the zero-order hold functionality into account separately, we can design the DDSR loop-filter in the CT domain, which simplifies the design procedure. Also, in a typical receiver design, signal levels at the input of the ADC are scaled by the preceding amplifier and filter stages so that the full range of the ADC is utilized. However, in a DDSR the input levels may be much smaller than what is optimal. Thus, even if a multi-bit quantizer is utilized, only single-bit quantization might take place, which in turn affects the STF and NTF through change of the quantizer gain.

When added to the feedback loop, the zero-order hold function of the quantizer distorts the designed CT STF and NTF. The filtering poles are practically unaffected, since they

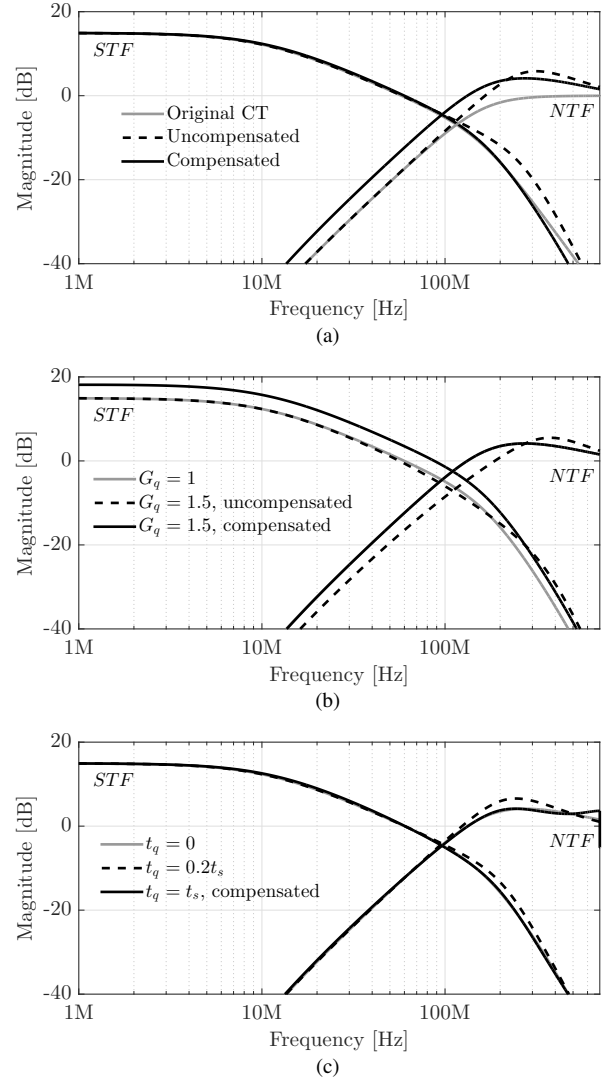


Figure 5. Uncompensated and compensated STF and NTF (a) with original CT STF and NTF after inclusion of the quantizer, (b) with different quantizer gains G_q , and (c) with different quantizer delays t_q .

are located well below f_s . However, the noise shaping poles are relatively close to f_s . Applying the zero-order hold function inside the feedback loop effectively moves the poles towards f_s , and the effect is stronger the closer the original poles are to f_s . A compensation factor ζ , obtained through empirical means, is applied here to pre-distort the pole locations. In this case, the pre-distortion is done by multiplying each noise shaping filter coefficient (a_2, a_3, b_2, b_3) with

$$\zeta = 1 - 2\frac{f_{ns}}{f_s}. \quad (17)$$

As illustrated in Fig. 5(a), adding the quantizer to the loop shifts the high-frequency poles higher, increasing the high-frequency gain of the NTF and adding peaking to both STF and NTF. Although adding high-frequency gain to the NTF is usually desirable, it can also increase sensitivity to clock jitter

[18] or make the modulator unstable. The compensation shifts the poles close to their original frequencies, which relaxes the peaking. The compensated STF follows the original CT STF when possible in the presence of a zero at f_s . Compared to the original CT NTF, the entire compensated NTF is shifted up by the amount of added high-frequency gain. The compensation method is effective up to the filter cutoff frequency $f_s / 4$. The pre-distorted coefficient values are $a_1 = 5.6$, $b_1 = 1$ (referred to f_{bw}) and $a_2 = b_2 = 0.54$, $a_3 = b_3 = 1.08$ (referred to f_{ns}).

In addition to pole shift due to sampling, signal dependent quantizer gain distorts the STF and NTF. In case the signal amplitude at the quantizer input is between $\Delta / 2$ and V_{FS} , the gain of the quantizer is approximately unity. However, if the input amplitude is less than $\Delta / 2$, even a multi-bit quantizer functions as a single-bit quantizer, whose gain is dependent on the statistical content of the signal. As a first order approximation, the gain of the quantizer increases as the signal amplitude decreases below $\Delta / 2$. As illustrated in Fig. 5(b), the increased quantizer gain moves the high-frequency poles of the STF and NTF further towards f_s and results in peaking, which might render the DDSR unstable. Furthermore, since the overall STF remains as before, there must be in-band attenuation in the internal nodes of the DDSR, which is undesired. The NTF and the internal voltage node responses can be recovered by dividing the feedback coefficients (b_1 , b_2 , b_3) by the quantizer gain as shown in Fig. 5(b) for a quantizer gain of 1.5. The overall STF will be amplified by the quantizer gain, which is unavoidable without adjusting the quantizer itself.

The quantizer and the feedback DAC always add delay to the feedback signal. As in traditional $\Delta\Sigma$ -modulators, the DDSR can handle only a certain amount of delay in the feedback before it becomes unstable [19]. In general, the higher the f_{ns}/f_s ratio is, the less feedback delay is tolerated. Excess loop delay of up to 20 to 30 % of t_s can usually be allowed without significant performance degradation. NRZ DAC implementations require additional hardware, such as a direct feedback to the quantizer, in order to compensate excess loop delay up to t_s [20], [21]. Fig. 5(c) shows the STF and NTF with quantizer delay $t_q = 0, 0.2t_s$ and t_s . While a delay of $0.2t_s$ can usually be tolerated, a delay of t_s would cause excessive peaking and result in unstable operation, and therefore compensation is required. The peaking is relaxed by moving the high-frequency poles away from each other by the same factor, i.e., in this case a_2 and b_2 are divided by $\sqrt{2}$ while a_3 and b_3 are multiplied by $\sqrt{2}$. Additionally, a direct feedback with $0.5t_s$ delay and a gain of 0.92 is added to the quantizer input.

C. Loop-filter amplifiers

The design specifications for the loop filter components can be obtained by including non-idealities. The loop-filter amplifiers are one of the key sources of non-idealities. The amplifier open-loop gain needs to be sufficient. The feedbacks divide the open-loop gain either to gain in the STF or to attenuation in the NTF, and thus the minimum requirement

for the total open-loop gain is

$$G_{\min} = G_{RX} + N20\log_{10}\left(\frac{f_{ns}}{f_{bw}}\right), \quad (18)$$

which equals $G_{\min} = 64$ dB. However, this would lead to the in-band quantization noise being equal to other noise sources and is therefore insufficient. A margin of up to 20 dB should be added to each stage to fully benefit from in-band noise shaping. Thus, the open-loop gain of the first stage should be 15 dB + 20 dB = 35 dB, while following two stages require gain of roughly 40 dB each. The RF transconductor of the first stage should ideally provide the gain across the receiver bandwidth f_{RX} , which leads to unity-gain bandwidth $f_u \approx 150$ GHz, if a single dominant pole is assumed. The BB transconductor unity-gain frequency requirement follows the general guideline of $f_u \approx f_s$, which has been deemed sufficient for CT $\Delta\Sigma$ modulators.

The loop-filter amplifiers are also the most significant contributors of noise in each DDSR stage. To obtain the required noise performance of each stage, we will divide F_{DEV} into contributions from the individual stages $F_{k,input}$, and then calculate the stand-alone noise factor of that specific stage F_k . The noise of the first stage will show at the receiver input directly, and thus we will use $F_{1,input} = F_1 = 2$ of the $F_{DEV} = 2.5$ noise budget here. This leaves 0.5 for other noise sources of which $F_{2,input} = 0.3$ will be directed to the second stage and ten times less $F_{3,input} = 0.03$ to the third stage. The noise factor for the second and third stage can be found by applying Friis' equation for noise. The noise factor for the k th stage in the chain, assuming $k - 1$ order in-band noise shaping and taking the closed-loop gain and amount of noise shaping at f_{bw} of previous stages into account, is:

$$F_k < 1 + F_{k,input} \frac{2(k-1) + 2}{2(k-1) + 1} \prod_{i=1}^{k-1} G_i \left(\frac{f_i}{f_{bw}}\right)^2, \quad (19)$$

where G_i and f_i iterate through the gain and pole location of the previous stages. This leads to noise factors $F_2 < 13.65$ and $F_3 < 315$. As expected, the noise factor of the second stage is still significant, while the stages after that can be relatively noisy.

As most of the noise is generated by the amplifiers, we can approximate the minimum required transconductance for each stage. For a single transistor in stage k , the g_m should be

$$g_{mk} > \frac{\eta}{R_s(F_k - 1)}, \quad (20)$$

where η is a process and transistor channel length dependent parameter and R_s is the source resistance. According to our simulations using a 28 nm FDSOI CMOS process, η varies from 1.8 to 1.2 for channel lengths between 30 nm to 60 nm and stabilizes to approximately $\eta = 1.1$ for 90 nm and longer channel lengths. Longer channels allow for higher dc gain and lower 1/f noise but increase parasitic capacitance. In order to meet the gain requirements, we will utilize only the longer channels for the main transistors and thus $\eta = 1.1$ is used in the calculations. Since (20) does not consider the noise of

the load device, the required transconductance in a practical amplifier implementation is higher. We assume that the noise of the load device is roughly the same as the input device, and thus the transconductance values are multiplied by a factor of 2 in Table II, which summarizes the amplifier requirements. These requirements should be met when the loading of the DAC and the proceeding amplifier are included.

Table II. LOOP-FILTER AMPLIFIER REQUIREMENTS.

	g_{m1}	g_{m2}	g_{m3}
Transconductance (g_{mk}) [mS]	> 44	> 3.5	> 0.14
Gain (G_{RF} , G_{fk}) [dB]	> 35	> 40	> 40
Unity-gain frequency (f_{uk}) [GHz]	> 150	> 1.4	> 1.4
Noise figure (NF_k) [dB]	< 3	< 11.4	< 25

D. N-path filter

Another source of non-idealities is the N-path filter formed by the mixers and baseband integration capacitors of the first stage. As there are several non-idealities, such as harmonic mixing and mixer switch resistance, functions $H_{RF/BB}(s)$ and $H_{FB}(s)$ in Fig. 4 have been formulated to tie the loop-filter coefficients to circuit parameters. For a quadrature mixer with 25% LO duty-cycle we can define

$$G_{RF} = \frac{g_{m,RF} Z_{RF} (R_{sw} Z_{sh} + 2\gamma R_{BB} (R_{sw} + Z_{sh}))}{2\gamma R_{BB} (Z_{RF} + R_{sw} + Z_{sh}) + Z_{sh} (R_{sw} + Z_{RF})}, \quad (21)$$

$$G_{BB} = \frac{\frac{\pi}{\sqrt{2}} \gamma R_{BB} Z_{RF} Z_{sh} g_{m,RF}}{2\gamma R_{BB} (Z_{RF} + R_{sw} + Z_{sh}) + Z_{sh} (Z_{RF} + R_{sw})}, \quad (22)$$

$$G_{FB} = \frac{4g_{m,FB} R_{BB} (Z_{RF} + R_{sw})}{R_{BB} + 2Z_{RF} + 2R_{sw}}, \quad (23)$$

$$\omega_p = \frac{2\gamma R_{BB} (Z_{RF} + R_{sw} + Z_{sh}) + Z_{sh} (Z_{RF} + R_{sw})}{C_{BB} R_{BB} Z_{sh} (Z_{RF} + R_{sw})}, \quad (24)$$

$$\omega_z = \frac{R_{sw} Z_{sh} + 2R_{BB} \gamma (R_{sw} + Z_{sh})}{C_{BB} R_{BB} R_{sw} Z_{sh}}, \quad (25)$$

where $\gamma = 2/\pi^2$, $g_{m,RF}$ and $g_{m,FB}$ are the input device and feedback device transconductances, Z_{RF} is the standalone impedance at the RF side of the mixer at f_{LO} , R_{BB} is the standalone resistance at the BB side of the mixer, C_{BB} is the total capacitance at the BB side of the mixer, and

$$Z_{sh} = \frac{1}{\frac{1}{\sum_{i=3,7,\dots}^{\infty} i^2 Z_s^*(if_{LO})} + \frac{1}{\sum_{i=5,9,\dots}^{\infty} i^2 Z_s(if_{LO})}}, \quad (26)$$

where $Z_s(if_{LO}) = Z_{RF}(if_{LO}) + R_{sw}$. For further information and derivation of the above equations the reader is kindly directed to [14], [22].

Equations (16) and (21)-(25) can be utilized to find component values for the first stage. As a simplification, the value of Z_{RF} is evaluated only at f_{LO} and its harmonics. As a consequence, (8)-(10) remain as first order equations, and

allow us to calculate the required C_{BB} and $g_{m,FB}$. From the unity gain frequency $G_{BB}\omega_p = G_1\omega_{bw}$ we can derive

$$C_{BB} = \frac{g_{m,RF}}{G_1\omega_{bw}} \frac{\sqrt{2}}{\pi} \frac{Z_{RF}}{Z_{RF} + R_{sw}}, \quad (27)$$

while the closed-loop gain condition $G_1 = G_{BB}/(1 + G_{FB})$ can be used to calculate $g_{m,FB}$, which can be expressed as

$$g_{m,FB} = \frac{C_{BB}\omega_{bw}}{2} - \frac{2}{\pi^2} \frac{Z_{RF} + R_{sw} + Z_{sh}}{Z_{sh}(Z_{RF} + R_{sw})} - \frac{1}{2\sqrt{2}R_{BB}}. \quad (28)$$

The mixer switch resistance has to be considered as well, since it limits the attenuation of blocker signals at the RF side of the mixer. The minimum gain at the RF side of the mixer is $H_{RF}(s \rightarrow \infty) = G_{RF}\omega_p/\omega_z$, from which we can solve the upper limit for the switch resistance

$$R_{sw} < \left(\frac{g_{m,RF}}{G_{blocker,max}} - \frac{1}{Z_{RF}} \right)^{-1}. \quad (29)$$

As we know the open and closed-loop gain and g_m requirement for the first stage, we can calculate the needed output impedance and then use (29) to find the required mixer switch resistance. To ensure that the switch resistance does not prevent us from reaching the 5 dB attenuation target, we calculate the required switch resistance for 8 dB of attenuation. After this, we can calculate the value of C_{BB} from (27). If we assume that the BB input resistance R_{BB} is large, $g_{m,FB}$ can be calculated from (28) after obtaining the value of Z_{sh} from (26). The resulting values are listed in Table III.

Table III. N-PATH COMPONENT VALUES.

	Value
RF transconductance ($g_{m,RF}$) [mS]	44
RF output impedance (Z_{RF}) [Ω]	1280
Mixer switch resistance ($R_{sw,max}$) [Ω]	9
N-path capacitance (C_{BB}) [pF]	55.9
BB input resistance (R_{BB}) [M Ω]	1
Feedback transconductance ($g_{m,FB}$) [mS]	1.6

E. Analytical and behavioral simulations

We will now verify the design so far with analytical frequency responses and transient behavioral simulations. The block-level transfer functions (8)-(12) are used to calculate the analytical transfer functions. The behavioral simulations use discrete real-time implementations of the block-level transfer functions, with the exception of the quantizer, which is implemented with a quantization function. The transient simulations use $f_s = 1.4$ GHz, while the real-time filters operate at an 8x internal sampling frequency of 11.2 GHz to simulate the continuous-time behavior. The quantizer delay t_q is neglected for now.

Fig. 6(a) shows the transfer functions from DDSR input to each stage output Y_k . As can be seen, the in-band gain of each integration stage is well-controlled in this design approach. The in-band gain of the first stage is 15 dB, while the other integration stages have unity gain. The RF node of the first integration stage $Y_{1,RF}$ has limited out-of-band gain due to

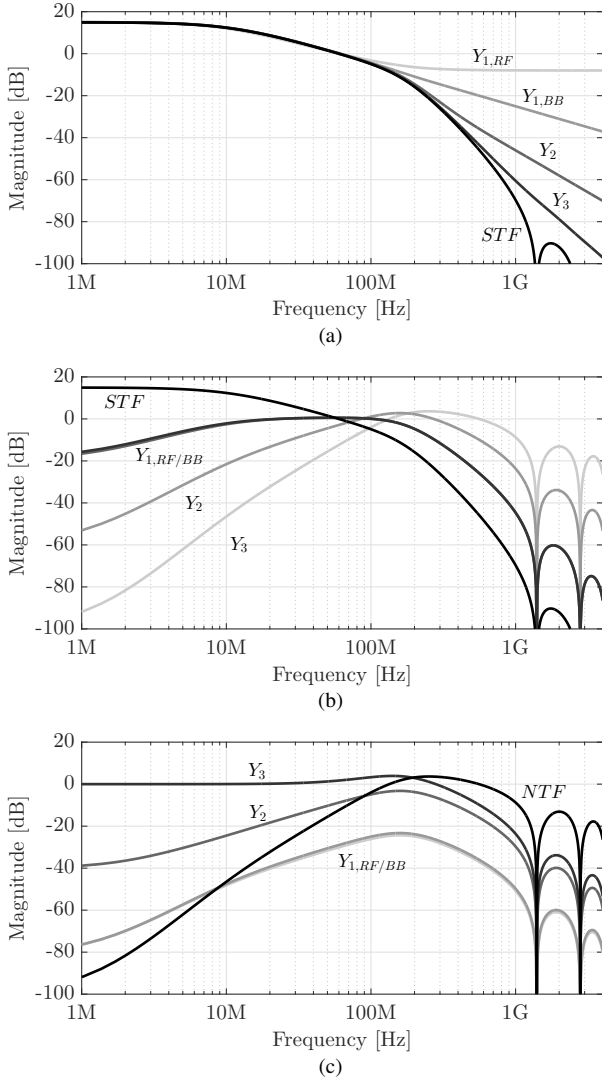


Figure 6. Transfer functions (a) from the input of the DDSR to the output of each stage Y_k , (b) from the output of each stage Y_k to the output of the DDSR, and (c) from the output of the quantizer to the output of each stage Y_k . The transfer function $Y_{1,RF}$ refers to the RF-side of the mixer and $Y_{1,BB}$ to the BB-side of the mixer.

the on-resistance of the mixer switches. This out-of-band gain limitation will ultimately define the far-away blocker resilience of the receiver together with the RF node linearity.

Fig. 6(b) shows the transfer functions from each stage output to the DDSR output. From the transfer functions we can observe how the circuit noise at each node contributes to the overall receiver noise. Compared to the STF, any noise at the output of the first stage will be attenuated by roughly 15 dB, with even more attenuation in the lower in-band frequency range due to the noise shaping. In the later stages, the attenuation increases as more stages participate in the noise shaping.

Transfer functions from the output of the quantizer to the output of each stage are shown in Fig. 6(c). The quantization

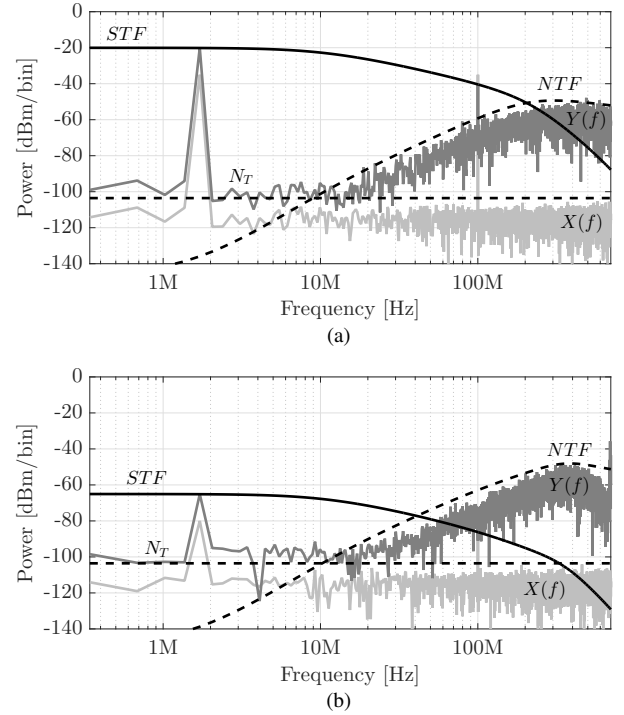


Figure 7. Input $X(f)$ and output $Y(f)$ spectra of the DDSR with overlaid analytical STF and NTF. The input consists of two tones at 1.71 MHz and 100 MHz. The input power of both tones is (a) -35 dBm and (b) -80 dBm. S_T marks the calculated thermal noise floor when in-band gain is applied.

noise level at the mixer node ($Y_{1,RF/BB}$) is especially important. The zero-order-hold functionality shapes the quantization noise spectrum, so that it has local minimums at $nf_s, n \in \mathbb{Z}$, and local maximums in between. When the LO and its odd harmonics upconvert the quantization noise, the total amount of quantization noise at RF in-band varies with the f_{LO}/f_s ratio due to quantization noise folding [6]. The most challenging cases occur when $f_{LO} = nf_s/4, n \in [1, 3, 5 \dots]$, since one or more of the local maximums in the upconversion products will be at f_{LO} . The position of the first pole at f_{bw} reduces the high-frequency quantization noise before the upconversion and thus alleviates the issue when $f_{LO} \gg f_s$. However, to minimize the folding, it should be ensured that $f_{LO} = nf_s/2, n \in \mathbb{Z}^+$.

A behavioral transient simulation of the DDSR with two -35 dBm input tones at 1.71 MHz and 100 MHz with added thermal noise is shown in Fig. 7(a). Both the in-band 1.71 MHz tone and the 100 MHz blocker tone follow the analytical STF, limiting the in-band tone output power to -20 dBm. As the quantizer input is well above the quantization step $\Delta/2$, the quantizer gain is approximately unity, and therefore the noise shaped spectrum follows the trend of the original NTF. In Fig. 7(b) the input power of each tone is -80 dBm and the quantizer output varies only between two states. The quantization gain is now larger, $G_q = 1.5675$. The high-frequency poles of the STF and NTF have shifted to higher frequencies due to the increased quantizer gain.

IV. IMPLEMENTING THE DDSR

Now that we have obtained the design equations and design specifications for the loop-filter components, the next step is to design the transistor-level circuits. In this section, we will first present the overall circuit design flow for a $g_m C$ -based DDSR, and then use it to design the required circuits. Steady-state ac simulation and transient simulation with noise are used to verify the transistor-level design.

A. Circuit design flow

We begin the circuit design by assuming that the input transconductor dominates the gain and device noise performance in each stage. Thus, we can use the specifications for the loop filter amplifiers as the starting point for circuit design. The simulation time required to verify the DDSR operation using transient simulation can be tens of hours for transistor-level circuits, and thus it is not feasible to use it for debugging. Instead, we will first design the receiver using steady-state ac simulation. The discrete feedback cannot be included in these simulations, and thus we replace the quantizer and the feedback DACs with ideal voltage-controlled current sources. We can now design the loop-filter amplifiers and mixers in a fraction of the transient simulation time. Our suggested design flow is as follows:

- 1) Design the input transconductor for each stage so that the requirements for the gain, unity gain bandwidth and input referred noise (transconductance) are satisfied
- 2) Calculate or simulate the standalone output impedance of the first stage input transconductor at the used f_{LO} to obtain Z_{RF}
- 3) Design mixer switches with R_{sw} that fulfils (29)
- 4) Calculate the value of C_{BB} using (27)
- 5) Assume that R_{BB} is high and calculate the value of $g_{m,FB}$ using (28)
- 6) Calculate the values of the remaining filtering stage capacitances: $C_k = g_{mk} / (b_k G_k \omega_{bw})$
- 7) Calculate the values of the noise shaping stage capacitances: $C_k = g_{mk} / (b_k G_k \alpha \omega_{bw})$
- 8) Calculate the remaining feedback transconductances: $g_{mk,FB} = g_{mk} / \left(\prod_{i=k}^{M+N} G_i \right)$
- 9) Scale the feedback transconductances to take the maximum quantizer input Q_{max} into account $g'_{mk,fb} = g_{mk,fb} Q_{max}$
- 10) Verify that the input referred noise of the receiver and the gain of each stage is as designed. Note that while the low-frequency poles are at the correct frequency, the high-frequency poles are at lower frequencies than expected since the quantizer is not present.
- 11) Verify the dynamic performance with transient simulation including noise by simulating SNDR vs P_{in}
- 12) Add an ideal quantizer and feedback DACs and repeat transient simulation
- 13) Design the feedback DACs and repeat transient simulation
- 14) Design the quantizer and repeat transient simulation

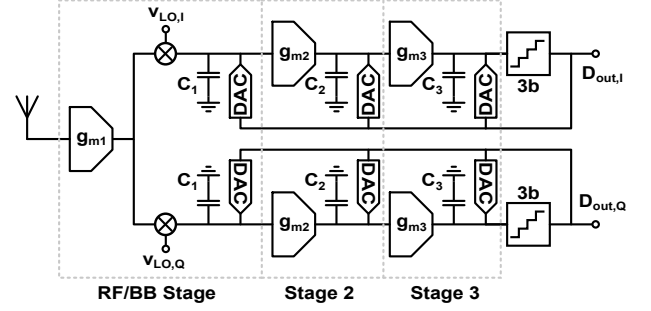


Figure 8. The $g_m C$ -based example DDSR.

B. Transconductor design

An example DDSR is designed using a 28 nm FDSOI CMOS process. The process enables high output impedance for the transistors, which in turn allows for high dc gain of 20 dB to 70 dB to be obtained from a single stage, depending on the used channel length. Thus, we are able to use single-stage transconductors in each of the integration stages. Push-pull circuit topologies with the minimum number of stacked transistors are utilized when ever possible. A simplified receiver schematic is shown in Fig. 8. We start by designing the transconductors, targeting the specifications in Table II.

The first stage transconductor g_{m1} is implemented with a pseudo-differential inverter shown in Fig. 9(a). The input of the receiver is matched with a resistor R_f buffered with a push-pull source follower to avoid loading the output node. Matching is achieved with $R_f \approx 300 \Omega$, since the gain of the first stage is set to 15 dB by the $\Delta\Sigma$ feedback. The transconductance of the main transistors is designed to meet the noise specifications, while avoiding unnecessarily high transconductance, which would lead to unpractically low mixer switch resistance due to the blocker gain requirement. The bandwidth of the g_{m1} is ideally at least f_{RX} . However, it is more important to fulfil the gain specification, as the $\Delta\Sigma$ feedback will ultimately flatten the gain to the designed 15 dB across f_{RX} .

As for the BB transconductors, we would like to have at least some common-mode and supply rejection. Thus, transconductors g_{m2} and g_{m3} are implemented with two parallel OTA structures with common-mode feed-forward shown in Fig. 9(b), adopted from [23]. The effective transconductance of the designed BB circuits is noticeably higher than the minimum requirement, mainly in order to push the dominating flicker noise to lower frequencies by using large devices while maintaining sufficient bandwidth. The performance of the designed transconductors is listed in Table IV.

Now that the main transconductors have been designed, we can proceed with designing the rest of the circuits. We need to find the minimum mixer switch on-resistance, which allows for over 5 dB of attenuation. Thus, using equation (29) we find that $R_{sw} < 10 \Omega$. A passive mixer with $R_{sw} \approx 8 \Omega$ was designed using NMOS transistors. Continuing the suggested circuit design flow, we can calculate the values of the integration capacitances and feedback currents, shown in Table V.

Table IV. SINGLE-ENDED PRE-LAYOUT TRANSCONDUCTOR PERFORMANCE.

	g_{m1}	g_{m2}	g_{m3}
Transconductance (g_m) [mS]	48	26.7	2.7
Output resistance (R_{out}) [k Ω]	1.2	21	117
Gain (G) [dB]	34	55	50
Noise figure (NF) [dB]	2.7	10	24
Supply current (I_s) [mA]	8	4	0.44
Gate drive (V_{eff}) [mV]	190	160	160
Saturation margin ($V_{satmargin}$) [mV]	300	330	330

Table V. COMPONENT VALUES.

	Value
FB transconductance / current 1 ($g_{m1,fb} / i_{1,fb}$) [mS/mA]	0.18
FB transconductance / current 2 ($g_{m2,fb} / i_{2,fb}$) [mS/mA]	2.67
FB transconductance / current 3 ($g_{m3,fb} / i_{3,fb}$) [mS/mA]	0.27
Integration capacitance 1 (C_1) [pF]	61.2
Integration capacitance 2 (C_2) [pF]	47.4
Integration capacitance 3 (C_3) [pF]	2.4

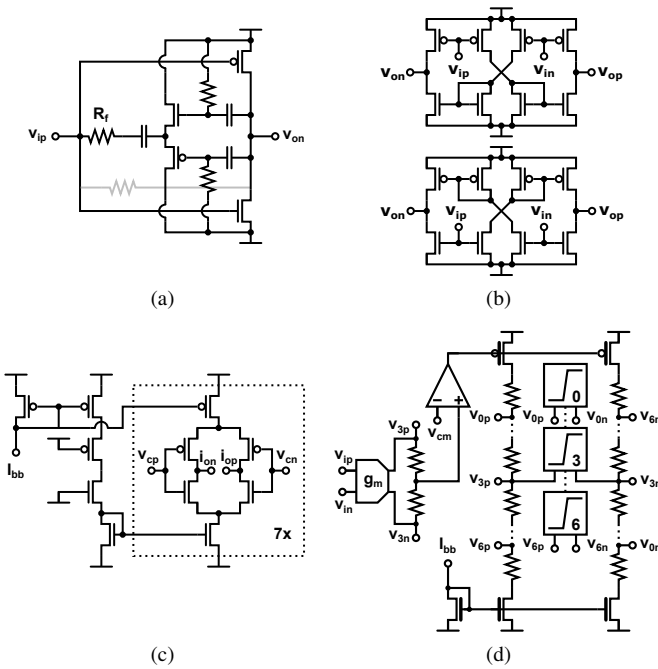


Figure 9. Circuit topologies for (a) RF transconductor, drawn single-ended for simplicity, (b) BB transconductors, (c) feedback DAC, and (d) quantizer.

C. Quantizer and feedback DACs

The 3-bit current steering DACs are implemented using thermometer weighting with push-pull current steering cells, as shown in Fig. 9(c). Since the second DAC has significantly higher current than the other DACs, two DACs with different W/L ratios are designed to maintain transistors in saturation. Matching for 3-bit accuracy is fairly straightforward, and thus the transistor dimensions are mostly dependent on a tradeoff between the flicker noise and non-linearity arising from the parasitic capacitance at the sources of the switch transistors. The resulting dimensions of the current source transistors is comparable to the corresponding BB transconductor, and

so there is a potential danger that the impedance level is modulated when the DAC output changes. To avoid this, the output impedance of each BB stage is intentionally lowered by connecting resistors between common-mode voltage and the outputs, so that the gain specification is still met.

The quantizer, shown in Fig. 9(d), utilizes string of resistors to generate appropriate offsets for comparators 0 to 6. The comparator circuit uses a differential-pair pre-amplifier with a diode and positive feedback load to reduce the kickback effects of the dynamic latch stage. The hysteresis of the comparator is designed to be below $\Delta/50$. The digital output is clocked with a flip-flop and then buffered to the feedback DACs using a tree structure of standard inverters available in the process. The excess-loop delay is 110ps and therefore compensation is not strictly necessary. Compensation might be required if dynamic element matching is used, but it is omitted here.

D. Tuning considerations

Finally, we need to consider which components should be or would benefit from being adjustable. The following cases can be identified.

- **Compensating for process variations** Monte-Carlo simulations indicate maximum transconductance variation of 10%. The resulting deviations in dc gain and pole frequencies can be compensated by adjusting the feedback DAC currents and integration capacitances.
- **Gain control** As discussed in Section II-B, 5 dB of gain control is required to meet the design objectives. A power efficient way to implement the gain control is to reduce the transconductance of the first transconductor by splitting the inverters into two unit inverters. As gain reduction is needed when the in-band power is high, the resulting increase in the circuit noise is not an issue.
- **Bandwidth control** The bandwidths of either the noise shaping or the signal filter can be controlled individually by changing the corresponding integration capacitance values, provided that $f_{bw} \ll f_{ns} \ll f_s$. Even if no bandwidth control is desired, the integration capacitances in the noise shaping stages might require adjustment. This is because the f_s varies with the f_{LO} , resulting in a change in the correction factor ζ as well. The severity of the effects are dependent on the f_{ns}/f_s ratio.
- **Dynamic range tradeoff** If the signal levels at the quantizer input are below Δ (in-band input power < -48 dBm), the quantizer operates as a single bit quantizer. Thus, excess dynamic range can be traded for lower power consumption by disabling 6/7 of the thermal bits of the quantizers and the feedback DACs.

E. Transistor-level simulations

We will begin the verification of the pre-layout transistor-level DDSR without the discrete feedback. The S_{11} and the transfer functions from the input to the output of each integration stage obtained using steady-state AC simulation are shown in Fig. 10(a). The stage gains are as intended across the carrier frequency range and the receiver is matched in the in-band.

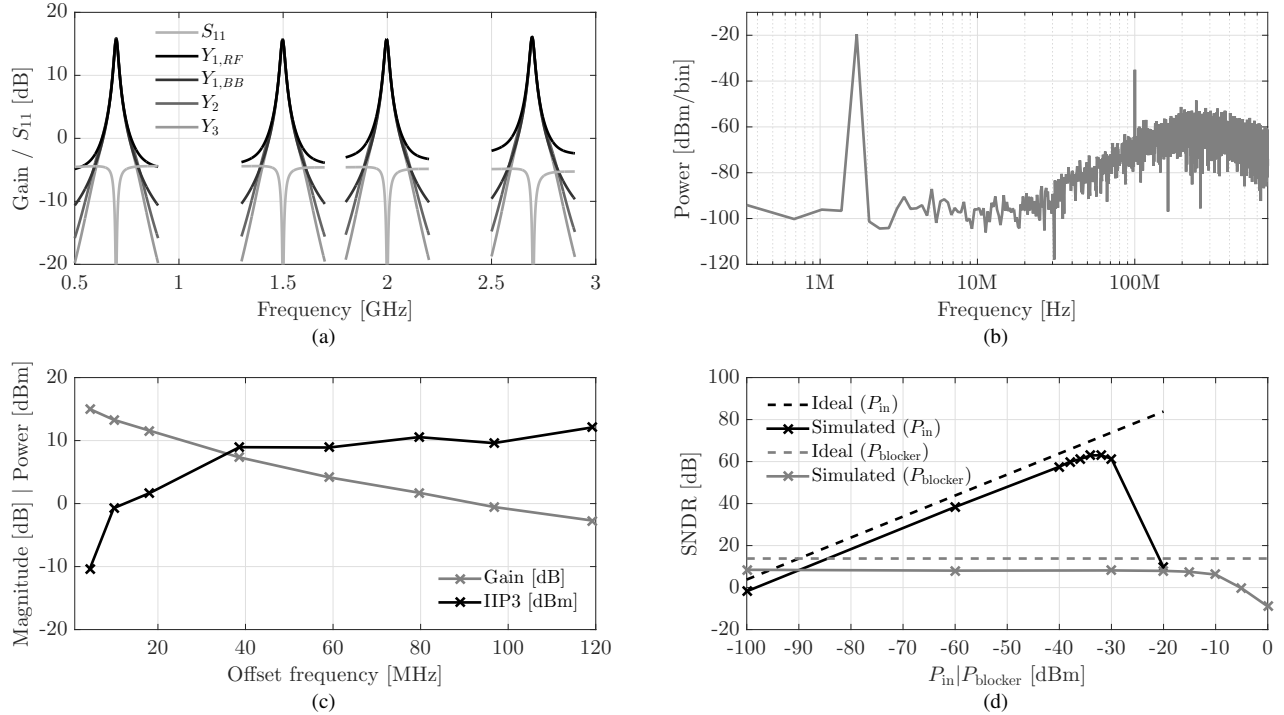


Figure 10. Transistor-level simulations of the designed DDSR showing (a) S_{11} and gains to each stage output when $f_{LO} = 0.7$ GHz, 1.5 GHz, 2.0 GHz and 2.7 GHz, (b) output spectrum of the DDSR when -35 dBm input tones at $f_{LO} + 1.71$ MHz and $f_{LO} + 100$ MHz are applied, (c) gain and IIP3 at different offsets from f_{LO} , and (d) ideal and simulated SNDR when the P_{in} or the $P_{blocker}$ is swept

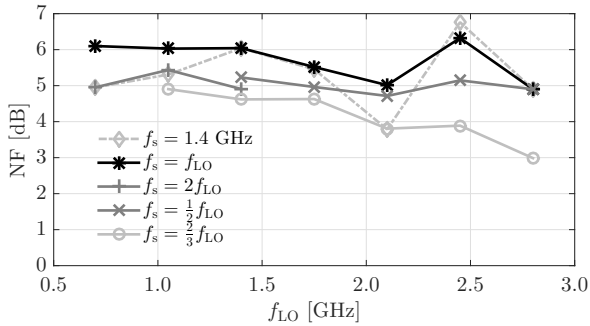


Figure 11. Receiver noise figure NF_{RX} when f_{LO} is varied from 0.7 GHz to 2.8 GHz and f_s is either constant or tied to the f_{LO} with factor 1, 2, $\frac{1}{2}$ or $\frac{2}{3}$.

The BB bandwidth is 10 MHz as designed. For more accurate results, we now switch to the transient simulations with noise. All of the following simulation use the parameters in Table VI unless mentioned otherwise. In addition to the amplifiers, mixers, the quantizer and the feedback DACs, also the LO buffers, the clock tree and the buffer inverters for the digital feedback are transistor-level designs. Bond-wire inductance and pad capacitance are included in simulations.

Fig. 10(b) shows the output spectrum of the DDSR. The quantization noise has the expected 40 dB/decade slope below f_{ns} . Peaking is visible near f_{ns} due to the excess-loop delay

Table VI. DEFAULT SIMULATION PARAMETERS.

Parameter	Value
LO frequency (f_{LO}) [GHz]	1.4
Sampling rate (f_s) [GHz]	1.4
Input offset frequency ($f_{in} - f_{LO}$) [MHz]	1.71
Blocker offset frequency ($f_{blocker} - f_{LO}$) [MHz]	100
Input power (P_{in}) [dBm]	-35
Blocker power ($P_{blocker}$) [dBm]	-35

added by the quantizer and the feedback DACs, but the operation remains stable. The in-band tone is amplified by 15 dB as designed. To our disadvantage, the chosen matching method leads to higher input impedance for the blocker, resulting in an overall gain of 0 dB, which is 5 dB more than intended. This can also be observed in Fig. 10(c), which plots the receiver gain and IIP3 with different f_{LO} offsets.

Fig. 10(d) shows the ideal and simulated SNDR when either the P_{in} or the $P_{blocker}$ is swept. The blocker tone is not present when the P_{in} is varied, while the $P_{in} = -90$ dBm during the $P_{blocker}$ sweep. When compared to the ideal SNDR curves, we observe that the $NF_{RX} \approx 5$ dB up to $P_{in} \approx -35$ dBm, after which distortion components begin to desensitize the receiver. The in-band and out-of-band P_{-1dB} compression points are -25 dBm and -10 dBm respectively.

Fig. 11 shows the receiver noise figure NF_{RX} when the f_{LO} is swept across the receiver bandwidth f_{RX} with different f_s . The NF_{RX} is obtained by comparing the output SNDR of

Table VII. PERFORMANCE SUMMARY AND COMPARISON

	This work (Simulated)	[8]	[13]	[6]	[7]
Carrier Frequency (f_{RX}) [GHz]	0.7 to 2.8	0.6 to 3	0.7 to 2.7	0.9	0.4 to 4
Gain (G_{RX}) [dB]	15	50	-	40	-
Noise Figure (F_{RX}) [dB]	3 to 5	2.4 to 3.5	5.9 to 8.8	6.2	16
Blocker P_{-1dB} [dBm]	$-10@10f_{bw}$	$-20@10f_{bw}$	$-14@10f_{bw}$	$-18@20f_{bw}$	-
Peak SNDR [dB]	63	49	43	56	52 to 65
BB bandwidth (f_{bw}) [MHz]	10	10	7.5	28^3	10
Power [mW] @ Supply [V]	35@1	35.5 to 53.5@1.2	90@1.1	80@1.2	17 to 70.5@1.1,1.5 ⁴
Architecture	LNA first g_mC DDSR	LNTA first DDSR	LNA first DDSR	LNA first DDSR	LNTA first direct RF-to-digital
CMOS process	28 nm FDSOI	65 nm	40 nm	65 nm	65 nm

1) Blocker offset normalized to BB bandwidth (f_{bw}) 2) Extrapolated value 3) BW with reported NF is 4MHz 4) LNTA supply

a -80 dBm input tone to the ideal SNDR. With a constant $f_s = 1.4$ GHz, the SNDR of the receiver drops due to the quantization noise folding with certain values of f_{LO} . For optimal performance, the f_s is tied to the f_{LO} with a factor of $\frac{1}{2}$, $\frac{2}{3}$, 1 and 2, while both f_{LO} and f_s are kept within 0.7 GHz to 2.8 GHz, adjusting the noise shaping stages according to (17). The factors $\frac{1}{2}$ and 2 show approximately constant performance, while the best performance is obtained with the factor $\frac{2}{3}$.

The designed DDSR is compared to similar RF-to-digital implementations in Table VII. Based on our experience obtained from manufactured DDSR prototypes, the simulations suggest better performance in terms of out-of-band linearity and maximum SNDR, while offering competitive noise figure.

V. CONCLUSION

In this paper we showed that the common practices for neither the receiver nor the $\Delta\Sigma$ modulator design yield optimum performance for the DDSR, and proposed a systematic design method for g_mC based DDSRs. The developed method improves performance and simplifies the design flow by combining the gain partitioning, noise considerations and loop-filter design. Using the proposed design method, the loop-filter can be designed in the CT domain by pre-distorting the pole shifts caused by the discrete feedback. In addition, the use of a variable sampling frequency is enabled, which can be used to avoid quantization noise folding without adding extra hardware. The design method was demonstrated by designing a g_mC based DDSR using a 28 nm FDSOI CMOS process. The simulations indicate state-of-the-art performance.

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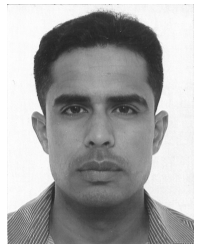
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