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Published in:
Proceedings of the 2018 7th Electronic System-Integration Technology Conference, ESTC 2018

DOI:
10.1109/ESTC.2018.8546398

Published: 26/11/2018

Document Version
Publisher's PDF, also known as Version of record

Process Integration and Reliability of Wafer Level SLID Bonding for Poly-Si TSV capped MEMS

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***Abstract*— The objective of this study was to develop a fully integrated process for wafer level MEMS packaging utilizing Poly-Si through silicon via (TSV) capped MEMS devices. First, interconnection metallurgy and Solid Liquid Interdiffusion (SLID) bonding process was optimized. Then sc. "vias before bonding" capping process and contact metallizations for Poly-Si TSVs were developed. Finally, the process integration was demonstrated by using piezoelectrically driven MEMS actuators. However, several design and manufacturing related challenges were observed and detailed failure analysis were carried out to resolve these problems.**

Keywords—MEMS, Process integration, Wafer level SLID bonding, Reliability

I. INTRODUCTION

Functional structures utilized in Micro Electro Mechanical Systems (MEMS) have to be electrically connected and often hermetically encapsulated. Wafer level Solid Liquid Interdiffusion (SLID) bonding, also known as Transient Liquid-Phase (TLP) bonding, a sub-category of the metal bonding, is becoming an increasingly attractive method for industrial usage[1-5]. The main advantages of SLID are the possibility to utilize a low melting point metal to reduce the bonding temperatures, a significant reduction of the bonding footprint that is required for metallic bonding as well as the possibility to achieve simultaneously vertical electrical interconnections when utilizing through silicon vias (TSVs).

Out of the several different material options demonstrated, Ag-In [6-8], Au-In [2, 9-14], Cu-In [15], Ag-Sn [16, 17], Ni-Sn [2, 3, 18-20], Au-Sn [21-28] and Cu-Sn [5, 29-38], Au-Sn and Cu-Sn based metallurgies are the most commonly utilized in SLID systems. In general, the formation of the bond in the SLID process occurs in four consecutive stages: melting, dissolution, intermetallic compounds (IMCs) formation that leads to isothermal solidification and homogenization of the interconnection structure. Immediately after the melting of the low melting temperature metal (i.e. Sn or In) rapid dissolution of the high melting temperature metal (i.e. Ag, Au, Cu or Ni) occurs. The dissolution rate is system dependent and is mainly affected by the solubility of the high melting temperature metal to the liquid. Once local supersaturation of the low-melting material occurs, subsequent isothermal solidification of the IMCs takes place. Finally, the bond is homogenized via solid-state reactions.

The objective is to study MEMS wafer level packaging with a fully integrated SLID bonding process for Poly-Si TSV capped MEMS devices. The development consists of studies for the process sequence and deposition methods required for the processing of sensitive MEMS structures and multi-stack and multi-material interconnection layers. A prime example of this is the deposition of contact metallizations and bonding materials that limits the design features and process integration options. Sensitive MEMS structures must be protected from these deposition processes, particularly when harsh chemical or electrochemical methods are used and how the bonding materials are protected during MEMS structure release. In addition, the integration of TSVs, TSV contact metallizations and the design and manufacturing of the 3D network of electrical paths for the functional structures are studied. Finally, a general refection is made on the wafer-level bonding as a whole, how the consecutive processing steps can be optimized for optimal functionality and reliability. This requires a thorough understanding of the structures and the underlying material compatibility, global and local thermo-mechanical stresses and volumetric changes as materials evolve over a processing and operational lifetime. In this paper the design, process and reliability assessment of sc. "vias before bonding" capping process will be carried out in three consecutive stages. First, the selection of bonding metallurgy is made and the mechanical reliability will be assessed. Second, the contact metallization structures, Poly-Si TSV manufacturing process flow as well as cap wafer backside processes are developed from manufacturability and reliability viewpoints. Finally, process integration for Poly-Si TSV capped MEMS will be demonstrated.

II. Materials and Methods

Standard double side polished 150 and 200 mm silicon wafers (thickness 400 µm) were used as device and cap wafers. Both wafer types were <100> with p-doping and were manufactured by Okmetic. For the first phase metallurgical studies a 40 nm TiW layer was sputtered as an adhesion layer between the silicon and the seed layer. A 100 nm thick gold or copper seed layer was sputtered to both wafers. The seal ring geometry was rounded-corner rectangle with dimensions of 1,576 µm x 783 µm and the width of the ring was 60 µm. 4 µm and 6 µm thick gold and copper layers were electroplated. Then a 2 µm thick tin layer was electroplated on top of the Au or Cu layers. In order to study the effect of an additional nickel contact metallization between TiW and electrochemical Au, a 200 nm thick nickel film was sputtered prior to seed layer deposition. More detailed description can be found from [39]. EVG 610 bond aligner and EVG 510 bonder were used in the bonding tests. For the electrical bonding tests, 400µm p-doped DSP dummy MEMS wafers were bonded onto 625µm TSV cap wafers from Okmetic. The dummy MEMS wafers had a 500nm thermal oxide insulation, the cap wafers Poly-Si filled TSVs with an oxide liner. TSVs were arranged into 30 TSV matrixes where the TSVs had a 250µm pitch. 2500µm die size was used in the electrical test layout.

For the cross-sectional analysis, the samples were prepared both using standard metallographic methods as well as ion-polishing using the Gatan Ilion+. The SEM+EDS analysis was performed with a JEOL JSM-6330F field emission scanning electron microscope with Oxford Instruments INCA X-sight EDS equipment. The shear and tensile teste were executed with MTS 858 Table System that contained a Flex Test 40 Digital controller and a MTS SilentFlow HPU system. Detailed description of the test setup is presented in [39]. The High Temperature Storage (HTS) aging test was conducted with a Heraeus Instruments oven for 1000 hours at 150°C. The Thermal Shock (TS) test was performed with an ESPEC TSA-71 S Thermal Shock chamber system. The operational temperature range was -40–+125°C with 33 °C/min ramp rate, 10 min dwell time, for both high and low temperature, and a total cycle time of 30 min. Samples from were exposed to 1000 cycles.

III. Results and Discussion

A. *Phase 1- Selection of bonding metallurgy and reliability assessment*

Simple seal ring structure between dummy Si wafers was used to study the bonding metallurgy and assess the mechanical reliability performance of both as bonded state as well as after aging. High tensile (>80 MPa) and shear (>120MPa) strengths were observed for both Au-Sn and Cu-Sn based metallurgies directly after bonding. In addition, the results show that the CuSn SLID interconnection microstructure is very stable against aging, with very high detected shear (~250MPa) and tensile (~100MPa) strengths even after HTS and TS tests. However, results showed that in the AuSn SLID interconnections the strength and fracture mechanisms are more affected by the aging treatments. The decrease in strength was associated with increased amount of interfacial failures. Therefore, as the AuSn bond microstructure and metallization layers are more complex, this complexity plays a significant role in the bonds mechanical reliability. A ~~More~~more comprehensive analysis can be found from [39]. Based on the first phase results, it was decided that the further steps would utilize the Cu-Sn metallurgy.

B. *Phase 2- Contact metallizations and SLID bonding for Poly-Si TSVs*

Electrical characterization of the bond layers was done with a "vias before bonding" process run. The benefit of this approach is the possibility to process the cap and the MEMS wafers in parallel. This makes the process integration easier and reduces the total process duration. The cap and the dummy MEMS wafers were processed side by side: First a 500nm Si alloyed Al-layer was sputtered and patterned on both of the wafers. On the cap wafer the Al(Si) layer were used to distribute the electrical signals from the TSVs to the bond layers. On the dummy MEMS wafer the Al(Si) layer was used as redistribution layer from one bond pad to another. On top of the redistribution layer a 500nm LTO oxide layer was used as a passivation. Contact openings were made to the bond contact locations. A 300nm thick copper seed layer with 40nm TiW adhesion layer was then used as a plating base for through photoresist plating. Copper layer was then electrodeposited onto the dummy MEMS wafers and CuSn layers onto the cap wafers. After electroplating the photo resist and seed layers were removed and the wafers were bonded with a wafer-level bond process at 320°C for 30 minutes. After the bonding the TSVs were revealed by thinning the cap wafer to approximately 150µm thickness (see Fig. 1). An insulation and redistribution layers were then deposited and patterned.

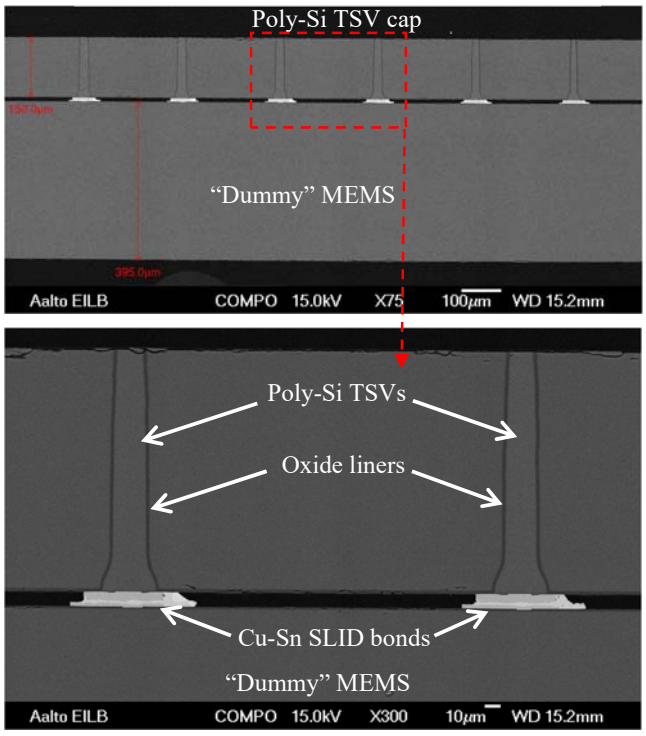
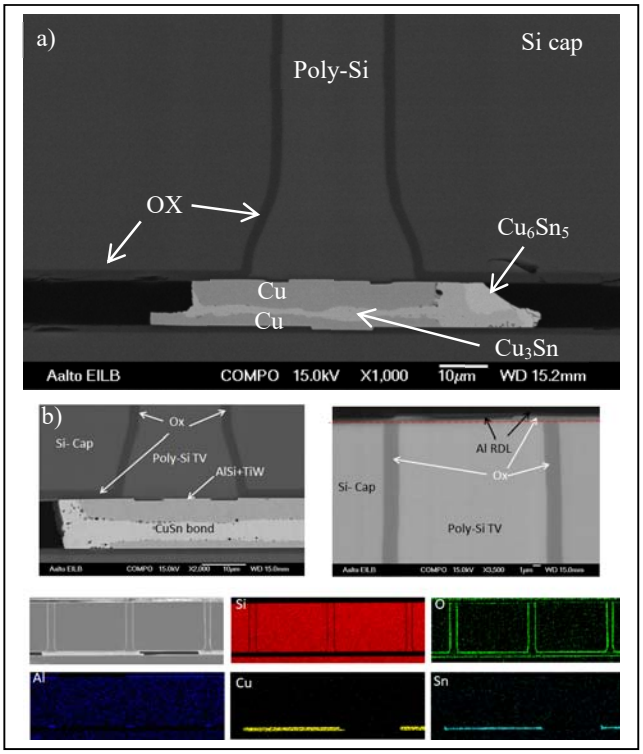


Fig. 1. SEM micrographs from partially processed wafer i.e Cu-Sn SLID bonding and cap sided thinning has been done but insulation and redistribution layers not deposited.

Figure 2 shows the cross-sectional SEM micrographs with EDS element map from fully processed sample. As can be seen from Fig. 2 a) targeted Cu-Cu_3Sn-Cu microstructure has been achieved. However, small amount of squeeze-out can be seen from the right side of the bond where some residual Cu_6Sn_5 is observed. In addition, several cracks in the Si are present. In order to confirm that these cracks were artefacts caused by manual sample manufacturing (grinding and polishing) few samples were manufactured with ion-polishing technique. As can be seen from Fig. 2 b) these cracks were indeed introduced by the grinding process and are not observed in the ion-polished



samples.

Fig. 2. SEM micrographs of the fully integrated MEMS package. Including Al redistribution layer, Cap wafer poly-Si TSVs, and wafer level SLID bonding providing electrical interconnection between the device and cap wafer as indicated by the SEM-EDS elemental analysis.

After processing, the TSVs and the bond layers were characterized with electrical measurements. The electrical measurements showed that all measured TSVs and bond contacts were functional. Kelvin TSV test structures revealed that the resistance from the top wafer to the MEMS wafer varied from 10Ω to 15Ohms, with average resistance of 12Ω. This resistance includes the TSV, the dummy MEMS and cap wafer RDL layers, bond layer and all contact resistances. Reliability of the test structure was studied with a 1000h high temperature storage (HTS) at 150°C and thermal shock (TS) test with 1000 cycles from -40°C to 125°C. These tests could not detect a measurable difference in electrical performance for the electrical test structures.

C. Phase 3- Process integration for Poly-Si TSV capped MEMS

The objective of the third phase was to bond real MEMS device wafers, containing various types of gyro structures, to cap wafers having poly-Si TSVs by utilizing the data obtained from the previous development phases. In addition, the critical process integration step was to develop a method to electrochemically deposit the copper metallization to the device wafer without destroying the sensitive MEMS structures. This was achieved with several lithography steps by first fabricating the active device structures, then protecting them during the Cu plating process and finally protecting the Cu layers during the release of the functional MEMS structures. The manufacturing process steps are shown in Fig. 3.

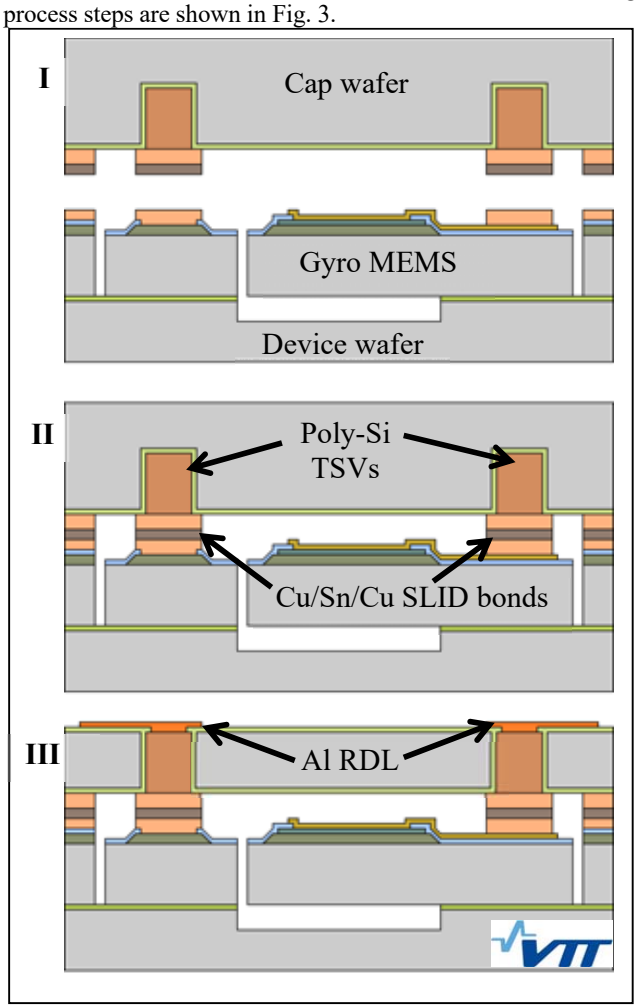


Fig. 3. Schematic illustration of the main manufacturing steps for the "vias before bonding" process

First, the cap and MEMS wafers were manufactured separately, followed by wafer bonding and finally the electrical connections to the backside of the cap wafers were made. The cap wafer manufacturing, the wafer-level bonding and backside processing were identical to that of phase three. The MEMS wafer consists of a Cavity-SOI substrate with piezoelectrically

driven actuators were similar to those described in [40]. The sense and actuation elements, consisting of a bottom molybdenum electrode layer, 1000 nm thick AlN, and top molybdenum electrode, were all deposited and patterned separately. Further passivation layers and interconnect metal layers are added to the process to protect the structures and later connect to the TSV during bonding. The release etch for the MEMS elements is performed in an STS ASE deep reactive ion etch tool, with added resist to protect the Cu and Sn metals during plasma etch. Post-etch cleaning is done with oxygen plasma and wet resist removal, including drying in IPA, before the wafer-level CuSn SLID bonding process.

Fig. 4 shows SAM images of the wafer pair after bonding. As can be seen the bonding looks successful and bonding accuracy seems adequate. In addition, no problems were noted during the thinning of the cap wafer to reveal the poly-Si TSVs. However, when the thinned wafer-pair was subjected to PECVD oxidation process at 300°C, for subsequently manufacturing the Al redistribution layer (RDL) on top of the cap wafer, severe cracking of the wafers were observed.

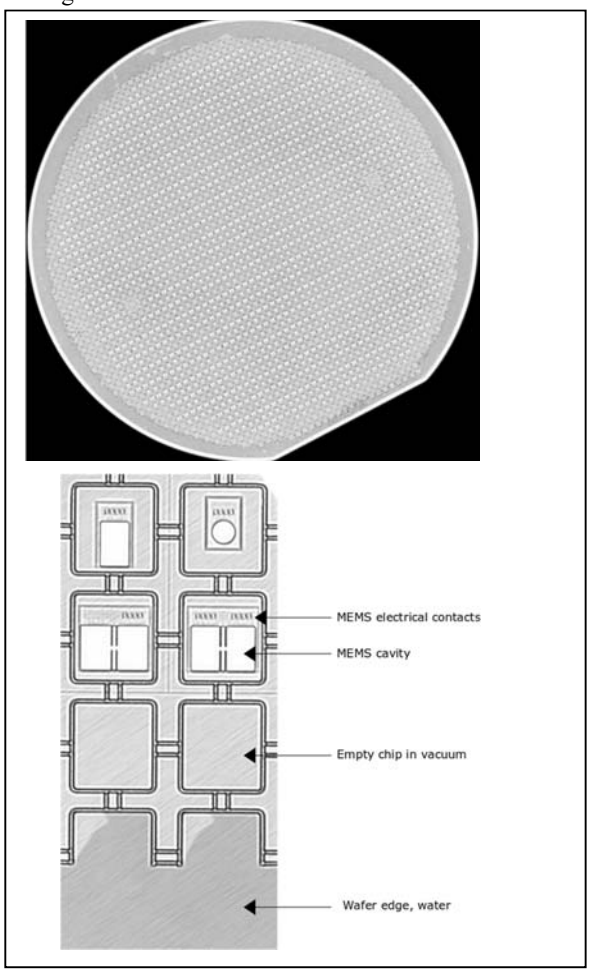
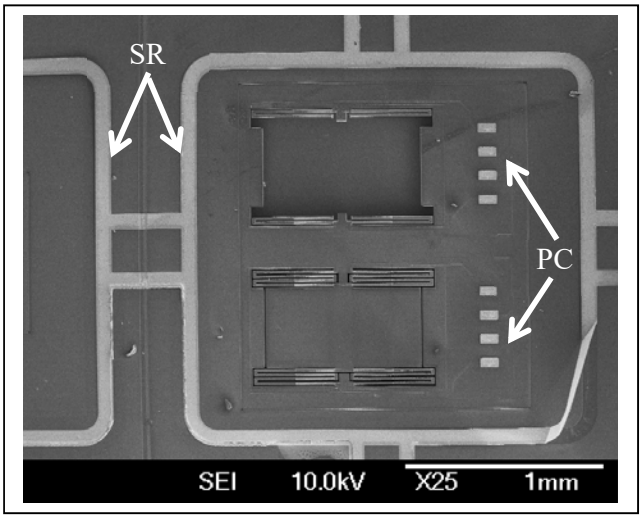


Fig. 4. SAM images of the Poly-Si TSV cap and MEMS waferpair after bonding.

During failure analysis (See Fig 5 where cap is detached to reveal one of the test structures) a mask error was found at the cap wafer side that created topography difference between the electrical contacts and sealing rings. Additionally a second mask error was found from the MEMS wafer, which had created a trench located at the sealing rings. Together these two design errors created a leakage point through the sealing rings where moisture was able to penetrate. This explanation is also supported by the fact that electrical test structures fabricated in the same run with a different mask set, survived the fabrication

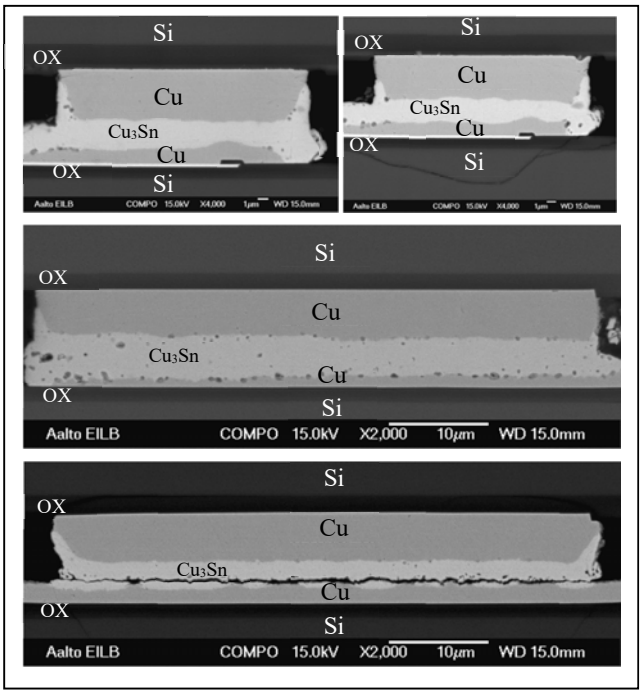


run.

Fig. 5. SEM image of the detached MEMS element showing the one of the gyro test structures, point contacts (PC) and sealing rings (SR).

When the fractured parts of the wafers were analyzed (See Fig. 6.) it was discovered that the CuSn SLID bonds had formed adequately in a majority of the wafer. About ±5µm bonding misalignment was detected. Based on the cross sectional samples it was observed that many of the bonds are of high quality (See Fig. 6a.) and the Cu-Sn reactions have proceeded to Cu_3Sn phase as targeted, however, few different types of defects were also seen. Some electrical point contacts (PC) had a clear crack underneath the bond as shown in Fig 6b. These cohesive cracks propagate through silicon indicating that there was significant stress present during the bonding and PECVD process. It was also noted that due to some design errors the bonded wafers had local topography differences, both in the cap as well as device wafer. These topography differences cause open cavities between the sealing rings and, thus, may form a path for contaminants, for example water during SAM imaging, to penetrate between the bonded wafers. Therefore, the most plausible explanation for the observed wafer cracking is the evaporation of the contaminants during the PECVD process that cause excessive pressure within the structure. Additional defects that were observed, can be seen from Fig. 6b are voids inside the Cu_3Sn phase. Voids observed within Cu_3Sn are intermetallic voids, often referred to Kirkendall voids. IMC voids form as a result of inconsistencies with the Cu electroplating process, such as uncontrolled additive concentrations, current densities or even the agitation rate. As the additives used in the Cu electroplating

process are not able to synergistically function to control the deposition behavior, they breakdown and are incorporated as impurities into the electroplated Cu. During the dissolution of Cu into liquid Sn, impurities in the Cu grain structure cause IMC voids to form once Cu diffuses in to the Cu-Sn IMCs. In addition, some bonds that were only partially formed were also detected. Typically these bonds located at the peripheral area of



the wafer. The reasons behind these defective could be variation in the bonding pressure or plating thicknesses at the edge of there wafers.

Fig. 6. SEM micrographs from electrical point contact (a,b) and sealing ring (c,d) the cross sections.

IV. Conclusions

This work has demonstrated a three-phase wafer-level SLID bonding for Poly-Si TSV capped MEMS process. The phases include, (i) selection of the bonding metallurgy and reliability, (ii) design of the contact metallizations and integration of the Poly-Si TSV with SLID bonding and (iii) process integration of Poly-Si TSVs capped MEMS. Based on the results it can be concluded that process integration for utilizing Poly-Si TSV caps for creating both electrical interconnections and hermetic encapsulation for MEMS devices was successfully demonstrated. The CuSn metallurgy was selected over AuSn for its high thermomechanical resilience during the reliability assessment and the simplicity of the resulting microstructure. However, few design and manufacturing related challenges need to be further studied in order to unambiguously verify the feasibility of proposed approach, such as Si cracking, IMC void formation and bonding yield at the periphery of the wafers. Nonetheless, CuSn SLID bond utilization for wafer-level Poly-Si TSV capped MEMS exhibits encouraging promise for industrial usage.

Acknowledgment

This work has been carried out as a part of an Eniac Project Lab4MEMS II (grant number 2013-2-621176). The authors would like to acknowledge the Innovation Funding Agency Business Finland (formerly Tekes), Okmetic and Murata Electronics for financial support. We acknowledge the provision of facilities and technical support by Aalto University at OtaNano - Nanomicroscopy Center (Aalto-NMC).

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