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Cast Monocrystalline Silicon: New Alternative for Micro- and Nano-Electromechanical Systems?

Zhengjun Liu, Ville Vähänissi, Nikolai Chekurov, Ilkka Tittonen and Hele Savin

***Abstract*—Casted silicon wafers dominate the current photovoltaic (PV) market due to much lower fabrication costs as compared to well-known Czochralski (Cz) –growth. Traditionally casted silicon ingots have been multicrystalline, but recent developments in casting technology have enabled also the growth of single crystalline (sc) silicon ingots. While the resulting sc-Si ingot quality is naturally high enough for PV, it is not sufficient for the integrated circuit (IC) industry, mainly due to the increased amount of intrinsic point defects and dislocations in comparison to Cz-Si. However, many applications that do not have such stringent requirements for substrates, such as micro- and nano-electromechanical systems (MEMS, NEMS), could potentially find this material beneficial. Indeed, here we take the first step in studying the applicability of cast mono-Si for such applications. More specifically, we focus on advanced focused ion beam lithography combined with deep reactive ion etching for NEMS and wet etching for MEMS. Our results show that the quality of cast monoSi is high enough for successful patterning in both micro- and nanoscale. Sub-micron resolution is achieved and the Ga^+ doses required for successful patterning are comparable to conventional Cz-Si. The preliminary results presented here thus show great promise for cast mono-Si as a low-cost alternative for micro- and nanoelectromechanical systems.**

***Index Terms*—cast mono-Si, focused ion beam, MEMS, monolike silicon, NEMS, photovoltaics, quasimono silicon**

I. Introduction

CRYSTALLINE silicon dominates as substrate material in the semiconductor industry ranging from integrated circuits (IC) to micro- and nano-electromechanical systems (MEMS, NEMS), sensors, photovoltaics (PV) and other optoelectronic components. Silicon wafer manufacturing is today a highly mature technology, mostly lead by the IC industry that sets stringent requirements for the substrate quality and mainly determines the used wafer sizes. Traditionally other industries, including MEMS, follow the footsteps of IC and thus rely heavily on existing silicon crystal growth methods such as Czochralski (Cz) and float zone growth. So far no other growth methods have been seriously considered. The only exception to this is PV, where the industry has been forced to look for cheaper alternatives. Indeed, cast multicrystalline silicon has dominated the PV industry for decades. Ever increasing requirements towards higher efficiencies have led to the development of new and innovative crystal growth technologies that provide better crystal quality and improved electrical properties. Currently the most promising technology is based on a simple and low-cost casting method, 15 % lower manufacturing cost compared to Cz-Si [1], resulting in high quality single crystalline silicon (cast mono-Si), also known as monolike, quasimono or mono^2 silicon [2, 3, 4, 5]. Obviously the quality of cast mono-Si is not high enough for IC or high-purity detectors, but for instance, MEMS technology could find it as an attractive alternative to conventional Cz-Si, especially in applications where lower substrate cost could bring a significant competitive edge, such as disposable applications [6, 7].

Cast mono-Si is fabricated using a directional solidification method combined with a single crystalline seed layer placed on the bottom of the crucible [5]. By properly tuning the growth parameters, one can grow square single crystalline ingots with dimensions of e.g. 1340 mm × 1340 mm × 500 mm (Gen8) [8]. Thus, in principle, there is no wafer size limitation for cast mono-Si and cutting wafers with different sizes is straightforward. By nature the method produces square wafers and typically, in PV industry, one Gen8 ingot is cut to approximately 69 000 pcs of 8 inch square wafers. In the short term the square shape can be considered as a possible drawback as the existing fabrication facilities are mainly for round wafers. In the long term, it could, however, turn out to be beneficial as more chips would fit on a single wafer. The growth method brings also other benefits, especially regarding crystal orientation that often plays an important role in MEMS. While the seed layer can be of different orientation, the wafers can also be cut perpendicular to the growth direction. Additional benefit of cast mono-Si is the low amount of oxygen impurities since oxygen is known to cause unwanted etch pits during wet etching [9]. For the same reason, cast mono-Si is also free of troublesome thermal donors [10]. With all the possible benefits listed above the material should have potential beyond photovoltaics as well.

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This work takes the first step in studying the applicability of cast mono-Si for microfabrication processing steps needed in MEMS and NEMS device fabrication. Here we target directly sub-micron resolution and thus select relatively challenging patterning technology, namely focused-ion-beam (FIB) lithography [11, 12], which is resist-free, flexible, relatively fast and suitable for highly corrugated surfaces [13, 14], and thus an ideal method for prototyping new technologies e.g. as compared to more commonly used electron-beam lithography. If the results turn out to be successful with such a demanding process step, also less complicated microfabrication processes should be viable with cast mono-Si. In the experiments we use commercially available cast mono-Si wafers and study the masking and etching properties of the wafers via both dry and wet etching. We search the optimal processing parameters for successful FIB mask formation, characterize the resulting structures and compare the outcome with Cz-Si. Our main goal is to give an overview of the potential of cast mono-Si for MEMS processing and point out the possible bottlenecks that prevent wider utilization of the material. Ideally this study provides a good starting point for further studies that would allow fabrication of complete devices.

II. Experimental

Fig. 1 (a) presents the process flow used in the experiments. The starting wafers were commercial PV-grade 156 × 156 mm^2 cast mono-Si with the resistivity of approximately 3 Ωcm, thickness of 180 µm and <100> orientation. After diamond-wire sawing the wafers from the ingot, the wafer surfaces had experienced the PV industry-standard alkaline-based saw damage etching [15]. Such etching results in a slightly rough surface as seen in the scanning electron microscope (SEM) image in Fig. 1 (b). While in solar cells this is a sufficient starting point for cell processing, IC and MEMS industry typically make additional relatively expensive polishing steps before the actual device processing. Similarly to Cz-Si, cast mono-Si wafers could also be polished with standard methods. Here these polishing steps were omitted on purpose to study the applicability of cast mono-Si wafers that are already now commercially available.

The first processing step was to clean the wafers in an RCA-1 solution, which was followed by a brief dip in a dilute hydrofluoric acid (HF) solution. In order to create a mask with sub-micron resolution for both dry and wet etching steps, we used the local Ga^+ FIB implantation method [11, 12, 16, 17]. The FIB implantation was performed using a Helios Nanolab 600 dual-beam system from FEI Company using acceleration voltage of 30 kV. The Ga^+ beam was generated from a liquid metal ion source with the beam current varying between 1.5 pA and 20 nA. The dwell time was varied between 50 ns and 4.6 ms resulting in Ga^+ doses between 1×10^{14} and 5×10^{17} cm^{-2}. However, since the doses below 5×10^{15} cm^{-2} did not seem to provide clear masking, we omitted them in this study.

As shown in Fig. 1 (a), we had three different mask designs. To determine the obtainable structure height and the selectivity

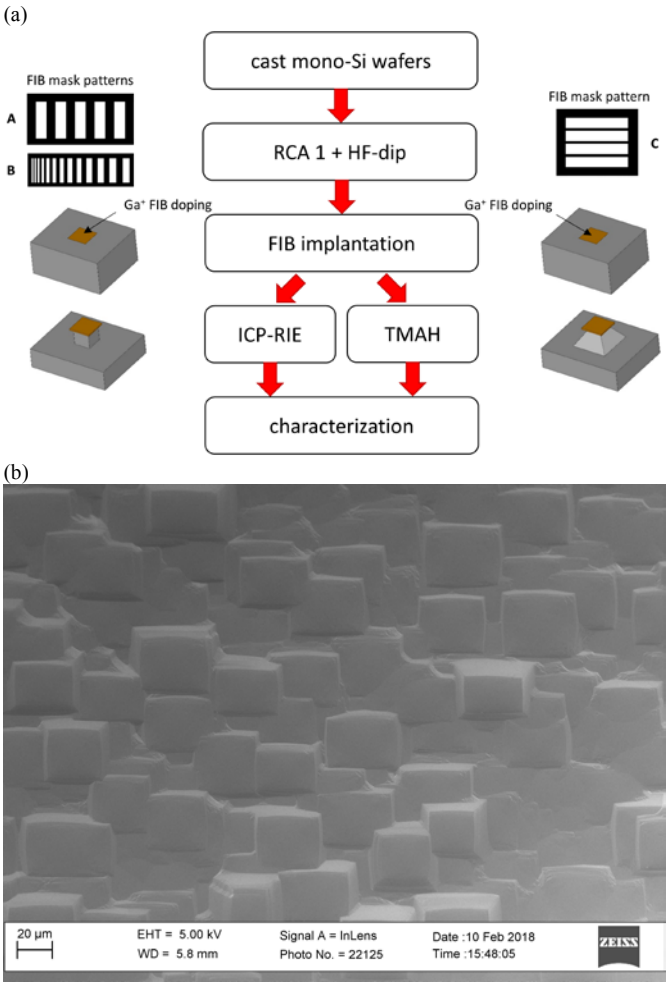


Fig. 1. (a) The processing steps used in the experiments. The dimensions of the different mask designs A, B and C are given in the text. (b) SEM image of the commercial PV-grade cast mono-Si wafer surface.

between the FIB Ga^+ mask and cast mono-Si substrate, design A with 4 µm wide and 20 µm long lines with a spacing of 8 µm was used. For spatial resolution tests, we selected design B with narrower lines with linewidths starting from 31 nm and increasing with an increment of 10 pixels (10 × 3.1 nm, determined by the Ga^+ beam) up to 589 nm width. Finally, design C with rectangles with dimensions of 1 µm × 15 µm was used for studying the applicability of cast mono-Si substrate for wet etching.

FIB implantation was followed by either dry or wet etching. Here dry etching with inductively coupled plasma reactive ion etching (ICP-RIE) was chosen as the main method to study the FIB masking capability in cast mono-Si since the etch rate in ICP-RIE can be made independent on the crystal orientation and it enables nanoscale structures. The dry etching was carried out in an Oxford Instrument's PlasmaLab System 100 cryogenic inductively coupled plasma reactive ion etcher (ICP-RIE) at the temperature of -120 °C. High density SF_6/O_2 plasma was generated by an ICP source at 13.56 MHz and ion energies were controlled separately with capacitively coupled plasma (CCP) operating also at 13.56 MHz. The SF_6/O_2 gas flow was 40/6.3 sccm. An ICP power of 800 W combined with

a CCP power of 3 W was used. The etching times were varied from 10 s to 3.5 minutes. Additionally, we studied the applicability of cast mono-Si to more commonly used wet etching that provides crystal plane dependent anisotropic etching. Prior to the etching, the native oxide was removed in a dilute HF solution. The etching was carried out in a 25% TMAH solution at 80 °C. TMAH was selected as it is known to be CMOS compatible.

The etched structures were characterized with a Zeiss Supra 40 scanning electron microscope (SEM). Special emphasis was put on the height of the structures. This was done in order to i) find the lowest Ga^+ dose needed for reliable pattern transfer, ii) define the threshold Ga^+ dose for mask resistivity saturation, and iii) determine the mask tolerance against the etching time as a function of Ga^+ dose. Additionally, SEM images were used to determine the obtainable linewidth and its linearity. Finally, the results were compared with standard Cz-Si wafers.

III. Results and Discussion

A. Dry etching

First we determine the needed Ga^+ dose in cast mono-Si for reliable pattern transfer by ICP-RIE, and the resulting structure heights, and compare them with Cz-Si. Fig. 2 shows the height of the etched structures in cast mono-Si with various time intervals (a) and with various Ga^+ doses (b) using the mask design A shown in Fig. 1 (a). Additionally, in Fig. 2 (b) the obtained structure height is compared with the corresponding data reported earlier for Cz-Si using a mask of 150 × 150 μm^2 squares [16, 18].

As mentioned earlier, among the tested doses, 5×10^{15} ions cm^{-2} is the lowest dose to provide clear masking in cast mono-Si as with lower doses no clear structures remained on the substrates even with the lowest selected times. On the other hand, we see that the masking effect saturates quickly with the increased Ga^+ dose. More specifically, Ga^+ doses of 1×10^{16} ions cm^{-2} or higher no longer affect the achievable structure height. However, it is worth to note that Ga^+ doses higher than 1×10^{17} ions cm^{-2} result in laterally distorted mask shapes. This was expected as higher doses often result in sputtering and re-deposition [19, 20]. Fig. 2 (a) shows also that the structure height increases linearly as a function of etching time demonstrating steady masking capability. Finally, after 3 minutes of etching, the structure height no longer increases in any of the samples indicating the removal of the protecting Ga^+ mask. If we consider that the mask thickness is approximately 50 nm as in [16, 18], we can roughly estimate the etch selectivity to be 160:1.

Fig. 2 (b) further confirms that the cast mono-Si pattern height follows the same natural trends as in Cz-Si: higher dose and longer etching time provide a higher mask resistivity and structure height, respectively, until reaching the maximum masking capability. Secondly, the threshold dose for the masking seems to be in the same range for both materials. Thirdly, with the corresponding doses and etching times, the

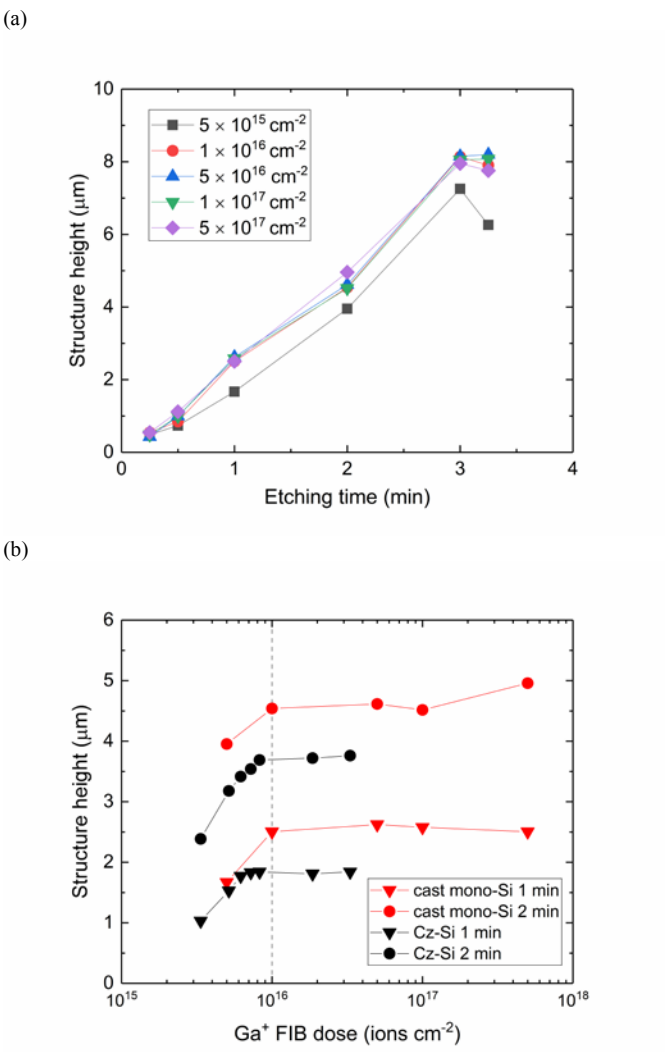


Fig. 2. (a) Obtained silicon structure heights with various Ga^+ doses and with various time intervals using mask design A with dimensions of 4 μm × 20 μm. (b) The comparison of obtained structure height in cast mono-Si with corresponding data reported earlier for Cz-Si [16, 18].

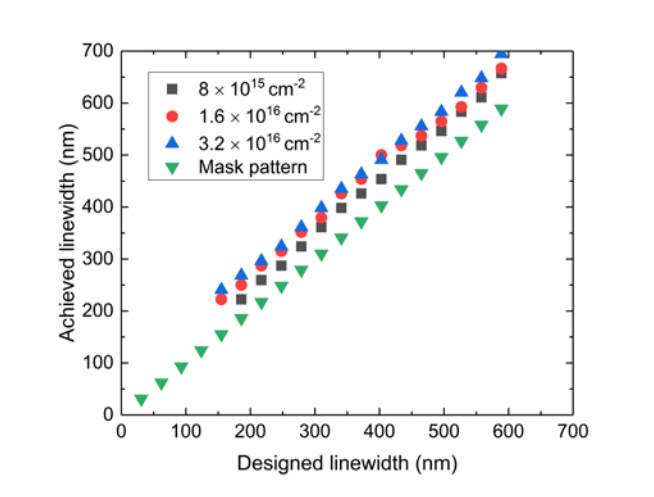
obtained structure height is somewhat higher with cast mono-Si. This suggests that cast mono-Si could provide structures with higher aspect ratios. The reason for faster etching rate requires further studies but could be related to the difference in the amount of various types of crystal defects. Finally, the slope in the curves at low Ga^+ doses (Fig. 2 (b)) suggests that also in cast mono-Si it is possible to control the structure height by varying the Ga^+ dose, which enables three dimensional shapes with only a single etching step.

In order to determine the achievable linewidth and linearity in cast mono-Si we used mask design B and fabricated a sequence of lines with increasing linewidths and with different Ga^+ doses. The results presented in Fig. 3 (a) show a good linearity with all the tested doses indicating that cast mono-Si substrate can be used for successful silicon nanolithography, even when the surface is not polished. The smallest achieved linewidth, i.e. the width of the narrowest pattern standing as an isolated line, was 222 nm with a 36 nm deviation from the designed mask with the lowest used Ga^+ dose. The higher Ga^+

dose was seen to widen the achievable structure width. The achieved structures were on average 50 nm, 75 nm and 90 nm wider compared to the designed mask with Ga^+ doses of 8×10^{15}, 1.6×10^{16} and 3.2×10^{16} ions cm^{-2}, respectively. In addition to surface roughness, such widening could be partly related to the possibly larger spatial distribution of implanted Ga^+ ions in cast mono-Si due to slightly different crystal quality and higher amount of crystal defects e.g. oxygen and dislocation concentrations.

A closer look on the SEM image in Fig. 3 (b) indicates that narrower linewidths were achieved with the Ga^+ dose of 8×10^{15} ions cm^{-2} but the mask did not sustain due to undercutting during etching. Nevertheless, these preliminary results indicate that with proper process parameter optimization, and especially after surface polishing, linewidths comparable to Cz-Si (54 nm [16]) should be obtained. However, possibly larger underetching in cast mono-Si needs to be considered.

(a)



(b)

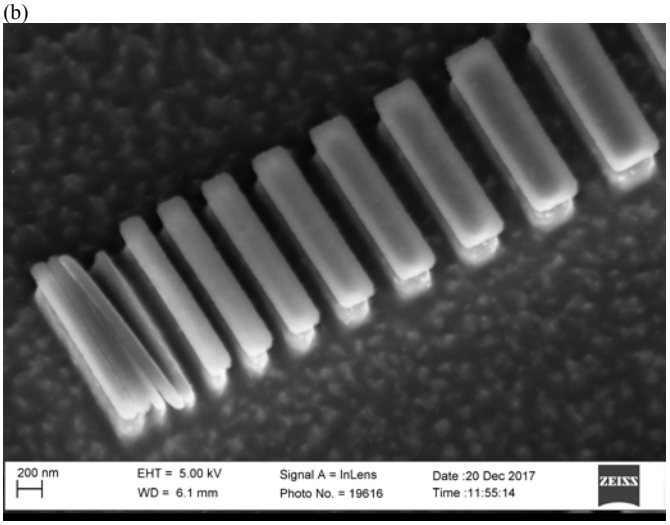


Fig. 3. (a) Measured linewidths on cast mono-Si substrate with various Ga^+ doses. (b) SEM image of the etched silicon line array with Ga^+ dose of 8×10^{15} ions cm^{-2} (mask design B).

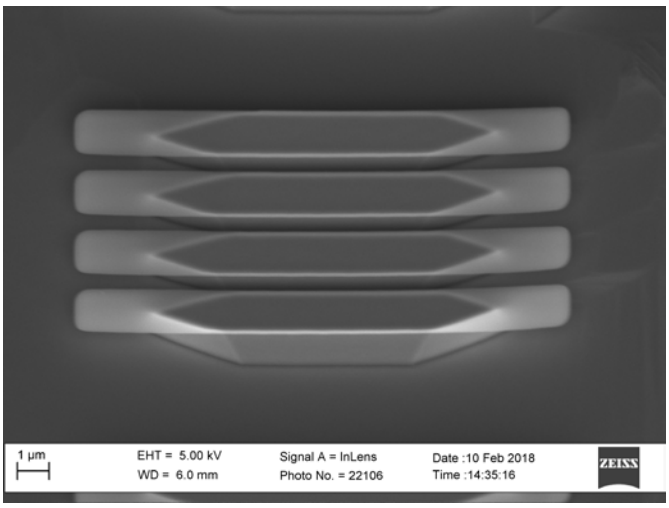


Fig. 4. Silicon line array fabricated with anisotropic wet etching using Ga^+ dose of 3.2×10^{16} ions cm^{-2} (mask design C).

B. Wet etching

Fig. 4 shows an example of the silicon line array fabricated with FIB masking using mask design C and anisotropic wet etching on cast mono-Si wafer. The dimensions of mask design C were 1 µm × 15 µm and the tested Ga^+ doses were 8×10^{15}, 1.6×10^{16} and 3.2×10^{16} ions cm^{-2}. Firstly, with all doses a successful and a robust mask was obtained demonstrating that the FIB masking capability extends also to wet etching in cast mono-Si. Secondly, the resulting structure shows that in cast mono-Si the wet etching rate depends on the orientation of the exposed crystal planes resulting in similar etching profile as in Cz-Si. This indicates that the degree of crystal regularity in cast mono-Si is high enough for successful anisotropic wet etching.

IV. Conclusion

In this paper we have made the first steps in studying the applicability of cast monocrystalline silicon for MEMS and NEMS applications. More specifically, we focused on the nanostructure formation using FIB rapid prototyping. We found that the lowest Ga^+ dose needed for reliable pattern transfer is 5×10^{15} ions cm^{-2} and the threshold Ga^+ dose for mask resistivity saturation is 1×10^{16} ions cm^{-2}. With a 50 nm mask thickness the obtained structure height was approximately 8 µm and thus the selectivity provided by the Ga^+ mask was 160:1 with rough surfaces. Furthermore, submicron linewidths with high linearity were achieved. Finally, we demonstrated that cast mono-Si has a high enough degree of crystallinity for successful anisotropic wet etching. The results demonstrate that cast mono-Si behaves similar to Cz-Si showing its potential as a cheap alternative. While further studies are required to verify the mechanical properties of cast mono-Si for specific MEMS devices, it is particularly attractive substrate e.g. for disposable applications.

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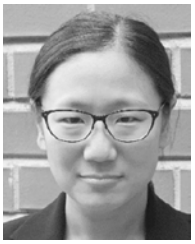

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