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A Blocker-Tolerant Two-Stage Harmonic-Rejection RF Front-End

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Abstract — SAW-less wideband receivers need to operate linearly in the presence of strong out-of-band blockers. In this paper, we introduce a blocker tolerant harmonic rejection RF front-end which is able to suppress blockers present at the local oscillator harmonics. The suppression is achieved by applying harmonic rejection in two stages, such that the first harmonic rejection already occurs at the output of LNA. The proposed front-end achieves this harmonic rejection with simpler 6-phase LO clocking and reduced number of base-band signal paths compared to 8-phase HR architectures. Further, the proposed design does not require any precise gain coefficients and implementing the harmonic rejection in two stages makes it more mismatch tolerant. In addition, near-band blocker linearity is improved by implementing a third order base-band feedback response which acts in conjunction with N-path filtering. Implemented in a 28nm FDSOI process, the front-end demonstrate 18-37dB harmonic rejection from the first stage and around 46-53dB of harmonic rejection from the second stage with a state-of-the-art blocker compression point of 2.5dBm for a third harmonic blocker and a near-band blocker compression point of -6.5dBm.

Keywords - Harmonic rejection, blocker tolerance.

I. INTRODUCTION

The emergence of multiple radio access standards have arisen the demand for wideband receivers which should be able to operate on multiple frequency bands. Such a receiver will need to perform in presence of strong out-of-band (OB) blockers which potentially saturate the receiver. Traditionally, these OB blockers have been attenuated through off-chip surface acoustic wave (SAW) filters which are not suitable for wideband receiver scenario due to their non-tunability. What is needed is an on-chip tunable filtering alternative for blocker suppression.

One such widely implemented on-chip filtering technique is N-path filtering, which offers moderate Q factor with a wide tuning range [1]. However, one of the shortcomings of original N-path filtering concept is its inability to suppress blockers at harmonics of the local-oscillator (LO) frequency. Various works [2], [3], [4], [5] have proposed harmonic rejecting N-path filtering. However, in order to achieve higher harmonic rejection (HR), these techniques implement a higher number of paths together with the requirement of precise gain coefficients. Higher number of paths, inevitably lead to a complicated design with increased area and power consumption, while precise gain coefficients suffer from implementation inaccuracies. In addition, HR is usually implemented later in the receiver chain when gain has already been applied [3], [6]. Blocker at LO harmonics will thus already saturate the first stages before the HR is even takes place.

Some recent works [4], [5] have proposed HR at the output of first gain stage to improve receiver linearity for blockers at LO harmonics. Though these techniques achieve promising linearity improvements for blockers at LO harmonics, they still implement a higher number of N-paths with the requirement of implementing precise gain coefficients.

In this paper, we propose a two-stage harmonic rejection RF front-end which achieves HR at the output of the first gain stage. This helps to improve front-end linearity for blockers at LO harmonics. The proposed architecture is simple as it utilizes a six-phase LO clock, compared with other implemented works which use eight phases or more [4], [5]. In addition, the proposed architecture does not require any precisely tuned gain coefficients while at the same time implementing the HR in two stages makes it more mismatch tolerant. We also propose a third-order base-band (BB) response together with an N-path filtering, which helps to greatly suppress near-band blockers.

The organization of this paper is as follows: Section II details the proposed two stage HR front-end while Section III elaborate the circuit design and measured results. Section IV ends in conclusion.

II. PROPOSED ARCHITECTURE

The proposed two-stage harmonic-rejection front-end is presented in Fig. 1. The architecture implements three base-band downconversion paths each of which is 60° degrees phase shifted from the adjacent path. This decreases the number of BB paths by one as compared to 8-phase N-path downconversion [4], [5], [2]. From the three 60° degree phase shifted BB outputs, conventional I and Q outputs can easily be derived in the digital domain after an ADC.

The first stage of HR rejection is implemented by two parallel low-noise amplifiers (LNA) together with six differential passive mixers clocked by six non-overlapping LO phases. The need for two LNA's and six mixers arise to create HR at the LNA output without using overlapping LO clocks which would otherwise decrease the LNA gain. The LO clocking for the passive mixers is presented in Fig. 2 which can be altered to either the 6-phase HR LO clock (blue),



Fig. 1. Block diagram of proposed two stage harmonic rejection front-end.

or conventional 6-phase clock for lower noise contribution front-end (grey). Conventional LO clock is identical to having one equivalent LNA and three mixers while in the HR clocking arrangement, the functionality can be explained as follows: During LO phases 1p and 2p, LNA1 and LNA2 get alternatively connected to BB1. In phase 3p and 3n neither LNA1 nor LNA2 are connected while in phases 1n and 2n, LNA1 and LNA2 get connected to BB1 with opposite polarity creating an effective LO at the input of the BB1 as shown in Fig. 2. Fourier analysis of HR LO waveform reveals ideally no third harmonic and therefore, creates third harmonic rejection with lower number of clock phases. Further, as the HR occurs exactly where the gain is applied, i.e. at the LNA output, front-end linearity in presence of blockers at the 3rd LO harmonic also improves. However, complete elimination of third harmonic is not possible due to device mismatches and LO non-idealities. Therefore, to improve the HR further second HR stage is required.

The second stage makes the effective downconverted signal more closely resemble a sine wave. To do this, we implement cross-coupled BB stages between three BB paths as shown in Fig. 1. This produces signals (A-C)/2, (B+A)/2 and (C+B)/2, where A, B and C are the signal outputs from the first BB stages of three parallel BB paths. The generated signals (A-C)/2, (B+A)/2 and (C+B)/2 resemble a sine wave more closely and simple Fourier analysis shows increased harmonic rejection.

In order to improve the near-band blocker attenuation we propose a third-order BB filtering stage as shown in Fig. 1. The response is implemented with a third-order feedback impedance, where the equivalent inductance has been implemented with gyrator transconductors for on-chip fabrication. The created response works in conjunction with N-path filtering to attain a sharp third-order band-pass response at LNA output, consequently, improving the near-band blocker linearity.

III. CIRCUIT DESIGN AND MEASUREMENTS

The proposed front-end was fabricated in a 28nm FDSOI technology for an operating frequency of 0.7-2GHz. The front-end was part of complete receiver, with $\Delta\Sigma$ ADC and digital processing. The chip photograph of complete receiver



Fig. 2. Conceptual representation of proposed two stage HR with the generated effective LO at each HR stage.



Fig. 3. NF and the first stage HR of the proposed front-end, for HR LO clocking (black) and conventional LO clocking (grey).

IC is presented in Fig. 7, in which the front-end part together with LO generator occupies an active area of 0.65mm². In order to measure the performance of the first HR stage, a test signal from the output of the first BB amplifier was routed outside the IC. RF performance was then measured by buffering this signal with an external operational amplifier and observing response at output measurement point as shown in Fig. 1.

On the circuit level, the implemented LNA's consist of push-pull common-gate common-source amplifiers with capacitive feedback for impedance matching, while the passive mixers were implemented with large aspect ratio transistors to ensure small switch resistance. The BB integrators were implemented with a dynamically-biased differential pair where the transconductance of the first BB stage was designed to be eight times higher than transconductance of later stage for lower noise contribution. The capacitors C_{NP} provide additional blocker rejection at higher frequency offsets where the bandwidth of the first BB stage is not sufficient for a reasonable feedback response. For LO generation, an external signal at $3f_{LO}$ was provided to LO chain which was then divided by three to create six non-overlapping LO clocks with 16.7% dutycycle, and finally routed to passive mixers through inverter buffers.



Fig. 4. BB filtering response, OB IIP3 and 1dB compression point vs. BB frequency for an $f_{LO} = 1.5$ GHz. Third order BB filtering response gets upconverted to LNA output nodes with N-path filtering consequently helping to suppress near-band blockers.



Fig. 5. OB IIP3 and P1dB versus front-end operating frequency. The blocker is placed at $f_{\rm LO}{+}100 MHz$

Fig. 3 shows the measured NF and HR of the first stage across the operating frequency range. HR in the range of 18 to 37 dB is observed for HR LO clock. One of the consequence of the HR LO clock is noise circulation from one base-band path to other. This happens because a single LNA is connected to two base-band paths at all time instances, resulting in creation of the noise circulation path and a higher NF front-end. To validate the noise circulation, we have also implemented an LO clocking mode where each BB branch is only connected to one LNA at a time, thus eliminating the noise circulation path. With this LO arrangement around 3dB improvement in front-end NF is observed in measurements. The increase of NF at high frequencies was due to non-optimal layout design of LO chain which resulted in overlapping of LO signals at higher frequencies resulting in increased NF. A careful re-design of LO chain should reduce this increase of NF.

In Fig. 4, the third order BB filtering response, OB IIP3 and P1dB compression points are plotted versus BB frequency offset. One can observe third order filtering near the BB bandwidth of 10MHz. This third order response is upconverted to LNA output nodes with N-path filtering, consequently, helping to suppress near-band blockers. For example, the measured P1dB compression point for a near-band blocker located at 40MHz offset from f_{LO} is -6.5dBm which is just 1.5dB less than P1dB measured at a 100MHz offset. To observe the front-end linearity behavior across the operating frequency Fig. 5 shows the measured OB IIP3 and P1dB versus frequency for a blocker at 100MHz offset from LO.

	This work	[4]	[5]	[6]	[7]
Carrier Frequency (GHz)	0.7-2	0.2-1	0.1-2.4	0.7-1.4	0.5-3
HR at first gain stage (dB)	18-37	20	52-54	NA	35
Second stage HR ² (dB)	46-53	51-52	NA	40-67	NA
Architecture	LNA first	LNA first	Mixer first	LNA first	LNTA first
N-path phases	6-phase	8-phase	8-phase	8-phase	8-phase
Blocker input P1dB (dBm)	-1 to -5@10f _{BW}	-2.4@10f _{BW}	-6 to 2.5@27f _{BW}	-8.5 to 10@10f _{BW}	-
Blocker input P1dB@3fLO (dBm)	2.5@10f _{BW}	-2.8	-8	NR	NR
Near band blocker P1dB (dBm)	-6.5@4f _{BW}	NR	NR	NR	-22 to -4@4f(LO
Noise Figure (dB)	5-11	5.4-6	1.7	1.5-8	3.8-4.7
OB IIP3 (dBm)	8-11@10f _{BW}	9@10f _{BW}	10	1-20.5@10f _{BW}	-20 to -4.8@4f _{BW}
Gain (dB)	36	36	NR	20.8-36.8	50
BB bandwidth (f _{BW}) (MHz)	10	2	0.2-3	10	10
Power (mW) @ Supply voltage (V)	54@1	26-32@1.2, 2.5	36.8-62.4@1	52@ 0.8, 1, 1.2	76-168@NR ⁽¹
Process	28nm FDSOI	65nm	28nm	65nm	65nm

Table 1. Performance summary and comparison

NR: not reported, NA: not applicable. 1) signal path 2) 1st and 2nd stage combined HR.



Fig. 6. Measured signal gain under the presence of strong blocker at $3f_{LO}$. For a blocker at $3f_{LO}$ +100MHz, blocker P1dB of 2.5dBm is observed.



Fig. 7. Chip photograph of the proposed harmonic rejection receiver.

For observing front-end linearity in the presence of blockers at $3f_{LO}$, linearity was measured with three offset frequencies, 100MHz, 40MHz and 4MHz. These three offsets represents downconversion of the blocker to out-of-band, near-band, and in-band reception frequencies. The measurement was performed by sweeping the blocker power and determining the P1dB point of the receiver. We observe P1dB points of -7, 1 and 2.5 respectively as shown in Fig. 6 achieving state-of-the-art results [4], [5].

IV. CONCLUSION

Blocker tolerance is one of the key specifications for SAW-less wideband receivers. In this paper, we have proposed a blocker tolerant harmonic rejection front-end which is able to efficiently suppress blockers present at LO harmonics together with suppression of near-band blockers. This is achieved by implementing HR in two stages: Output of the LNA and in the second BB stage. Further, a third order BB impedance is implemented which acts in conjunction with N-path filtering for near-band blocker attenuation. The proposed architecture uses a lower number of LO phases and BB paths compared to 8-phase HR architectures and achieves HR without implementation of precise gain coefficients. Measured results from a fabricated prototype implemented in 28nm FDSOI technology demonstrate 18-37dB HR from the first stage and around 46-53dB of HR from second stage with a near-band blocker compression point of -6.5dBm and an impressive BCP of 2.5dBm for third harmonic blocker.

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