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A Wideband IF Receiver Module for Flexibly Scalable mmWave Beamforming Combining and Interference Cancellation

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Abstract— Large-scale phased arrays need to combine weighted signals from multiple sub-arrays either in analog or in digital domain. Sub-arrays are preferably implemented modularly with integrated circuits placed next to the associated antennas. In order to enable flexible and scalable combining networks of several mmWave sub-arrays, this paper presents a wideband receiver module that provides the cartesian combining of beamforming weights for one sub-array at IF. Furthermore, it allows interference cancellation between sub-arrays or combining multiple sub-arrays. It also provides filtering before ADCs to support current and foreseeable 5G channel bandwidths up to 800MHz. The receiver is operating at 2-4GHz IF frequency range and has more than 400MHz baseband bandwidth, a noise-figure of 5.5dB, -6dBm 1dB compression point and +3dBm in-band IIP3. In addition, over-the-air measurements are performed, showing 26dB of interference cancellation between the sub-arrays. The prototype is implemented using 45nm CMOS PDSOI.

Keywords— phased array, beamforming, phase shifter, complex multiplication, inter-beam interference cancellation

I. INTRODUCTION

Fifth generation (5G) communication utilizes large scale phased arrays to enhance the signal-to-noise ratio (SNR), link budget and spatial selectivity at millimeter wave (mmWave) frequencies [1]. The silicon implementation of the associated beamforming transceivers supporting arrays of e.g. 32, 64 or even higher number of elements requires large chip area and increases system on chip complexity. Therefore, a scalable solution is preferred. Some earlier approaches for scalable phased arrays use heterodyne down-conversion from mmWave to IF and perform the beamforming at baseband (BB) to avoid the complexity and power penalty of mmWave quadrature LO-generation [2]. Local oscillator (LO) phase shifting for scalable arrays increase the buffering and LO routing at mmWave resulting in significant area and high-power consumption [3]. In [4] and [5], I/Q is generated separately at mmW or at very high IF for each element which is less accurate and requires dedicated I/Q signal generation which increase the area of chip.

This work exploits the cartesian combining architecture in [2] for a scalable solution and proposes a modular sub-array architecture combining signals of mmWave subarray antenna elements. Each antenna signal needs complex weighting, but this function is distributed between mmWave and IF as in [2], where only the variable gain is required at mmWave, while the phase shift of 90° to realize the cartesian combining is implemented in IF-RX exploiting quadrature mixing (see fig 1). Hence, only one mmWave LO per sub-array is needed and no different phases.

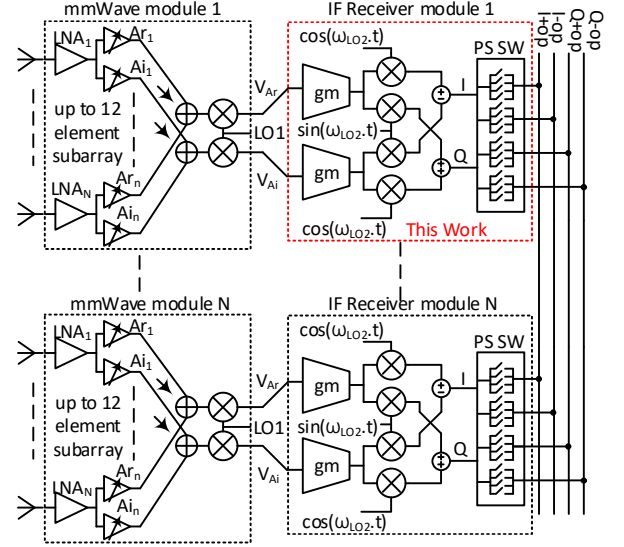


Fig. 1. A dual-stage mmWave phased array architecture for a large array. This work describes the implemented IF receiver module.

Moreover, a modular approach enables combining multiple sub-arrays implemented on separate IC's into one BB output as depicted in Fig. 1. It also offers the flexibility of implementing multiple parallel IF-RX stages due to voltage output of mmWave module. Those can be used for interference cancellation between multiple data streams. However, cancellation requires additional weights which are provided by using the IF-RX as vector modulator (VM). In addition, low noise figure (NF) and gain provided by the IF-Rx module allow substantial wiring losses in large scale arrays without degrading system performance.

Section II describes the receiver architecture while Section III explains the details of the IC prototype. Experimental results are given in Section IV followed by conclusions in Section V.

II. RECEIVER ARCHITECTURE

The proposed IF-RX receiver utilizes a cartesian combining architecture based on work in [7] for a direct conversion receiver and extended for a mmWave beamformer in [2]. In this paper, we convert down to a fixed IF between 2 to 4 GHz. The selection of IF depends on the number of sub-array elements and maximum steering angle, such that, the IF phase shifter can operate over the wide bandwidth and the beam squinting error remains within the 3dB-beamwidth. The maximum number of antenna elements in a sub-array can be estimated as [6]

$$BW = \frac{2f_o}{N \sin(\theta_o)} \quad (1)$$

where BW is the fractional bandwidth of phase shifter, f_o is the center frequency, N is the number of elements in a subarray and θ_o is the maximum steering angle. 500MHz bandwidth, $\pm 60^\circ$ steering angle and 2.5GHz center frequency results in 12 antenna elements per sub-array.

The mmWave module variable gain amplifier (VGA) weights serve to optimize the SNR of the receiver and realize spatial filtering. The amplitude weighting by the mmWave VGAs with weights A_{r1} and A_{i1} after mixing with a sine and cosine functions result in voltage output V_{Ar} and V_{Ai} as shown in Fig. 1. Note that these are voltage outputs, which provides the flexibility to realize multiple parallel IF-RX stages. This can functionally be exploited in different ways, e.g. to realize multiple data streams, while also interference cancellation between different subarray data streams is possible. Such interference cancellation requires accurate weighing, which may be difficult to achieve at mmWave, but much easier at a few GHz IF. Our design targets to achieve 26dB rejection, which is possible with 5-bit phase shifter [8].

A. IF-RX Architecture

The IF-Rx architecture is based on dividing the receiver into parallel slices and utilized as a vector modulator [9]. Instead of exploiting charge sharing on a capacitor as in [9], that results in averaging, cartesian combining is implemented by true current summing into a virtual ground node provided by a transimpedance amplifier (TIA) as shown in Fig. 2. This can provide more gain over a wider bandwidth. The VM consists of sliced gm cells, followed by a reconfigurable switching matrix (PS SW) that adds current contributions of slices at the virtual ground node of the TIA. This TIA provides both baseband I-V conversion and baseband low-pass filtering. The amplitude and phase constellation points of VM depend on the number of slices. For M slices the constellation consists of $M+1$ by $M+1$ elements and contains $\sim 2\pi(M/2-1)$ amplitude points in the largest circle that can be drawn inside the boundaries of the constellation. This IF-Rx architecture provides a low NF and hence allows good system NF even for moderate or low gain mmWave sub-arrays with long and lossy wiring.

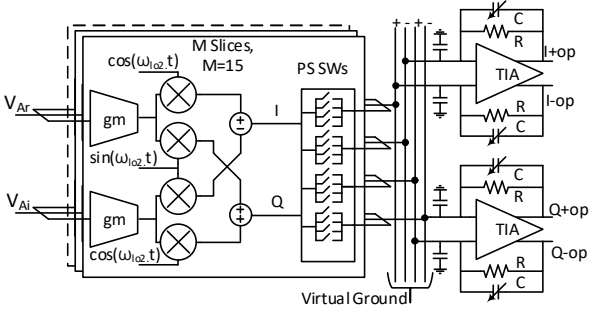


Fig. 2. IF receiver architecture. The current combining at output is done by baseband transimpedance amplifier (BB-TIA).

III. IC DESIGN

The implementation of the IF-Rx is realized by dividing the input into 15 binary weighted, parallel slices where each slice acts as an independent vector component in the VM. Each slice consists of a differential transconductor (gm), a double-balanced quadrature passive mixer for each differential V_{Ar} and V_{Ai} inputs and a reconfigurable switch at baseband. The four-phase 25% duty cycle current mixer converts the RF transconductor current to zero-IF, performs

the cartesian combining for V_{Ar} and V_{Ai} signals and provides the differential I and Q signals. The reconfigurable switches

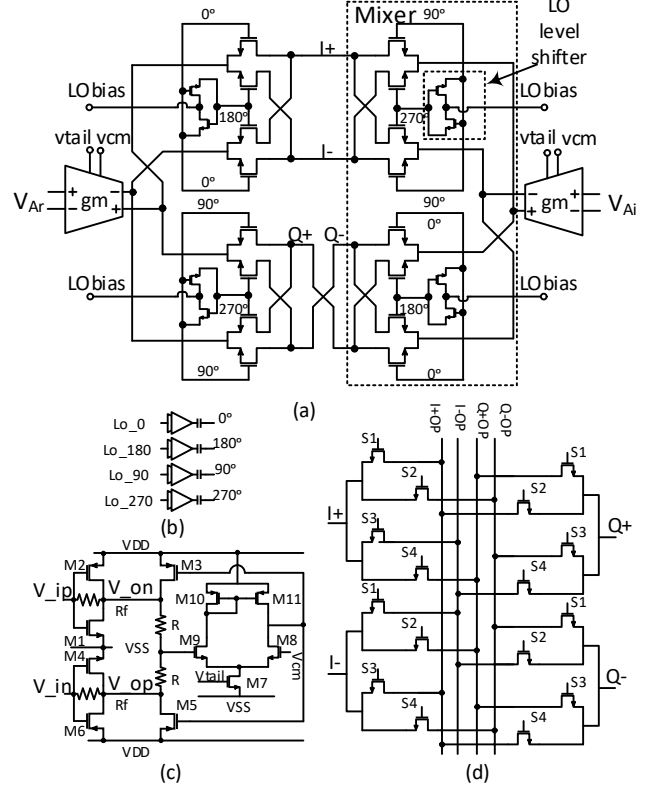


Fig. 3. (a) Cartesian combining with passive mixer, (b) LO buffer, (c) Transconductor stage, (d) reconfigurable switches.

at baseband rotate the IQ signals by 0° , 90° , 180° or 270° depending on the phase constellation point.

A. Transconductor Stage

A pseudo-differential transconductor pair (gm) acts as a low noise amplifier (LNA) and provides the input matching at the RF port. Schematic of the LNA is shown in Fig. 3(c). In the inverter, both NMOS and PMOS contribute to the total transconductance and resistive feedback R_f provides low noise figure and low impedance match due to Miller effect [9]. The gm stage is DC-coupled with mixer switches to avoid the large AC-coupling capacitor in each slice. To avoid the DC operating point mismatch, a common-mode feedback (CMFB) stage is added to each differential pair and controlled independently through the current DAC. The PMOS transistors M3 and M5 are controlled by CMFB and they feed the current at the output node of the gm stage depending on the common mode and bias input and output of the gm stage. All devices in the gm stage use $7\mu\text{m}/40\text{nm}$ transistors including feedback transistor with $3.5\text{k}\Omega$ feedback resistor R_f . Circuit provides gm of 4mS in both PMOS and NMOS.

B. Quadrature Downconversion

The cartesian combining of the weighted inputs V_{Ar} and V_{Ai} and down-conversion is realized with double-balanced quadrature passive mixer as shown in Fig. 3 (a). The mixer consumes no static power and has theoretical minimum conversion loss of 0.9dB for 25% duty cycle with additional 4.4dB loss of cartesian combining. The gate terminals (LObias), sources (biased from gm side) and drains (biased from BB-TIA side) of the mixer switches are biased to half

of the supply and shift the level of the LO locally to fully switch ON and OFF the mixer switches (Fig. 3 (a) and (b)).

A four-phase, 25% duty cycle clock is required to drive the mixer switches in the VM. The clock generation is done on-chip by current mode logic (CML) divider. It divides the external reference clock (LO+ and LO-) by 2 and generates four phases with 50% duty cycle. The 25% duty cycle clock is generated by AND gate logic.

The amplitude and phase balance of the reference clock is of importance as the inaccuracy is transferred directly to IQ imbalance. Therefore, reference clock is first amplified through self-biased differential amplifier to reduce the common mode. In the simulation, the IQ imbalance is checked at the input of each slice and slice-to-slice. The rms phase imbalance is found to be less than 1° .

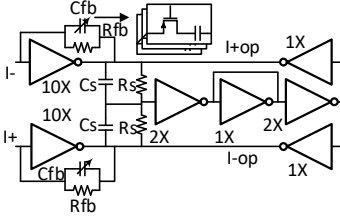


Fig. 4. Baseband TIA stage.

The IQ signals generated in the mixer pair are further processed by reconfigurable switches. The switches are driven by static control signals and allow to pick one of the four mixer phases, which effectively rotate the phase by 0° , 90° , 180° , or 270° (Fig. 3 (d)).

All reconfigurable switches are then connected to the BB-TIA input, which is filtered by the switch-RC path. The inverter-based BB-TIA is implemented as in Fig. 4 to provide the better trade-off between power and noise performance as compared to single stage Op-amp based BB-TIA. The BB-TIA is self-biased and has common-mode at the output to suppress the offset and even-order distortion. The feedback of the BB-TIA contains tuneable capacitors for bandwidth control.

IV. MEASUREMENT RESULTS

A. IF-RX Measurement

IF-RX is implemented on 45nm PDSOI. The chip photograph is shown in Fig. 5. The IC has active area of 0.26mm^2 including clock generation and consumes 104mW power from 1V supply and 18mW from 1.5V supply for buffers to drive static switches. IF-RX measurements are performed using external baluns at RF, baseband and LO side on printed circuit board (PCB). The IF-RX provides maximum $\sim 10\text{dB}$ of gain as shown in RF/IF response in Fig. 6 (a) and more than 400MHz BB bandwidth (Fig. 6 (b)). Circuit achieves minimum 5.5dB double side band (DSB) NF at 60MHz and +3dBm in-band IIP3 (Fig. 7 (a)).

Relative amplitudes and phase shifts of all possible VM settings are measured with UXA N9040B IQ analyser option. By this option, UXA splits measured signal into IQ vectors. By taking the first measurement as reference, all the control words of VM were swept and resulting IQ vectors constellation is shown in Fig. 7 (b). It is observed that phase variation around outer circle is less than 1.5° and close to the center less than 4° , respectively.

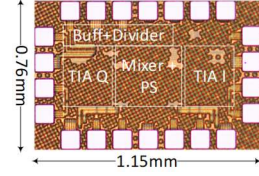


Fig. 5. Chip photograph of IF-RX module.

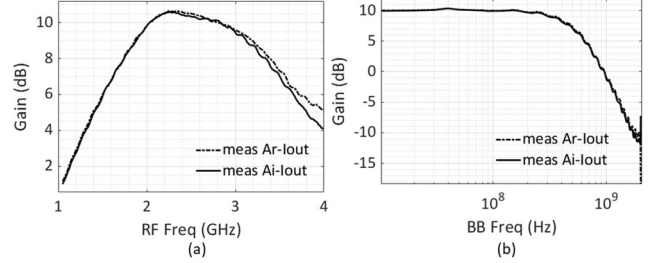


Fig. 6. (a) Measured frequency response of the IF-RX. Below 2GHz the off-chip RF input balun dominates the wideband response in the measurement setup. (b) BB gain and bandwidth measured at 2GHz LO.

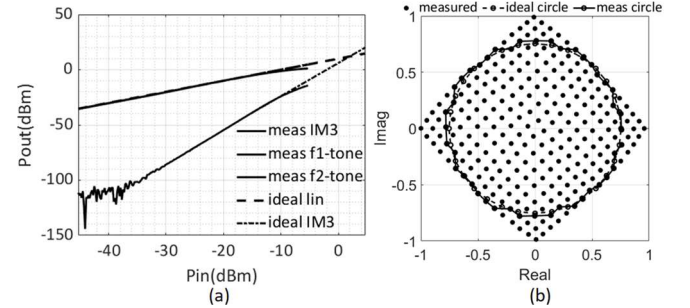


Fig. 7. (a) Measured in-band IIP3. RF tones were at 2.225 and 2.175 GHz and LO at 2GHz providing IMD3 components at 125 and 275 MHz. (b) Phase constellation of constant Gm-vector modulator measured at 2GHz LO and 2.1GHz RF.

B. Over-the-Air (OTA) measurement

IF-RX capability to cancel inter-beam interference from two adjacent sub-arrays as in [10] is verified using two IF-RX receivers with combined output. Measurements are performed over-the-air (OTA) using discrete 28GHz front-end of [11]. The front-end has two 16×4 -element sub-arrays (A1 and A2) with 16 electrically controllable phase shifters, one for each 2×2 antenna group. A1 and A2 provide the IF output from 3 to 4 GHz and outputs are combined at BB using IF-RX shown in Fig. 8. Only single stream configuration of the IF-RX (red in Fig. 8) is used for verification. One input V_{Ar} of IF-RX is used because sub-array IF output is single-ended. The other IF-RX input is terminated to 50 Ohms and it is needed only for possible mmW gain control. VM itself in IF-RX will not require both inputs in the setup.

A1 and A2 are horizontally aligned on top of each as shown in Fig. 8. The two horn antennas, H1 and H2, transmit two continuous waves (CWs) at two-meter distance representing two data streams from different sources at 28.00 and 27.98GHz, at 10° angle difference. On the receiver side, first A1 is switched ON and A2 is OFF. A1 receives signal from H1 and H2 and converts signals to IF of ~ 3.6 GHz. Then IF-RX1 converts CWs to baseband output at f1 (100MHz) and f2 (80MHz). The beam patterns of sub-array A1 were measured at f1 and f2 and are shown in Fig. 9. It also provides the information about the level of f2 as an interferer (dashed line at 0°), when A1 is steered in the direction of H1 and vice versa. Same measurements are performed for A2.

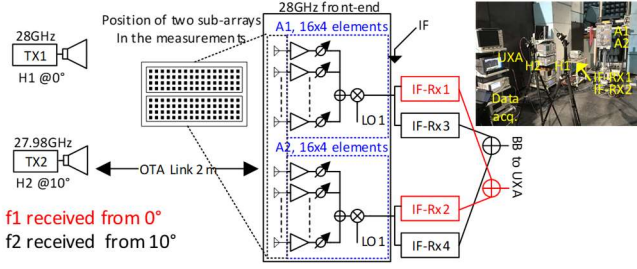


Fig. 8. System configuration for receiving multiple streams with cancellation for system verification.

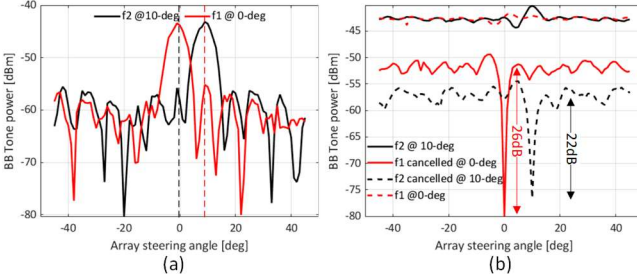


Fig. 9. (a) Beam pattern measured OTA without interference cancellation and (b) measured level of interference cancellation.

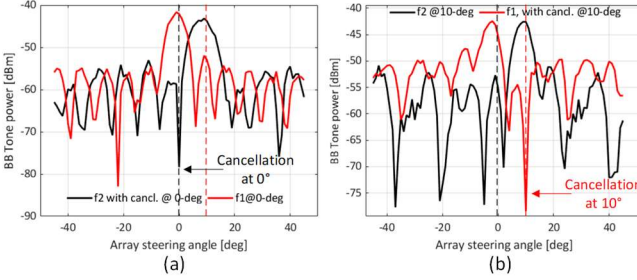


Fig. 10. Measured beam pattern after interference cancellation at 0° (a) and at 10° (b).

Table 1. Comparison with previous scalable phased array solutions

	[5]	[4]	[3]	This Work
Technology	40nm	40nm	130nm	45nm-SOI
PS Topology	BB	BB	LO	BB
Interference cancellation	No	No	No	26dB
Support No. of Element	1	4	1	flexible
RF Frequency (GHz)	12	BB	6 - 18	2 to 4
BB Bandwidth (GHz)	0.7	1	0.8	0.4
Phase resolution (°)	8.6	6.8	<1	8.2
Gain (dB)	6.6	10 - 30	16 - 24	10
PDC (mW)/element	14.7	10.5	195	104
Noise Figure (dB)	13	13	12	5.5
In-band IIP3(dBm)	0	1.4	-15	3

Then both A1 and A2 are switched ON for interference cancellation measurements. A1 is steered to 0° and A2 to 10°. First, 10° interferer is canceled by weighting IF-RX2 at A1 and cancellation result is ~22dB (see black dashed curve in Fig. 9 (b)). The pairs of dashed curves in Fig. 9 (b) are obtained by sweeping the phase shifters of A2. The red dashed curve shows signal level received from 0° at BB. The cancellation can be seen in beam pattern shown in Fig. 10 (a) by sweeping the A1 phase shifters. In the second measurement, 10° interferer is canceled by weighting IF-RX1 at A2 and result in ~26dB of cancellation (red solid line in Fig. 9 (b)). Beam pattern with cancellation is shown in Fig. 10 (b).

Results are compared with other scalable phased arrays in Table 1. In VM operation, it can provide 32dB amplitude

control that can be used for interference cancellation. The power consumption of the IF-Rx can still be considered as low because it would be in-front of a very large sub-array, which is not the case of [3] and [5].

V. CONCLUSION

In this paper, an IF-Rx module is presented that enables a scalable approach for large scale phased arrays operating at mmWave. The processing at an IF of a few GHz provides the freedom to improve the spatial selectivity by having accurate weights for interference cancellation. OTA measurements were performed to show the interference cancellation between sub-arrays by using IF-RX. IF cancellation improves ~26 dB of spatial selectivity measured from the worst-case scenario that is here the first sidelobe. The low noise figure of 5.5dB and high in-band dynamic range (IIP3 of 3dBm) make system processing insensitive to sub-array gain.

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