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Resilient flow control for wireless data streaming in inductively coupled medical implants



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1. Introduction

In recent years, the complexity of implantable medical devices has steadily increased, driven by the downscaling of the transistor size and the ever-increasing demand on the performance of electronic systems used for applications like continuous patient monitoring [1,2] and seizure onset prediction [3]. Enabled by modern nanometer-scale semiconductor technology, the complexity of medical implants can reach a level comparable to that of an advanced System-on-Chip (SoC), where power regulators, multichannel front-ends, and digital post-processing are integrated into single die. Many implant-centric works are shifting the focus from optimizing simple functions to improving the performance of the whole application-specific SoC through increased complexity and advanced system-level design techniques [4].

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ABSTRACT

This paper describes the hardware implementation of a custom communication protocol tailored for low power telemetry data streaming over an inductive link. An efficient transceiver design is achieved by adapting only the essential physical layer features of a typical RFID baseband processor and optimizing the flow control logic for continuous and reliable data transfer. For the external near-field reader, we provide a logical model for receiver operation and suggest a simple forward error correction (FEC) mechanism. The benefit of FEC in the context of developed communication system is demonstrated by simulations, and projections of design scalability are also presented. The proposed communication system was implemented in 28nm CMOS process. Place-and-route (PNR) results occupy only 0.0048 mm² of core area, and the transient simulations show a power consumption of 306 nW at 0.5 V supply and a master clock of 845.7 kHz. The implementation provides an uplink rate of 12 kbit/s, sufficient for reliable transmission of a 1-channel 1 kS/s 12-bit sample recording.

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As implantable electronic system becomes more intricate, so does the amount of processed information. Consequently the communication traffic between implants and the external readers is increasing in volume. Typically, such traffic is exchanged wirelessly using industrial, scientific and medical (ISM) frequency bands. In the case of subcutaneous medical devices that are implanted only a few centimeters below the skin surface, the acquired information can be communicated over an inductively coupled wireless link, which also serves as the main power feed for the electronic system [5]. When single inductive link is not sufficient for data acquisition, the reverse telemetry data may be transmitted via auxiliary wireless channels at expense of more sophisticated system setup [6].

The universal performance metric which demonstrates the communication capability of an implant is the uplink data rate. In massive biopotential acquisition such as Electroencephalogram (EEG) and Electrocorticogram (ECoG), higher data rates imply richer possibilities in data analysis, enabled by more channels and higher sampling resolution. While a lot of related implant SoC papers report state-of-the-art transmission rate figures up to

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megabits per second, the description of utilized communication techniques is often limited to physical layer aspects such as choice of carrier, modulation, and clock recovery methods [7–10]. Similar trend can be observed for implant sensors targeted at less uplink-intensive applications such as blood pressure monitoring [11,12]. To the best of authors' knowledge, the data link layer details of implemented communication routines such as packet structure, error correction, or data retransmission are rarely reported in the implant literature, exception being custom large-scale designs such as [13]. This leads to research question: how should the implant communication be organized in a reliable yet power-efficient manner?

This paper is an extension of our previous work [14] where we presented a low power implementation of a customized communication protocol specifically targeted at inductively powered implantable medical sensors. This manuscript extends our findings in robust implant communication with deeper analysis of utilized channel airtime and effects of error correction on the effective throughput of the communication system. For the implemented hardware we present evaluations of active power consumption profile of pre-layout digital circuit and report the effect of power supply scaling in various process corners. To demonstrate the potential for adapting this design for higher data rates, we show projections of link performance versus the clock frequency.

The paper is organized as follows. Section 2 gives a brief overview of state of the art in the scope of wireless medical communication. Section 3 introduces the proposed communication protocol and outlines the parameters of the implant baseband processor. Section 4 describes the implementation of proposed hardware in digital logic. Section 5 presents the results of hardware synthesis and further analysis of the communication system. The conclusions will be given in Section 7.

2. Prior art

The topic of wireless implant communication covers a wide range of experimental and industrial devices, ranging from commonly known cardiac pacemakers to novel endoscopy capsules [15]. There is a number of frequency bands that are utilized for this purpose [16], however a distinction can be made between high-performance medical radio link and the inductive near-field data channel.

2.1. Medical transceivers

A majority of works related to wireless medical device communication focuses on optimizing the transceiver hardware for Medical Implantable Communication Service (MICS) frequency band [17]. In this area, the emphasis is generally on low-power circuit design techniques that enable integration of advanced radio components such as low-noise amplifier (LNA) and I/Q modulator into power budgets of micro watt range [18–24]. Few transceiveroriented works also target an additional ISM band as auxiliary signalling channel [25–27]. In terms of logical link control, reported details are usually scarce. However, one paper on proprietary Zarlink (now Microsemi) MICS-band transceiver [28] is of particular interest, for its brief mention of automatic retransmission and error correction practices that are relevant for this work.

On the higher level, a number of papers investigates the issues of medical device communication within Wireless Body Area Network (WBAN) [29]. The typical issue being addressed is the Medium Access Control (MAC), with most of the related works focus not on optimizing point-to-point communication but on novel arbitration mechanisms to increase the collective throughput efficiency of the whole network. A lot of this protocol-oriented research is adapting channel access methods such as ALOHA, CSMA, or TDMA into context of WBAN [30–35]. There are also several proposals of utilizing the wake-up radio signal over an additional radio band to improve the latency on the main transmission channel [36–38]. A recurring issue reported in this area is the need of handling the so-called emergency traffic with a deterministic delay, as dictated in the MedRadio standard by Federal Communications Commission (FCC) [39,40].

2.2. Near-field channel communication

Like any inductively powered electronic device, medical implants can utilize the same inductive link for bidirectional data exchange without resorting to use of additional frequency bands or advanced radio hardware. In such environment, the uplink transmission from the device to its power provider is realized by modulating the antenna load impedance on the receiving end [5], essentially requiring a constant carrier wave to be supplied externally. Because of that, the near-field channel communication is typically organized in a master-slave fashion where power provider orchestrates the transaction. This type of exchange is employed to a great extent in the scope of Radio-Frequency Identification (RFID), where the reader device uses the inductive link to provide power and access to the non-volatile memory on a "passive" tag device.

Reported implementations of integrated RFID systems indicate a considerable potential for ultra-low power operation [41–44] and RF energy harvesting [45–47]. Some works extend the functionality of inductively-powered devices beyond simple memory access to incorporate features such as data encryption [48], ultrawide-band frequency hopping [49], and most importantly, sensor interfaces [50,51]. Papers on RFID sensing describe integration of Analog-to-Digital Converter (ADC) [52–54] and even complete sensors [55] together with the typical near-field transceiver functionality. There also exists a family of programmable devices called Wireless Identification and Sensor Platform (WISP) [56], an open-source initiative which helps to facilitate research in this field [57,58].

The majority of developed passive sensor systems are designed to operate in conjunction with a standardised Ultra-High Frequency (UHF) RFID reader. The associated communication standard is publicly open and governed by GS1 as the Electronic Product Code (EPC) "Gen2" air interface protocol [59]. However, while providing the means for data exchange, this protocol is mainly targeting industrial applications like inventory management and access control. All devices compliant to EPC Gen 2 are bound to implement the protocol practicalities such as memory access functions and anti-collision measures [60], which in turn introduce overhead in terms of hardware (random number generator) and airtime (handshake, arbitration). These standard-specific features are not necessary in the context of a direct communication between the implant and the reader separated by a layer of body tissue.

3. Proposed communication protocol

This work aims to provide a set of communication primitives necessary to establish continuous transmission of ADC readings from the front-end of an inductively coupled implant. In order to minimize the typical overheads discussed in Section 2.2, only the basic data link functions of RFID transceiver are incorporated into this implementation. The intention of this work is not to comply with an existing standard such as MICS or EPC Gen 2, but to find the baseline which enables a reliable wireless streaming interface while keeping in mind the exceptionally constrained power and area budget.



Fig. 1. Example communication scenario.

Table 1 Reader-to-implant commands

Bit #0 Bit #1 C	Command name	Function
0 s	top	Stop communication, halt buffer
0 1 s	end (ACK)	Start communication, send new packet (previous packet is OK)
1 0 r	resend	Send previous packet
1 1 -	-	Reserved for future use

3.1. Master-slave communication scheme

In telemetry implants, the data payload often comes as an uniformly sampled signal. The task of the communication subsystem, especially in implants without mass storage is to ensure that all of the acquired data arrives at the reader device. In order to preserve the integrity of the sampled sequence transmitted through a noisy medium, the communicating entities must incorporate a mechanism to avoid data loss and corruption. Two most important protocol features suggested for to counter these effects are the error detection and the automatic repeat request (ARQ) [28,61]. For cases when error cannot be corrected at the reader, the received samples shall be stored in buffer memory for retransmission. The reader device should implement a fast ARO routine so that the implant gets either an Acknowledgement (ACK) or a retransmission request after every transmitted packet. These functions are realized with two reader commands, namely "send" and "resend". Former can be also used to initiate the transmission.

The example communication scenario between reader and implant is illustrated in Fig. 1. The reader initiates the transmission by requesting a packet, and the implant responds as soon as data is ready. Should the data become corrupted, reader detects the damage and requests to resend the packet. To provide the reader with ability to pause the communication, an additional "stop" command is used. Resuming (and starting) the operation should be possible with the "send" command. Table 1 shows the full list of the commands which can be enumerated with two bits, thus reserving minimal overhead for the downlink message. Based on this requirements, a simple functional model of the reader is conceived as described by the flowchart in Fig. 2. In addition to maintaining the nominal link shown in Fig. 1, this reader model takes the transmission black-outs into account with a timeout clause. Each received packet should also pass through data error check.



Fig. 2. Simplified model of reader operation. Gray blocks indicate commands sent to the implant.

3.2. Error detection and correction

An efficient way to enable detection of corrupted data is to transmit a Cyclic Redundancy Check (CRC) pattern together with the payload [62]. For calculating the checksum, we choose conventional CRC16-CCITT generator polynomial

$$g(x) = x^{15} + x^{12} + x^5 + 1.$$
⁽¹⁾

Even though there exist other 16-bit polynomials which provide better performance for detection of higher-order errors, (1) has minimal amount of non-zero elements which allows for a compact hardware implementation [63] and is therefore advantageous for use in implants.

On the reader side, forward error correction (FEC) of the received data can be realized by using the CRC pattern appended to it. Optimal CRC16 polynomials such as (1) are capable of detecting a single-bit flip in payloads up to 32,767 bits in length and there exist methods to recover the flipped bit using precomputed lookup tables [64,65] or tailored digital logic [66]. Correction of two-bit errors has also been reported [67].

3.3. Physical layer

For the physical air interface, the proposed protocol utilizes Amplitude-Shift Keying (ASK) and backscattering as the most basic modulation techniques for inductively coupled channel [16,68]. During the whole communication time, reader emits continuous wave (CW) and sends commands with Pulse-Width Modulated (PWM) envelope. The implant response is backscattered by means of On-Off Keyed (OOK) load modulation. Fig. 3 gives an example of the time division sequence where downlink and uplink frames are separated by pre-defined periods T_{reply} and T_{post} accordingly. As a generic convention for a PWM downlink, we use the Pulse-Interval Encoding (PIE) as described in EPC Gen 2. The OOK uplink from





Fig. 4. PIE and FMO symbols and respective preambles.



Fig. 5. Structure of the implant baseband processor.

tion parameter

Table 2

Frequency bandCarrier (CW)866 MHzFM0 baseband422.85 kHzPWM ParametersDelimiterDelimiter12.5 μs data-015 μs data-125 μs PW5 μs RTcal40 μs Wait PeriodsTreplyTpost40 μs	communication parameters.						
Carrier (CW)866 MHzFM0 baseband422.85 kHzPWM ParametersDelimiter12.5 μs data-015 μs data-125 μs PW5 μs RTcal40 μs Wait PeriodsTreply40 μs	Frequency band						
FM0 baseband422.85 kHzPWM ParametersDelimiter $12.5 \ \mu s$ data-0 $15 \ \mu s$ data-1 $25 \ \mu s$ PW $5 \ \mu s$ RTcal40 \ \mu sWait PeriodsTreply40 \ \mu s	Carrier (CW)	866 MHz					
PWM ParametersDelimiter $12.5 \ \mu s$ data-0 $15 \ \mu s$ data-1 $25 \ \mu s$ PW $5 \ \mu s$ RTcal $40 \ \mu s$ Wait PeriodsTreplyTpost $40 \ \mu s$	FM0 baseband	422.85 kHz					
Delimiter $12.5 \ \mu s$ data-0 $15 \ \mu s$ data-1 $25 \ \mu s$ PW $5 \ \mu s$ RTcal $40 \ \mu s$ Wait PeriodsTreplyTrpost $40 \ \mu s$	PWM Parameters						
data-015 μs data-125 μs PW5 μs RTcal40 μs Wait PeriodsTreplyTropst40 μs	Delimiter	12.5 μs					
data-1 $25 \ \mu s$ PW $5 \ \mu s$ RTcal $40 \ \mu s$ Wait Periods $reply$ Treply $40 \ \mu s$ Tpost $40 \ \mu s$	data-0	15 μs					
PW5 μsRTcal40 μsWait PeriodsTreply40 μsTpost40 μs	data-1	$25 \ \mu s$					
RTcal40 μsWait PeriodsTreply40 μsTpost40 μs	PW	$5 \ \mu s$					
Wait PeriodsTreply40 μsTpost40 μs	RTcal	40 μs					
Treply 40 μs Tpost 40 μs	Wait Periods						
Tpost 40 μs	Treply	40 μs					
	Tpost	40 µs					

the implant is encoded with FMO [59]. Fig. 4 gives an overview of symbols and preambles of corresponding encoding schemes.

The numerical values for chosen communication parameters are presented in Table 2. The 866 MHz carrier is selected according to UHF RFID band regulations in Finland [69]. The baseband rate is fixed in kilohertz range to a value 2¹¹ times lower than the carrier frequency so that the uplink clock can be derived from it with a simple binary divider.

3.4. Implant baseband processor

Fig. 5 shows the feed-forward structure of the implant communication processor. At the start of the chain, the asynchronous firstin first-out (FIFO) transfers the front-end data from the slow sampling clock domain into the baseband clock domain. FIFO also acts as a buffer for accumulating the multi-sample payloads and storing the excess data when old packets are pending to be retrans-

Table 3 System parameters.	
Front end	
Sampling rate Resolution	1 kS/s 12 bit
FIFO Width Depth	12 bit 8 words
Transceiver Uplink bit rate Packet rate Payload size Uplink packet size	12 kbit/s 500 packets / s 24 bits 47 bits

mitted. The packet manager collects the data from FIFO to populate the payload and calculate the CRC checksum. Transceiver block will handle parsing of reader commands and encode the prepared uplink packets.

Table 3 gives an overview of system parameters selected for the implementation. With a 12-bit 1 kS/s front end, the effective bit rate of the whole acquisition chain is 12 kbit/s. However, the transmission doesn't have to happen at the exact rate of the front end, so in order to reduce the overhead per payload, we choose to send uplink payloads twice as slow but twice as long. The final size of the uplink packet is 23 bits longer than that of the payload, with 16 bits occupied by CRC, 7 bits by FM0 preamble (Fig. 4) and one bit is the FM0 end-of-signaling [59]. To provide room for packet retransmission, an 8 word deep FIFO size is selected, which gives us 7 ms margin of standalone data acquisition.

3.5. Utilized airtime

The estimation of airtime occupied by active communication is important for planning packet retransmission. More free airtime means that the reader-implant system can recover more quickly after transmission black-outs and return to normal data streaming mode. During normal operation, the utilized portion of total airtime can be approximated as

$$A = f_{\text{packet}} \left(\frac{n_{\text{pay}} + n_{\text{ovh}}}{f_{\text{FM0}}} + T_{\text{cmd}} \right), \tag{2}$$

where $f_{\rm FM0}$ is the FM0 baseband frequency, $f_{\rm packet}$ is the packet rate, $n_{\rm pay}$ and $n_{\rm ovh}$ are bit sizes of payload and packet overhead accordingly, and $T_{\rm cmd}$ is the duration of reader command overhead determined as

$$T_{\rm cmd} = t_{\rm reply} + t_{\rm preamble} + 2t_{\rm data-1} + t_{\rm post}$$
$$= t_{\rm reply} + t_{\rm delimiter} + t_{\rm data-0} + t_{\rm RTcal} + 2t_{\rm data-1} + t_{\rm post}.$$
(3)

From the values in Tables 2 and 3, the utilized airtime portion is only 15.4%, which means that it would take less than one normal exchange period (2 ms) to send all FIFO contents after communication black-out.



Fig. 6. Asynchronous FIFO with a level observer. The dashed lines denote the graycoded pointer data.

4. Implementation

The implant baseband processor was implemented in digital logic. The design was sectioned into three functional parts according to the architecture shown in Fig. 5.

4.1. Asynchronous FIFO and level observer

Fig. 6 shows asynchronous FIFO structure with grav-encoded pointers as described in [70]. During communication, the operation of data buffer is partly dictated by the transceiver, so the FIFO must also inform the packet manager about its immediate state (FIFO level). The state of an asynchronous FIFO is represented by read and write pointers and is distributed across separate clock domains. After each read or write event, corresponding pointer is updated and synchronized to the control unit in the opposite clock domain [70]. To simplify the domain crossing, gray-coded pointers are used as illustrated in Fig. 6 with dashed lines. The level observer logic resides in the reading clock domain and eavesdrops the signals of FIFO read controller. To determine the amount of words in the buffer, observer subtracts write and read addresses, and the full-condition (when addresses are equal) is resolved by gray pointer comparison as explained in [70]. Control of both read and write enable flags is done from the transceiver side, therefore the write flag has to also cross the clock domain along with the gray coded pointers.

It is important to note that synchronization of the read pointer lasts two cycles of the slow sampling clock. This causes a delay in informing the write controller that FIFO is emptied for next packet transmission. This equally affects the removal of full-condition at the writer side, which may momentarily inhibit the ADC from writing, even if FIFO is already flushed. In order to avoid losing samples at the input of the buffer, it is mandatory to always read the payload data sooner than FIFO becomes full. This also implies that the chosen sample buffer capacity shall not be equal but strictly larger than the payload size. In this work, during normal operation the FIFO is emptied after each two samples, so no data loss should occur due to synchronization.

4.2. Packet manager

The structure of the packet manager module is depicted in Fig. 7. The packet manager Finite-State Machine (FSM) controls



Fig. 7. Organization of the packet manager module. The registers which store payload and CRC are further accessible for the transceiver.



Fig. 8. State diagram for the packet manager FSM.

the packet assembly process according to state diagram shown in Fig. 8. Once enough samples are accumulated in the FIFO, the payload register is rewritten with a number of consecutive samples from the FIFO through the routing (R) demultiplexer. The contents of the new payload are fed into the CRC encoder with the serializer (S) multiplexer as shown in Fig. 7. Once the CRC operation is finished, transceiver is informed that the packet is available for transmission with the "ready" flag. The FSM will remain in the standby state until the "next" flag is asserted by the transceiver, then the operation is started from the beginning as illustrated in Fig. 8. 6



Fig. 9. Organization of transceiver module.

The difference between sampling and communication clock domains provides enough time in between front end samples to use a serial-type CRC encoder [71] without penalty in transmission speed, thus allowing to keep the physical area of the implementation at its minimum [72].

4.3. Transceiver

Fig. 9 shows structure of the transceiver. The control of communication is distributed between two state machines, namely the Transceiver FSM and the PWM decoder FSM. The PWM decoder performs non-coherent detection of ASK messages from the reader and passes the decoded command bits to transceiver FSM. Both state machines operate in the communication clock domain, frequency of which is dictated by the decoder, since PWM sampling resolution is the most restricting factor for the lowest clock rate in the system [43]. The coarse PWM constants selected in Section 3.3 allow to run the transceiver clock as slow as 845.7 kHz $(1/2^{10}$ of carrier frequency) without sacrificing lots of sampling resolution.

Once the "send" command is detected by decoder and the outbound data is prepared, the payload register will be serialized along with the rest of the packet elements into the FMO encoder as shown in Fig. 9. The length of the transmission is controlled with a dedicated slow counter so the encoding can be shut down by the FSM at the end of the packet. The FMO baseband clock is generated with a binary divider, providing a phase-coherent subdomain for safe register comparisons at the FSM side.

The FMO encoder is realized with a 2-flipflop structure (dashed section in Fig. 9) which is derived from the FMO state transition diagram [73]. The NOR gate suppresses the output of the encoder for the next high cycle of the uplink clock, producing the desired encoding violation during the transmission of FMO preamble sym-



Fig. 10. Value of the Interval counter during the decoding of command from the reader.

bols "101001" (see Fig. 4 for reference). At the end of the packet, a dummy "1" is appended to indicate the end of FMO signaling [59].

4.4. PWM Decoder

The PWM decoder utilizes a fast interval counter to measure the length of signals arriving from the synchronized envelope detector input (denoted as Rx in Fig. 9). During the uplink state, the decoder FSM stays in a standby state, activated by the transceiver FSM only after T_{reply} has passed. The detection of incoming PIE preamble starts with a low to high transition as shown in Fig. 10. If the delimiter length matches the pre-defined value (Table 2), the state machine resets the interval counter and measures the time between adjacent falling edges. If the received intervals do not deviate outside of $\pm 20\%$ bounds and all match the expected sequence, the decoder provides received command bits for transceiver FSM. In all other cases, decoder shuts down and raises the receiving-fail flag.

4.5. Transceiver FSM

Fig. 11 shows the flowchart of transceiver FSM operation. This state machine logically complements the reader (Section 3.1), thus realizing the proposed communication protocol. The normal operation sequence of implant transceiver is to wait until either "send" or "resend" commands are received by the PWM decoder and then upload the new or old packet accordingly. In order to control the state of implant data acquisition, an exclusive "session" bit in transceiver memory is set or reset with commands "send" and "stop" respectively. Initialized with zero, this flag controls the writing into FIFO as the "read" input to the packet manager. In exceptional cases such as when the PWM decoder gets a broken input sequence or "session" flag is not set, the implant will simply return to standby mode after pausing for duration of T_{post} . This delay, as well as T_{reply} are measured with a dedicated counter (not shown on Fig. 9).

5. Results

The hardware description of the proposed communication system was implemented in VHDL and synthesized for 28nm CMOS process. Place and route (PNR) was performed and layout was generated shown in Fig. 12. The timing closure of the implemented digital design was verified by static timing analysis tool. The functionality of the communication system was tested by analog transient simulation of pre-layout netlist and by register transfer level (RTL) simulation with back-annotated propagation delays extracted from the final layout.



Fig. 11. Flowchart of the transceiver FSM operation. Gray blocks indicate decisions based on the command from the reader.

5.1. Analog transient simulation

To determine the power consumption of the circuit in various states of its operation and to estimate its supply scaling capability, the analog transient simulation was performed as follows. First, the circuit comes out of reset state into standby mode, with both fast and slow digital clocks supplied from the start. 12-bit FIFO input is fixed at hex value of 0xAC9, which has equal amount of zeros and ones in binary. After 80 μ s of standby operation, a PWM sequence corresponding to reader "send" request is applied to the decoder input. The simulation continues for 2.3 ms until the FIFO input is sampled twice and the FMO packet is produced from the encoder output, thus covering a full communication cycle between implant and the reader.

To determine the lowest operating point for the circuit, this transient simulation was repeated with different V_{DD} values un-



Fig. 12. Layout of the baseband processor after place and route.



Fig. 13. Power consumption of the pre-layout circuit versus supply voltage. Analysis includes typical (TT), slow (SS), and fast (FF) process corners.

til the circuit stopped working at around 0.2 V supply. Total power consumption was extracted as a global average of power drawn from supply during the full communication cycle. Fig. 13 illustrates the effect of supply scaling on total power consumption as well as on the static (leakage) power consumption. The experiment was repeated for typical (TT), slow (SS), and fast (FF) process corners.

The lowest point of operation is at 0.21 Volt supply, where circuit consumes 58.43 nW of power, where 44.46 nW is static power consumption (leakage).

To determine the maximum clock frequency at which the circuit can operate, exhaustive transient simulations were ran by sweeping supply voltages from 0.21 Volt to 1 Volt and clock frequency from 1 MHz to 30 MHz. Table 4 shows the results of this evaluation. At 0.21 Volt supply, the circuit can operate only at 1 MHz supply clock, and at 0.3 Volt supply maximum clock frequency increases up to 12 MHz. From 0.4 Volt onward pre-layout



Fig. 14. Instantaneous power consumption during the PWM decoding. Averaging window of 10 μs is applied to smoothen the switching spikes.



Fig. 15. Instantaneous power consumption during the FMO encoding. Averaging window of 10 μ s is applied to smoothen the switching spikes.

Table 4Regions of operation for pre-layout digital circuit*.

		Supply voltage, Volt				
		0.21	0.3	0.4	0.5	0.6 – 1
Clock frequency, MHz	1	*	*	*	*	*
	2 - 12		*	*	*	*
	13 - 30			*	*	*

*Using slow (SS) corner and temperature of 36.6 degrees Celsius.

circuit can operate clocks up to 30 MHz, which is an order of magnitude greater than typical master clock for RFID applications.

The nominal supply voltage for the circuit is chosen to be 0.5 Volt, which is typical for digital circuits manufactured in 28 nm CMOS [74], [75]. Fig. 14 demonstrates the circuit power consumption profile at 0.5 Volt V_{DD} during decoding of the command from the reader. A 10 μ s averaging window is applied to the instantaneous power consumption waveform to smoothen the switching spikes. Similarly, Fig. 15 shows the power consumption during the FMO encoding. The average power consumption is indicated in



Fig. 16. Simulation of data loss and retransmission.

dashed line in both graphs. The baseline for standby power consumption slightly fluctuates from it depending on the phase of sampling clock (not shown). In both states of transceiver operation it can be seen that the system draws slightly more current than the average during periods of active switching, however the relative variation is still below 10 percent. This implies that with the proper supply decoupling network in place, proposed baseband processor can be considered as a constant load for the internal power regulator of the implant.

5.2. RTL Simulation

The resilience of communication system to transmission failures was verified with long RTL simulation. An setup sequence similar to that of the transient test was applied to the implemented system repeatedly. Fig. 16 shows the operation of the implant transceiver as it communicates with the reader emulator. Upon reader request, the implant accumulates the incoming data and dispatches it shortly. The reader acknowledges the successful transmission by requesting new data, and the procedure repeats. Upon issuing the "resend" command continuously, the reader forces the implant to reuse the packet while accumulating the data in FIFO. After the reader starts acknowledging the incoming packets again, the implant will continue the communication by dispatching all of the FIFO entries first.

5.3. Error correction analysis

In ARQ-type of communication over a lossy channel with a certain bit error rate (BER), there exists an optimum packet length which indicates the balance between dominating transmission overhead in small packets and susceptibility to error in big packets [76]. Hence, by taking the overheads such as CRC and preamble into account and selecting the payload of optimum length we can maximize the channel throughput under the given BER.

In order to evaluate the potential performance improvement from adding FEC to the proposed ARQ communication scheme, an idealized simulation of packet transmission and corruption was performed. To simplify the task, the commands from the reader



Fig. 17. Payload size versus normalized channel throughput at $BER = 10^{-2}$.



Fig. 18. Optimal packet size versus BER.

are assumed to take zero airtime, and the only overhead added to payload is the 23 bits of "service" data described in Section 3.4.

The assembled packets are then subjected to randomized errors with probability equal to BER. If less than two errors "land" on the payload, it is considered recoverable, but if any error lands on CRC or preamble, the whole packet is considered corrupted. The simulation is then run until total length of "sent" payloads is equal to certain value significantly larger than any packet size, e.g. 500 thousand bits.

Fig. 17 shows result of payload length sweep in presence of a constant BER of 10^{-2} . The curve demonstrates the relationship between the payload size and channel throughput, and most efficient payload length can be found from the horizontal location of the optimum peak. It can be noted that with 1-bit FEC there is an increase in the channel throughput, up to almost 60% more than with just ARQ alone.



Fig. 19. Projected airtime curves for packet rate of 500 packets/s.

Fig. 18 shows the progression of optimal packet size for a range of BER. It is visible that by using just one-bit FEC, the optimal packet size improves three-fold at a BER of 10^{-3} and more than six-fold at a BER of 10^{-4} . As hinted in [28], utilizing FEC technique on the reader greatly improves the effective BER of the communication channel.

5.4. Bit rate and airtime projections

To analyze the scalability of the proposed communication system, the nominal bit rate was extrapolated by increasing the major design parameters: master clock, payload size, and packet rate. We obtain bit rate as a function of airtime and master clock by rearranging airtime equation (2) as

$$BR = A \frac{f_{Mclk}}{2} - f_{packet} \left(n_{ovh} + T'_{cmd} \frac{f_{Mclk}}{2} \right), \tag{4}$$

where the new elements are the channel bit rate BR ($f_{\text{packet}} \cdot n_{\text{payload}}$) and the master clock factor $f_{\text{Mclk}}/2$ which denotes the FMO baseband frequency derived by the transceiver (Section 4.3). The reader overhead T'_{cmd} is scaled down from the original value of T_{cmd} with the inverse of f_{Mclk} so that relative length of the reader command intervals stays constant from the perspective of PWM decoder.

Fig. 19 shows the projected bit rate for master clocks up to 2 MHz. Straight lines indicate the bit rate evolution when the utilized airtime is kept constant. For example, when clocking the implemented circuit using the master clock of 2 MHz instead of original 845.7 kHz, the 12 kbit/s transmission would occupy significantly less than 15% of total airtime (region below dotted line). If the allowed payload size is increased along with the master clock, the system can achieve throughput of up to 100 kbit/s and not exceed the 15% airtime limit. The throughput can be further increased by choosing longer payloads, but this is done at expense of airtime available for retransmission. If we were to determine parameters of a high bit rate system from this plot by increasing the payload, at some point the its length will become sub-optimal for large values of BER, according to the results outlined in Section 5.3. In such case, the packet rate f_{packet} can be also increased, meaning that the data will be sent more often through smaller packets, which is a good trade off in terms of overall channel efficiency, like demonstrated on Fig. 17.

Fig. 20 illustrates the bit rate lines for 50% and 100% airtime when the packet rate is increased to 2000 packets/s which is four

Table 5

Р	er	form	ance	comp	arison.	
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Work Year	Y. He [77] 2006	X. Yang [78] 2010	C. Chung [79] 2011	D. Wei [43] 2012	L. Xie [80] 2013	X. Liu [44] 2015	This work
Obtained results	Experimental	Simulation	Experimental	Experimental	Simulation	Experimental	Simulation
Process node	0.35 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm	28 nm
RFID Protocol	EPC Gen 2	EPC Gen 2	EPC Gen 2	EPC Gen 2	ISO 18000-6B	GB 29768-2013	Custom
Uplink data rate	640 kbps	640 kbps	640 kbps	640 kbps	160 kbps	640 kbps	12 kbps
Supply voltage	1.5 V	1.1 V	0.8 V	1.0 V	0.77 V	0.6 V	0.5 V
Clock frequency	1.28 MHz*	720 kHz	2.07 MHz	1.92 MHz	1.28 MHz	640 MHz	845.7 kHz
Power consumption	3.15 μW	0.963 μW	2.64 μ W	2.7 μW	0.92 μ W	215 nW	306 nW
Digital core area	0.88 mm ²	0.126 mm ²	0.0692 mm ² **	0.11 mm ²	0.11 mm ²	0.1 mm ²	0.0048 mm ²
$FoM\left[\frac{Uplink(kbps)}{Area(mm^2) \cdot \frac{Pow.cons.(nW)}{Clock(MHz)}}\right]$	0.2955	3.7977	7.2517	4.1374	2.0237	19.0512	6.9093

* Clock frequency was not reported. Listed value is taken from preceding publication from the same group (which describes the design of the exact transponder processor) [81].

** Area of the digital baseband processor is estimated from chip micrograph.



Fig. 20. Projected airtime curves for packet rate of 2000 packets/s.

times the original (Table 3). As an example of a high bit rate application, subcutaneous EEG is selected [82]. Dotted line indicates the bandwidth required to transmit the output of 32-channel ADC front end of 16-bit resolution and 512 S/s sample rate. Since the 100% airtime is the absolute maximum available, choosing master clock around 1.5 MHz will either result in insufficient channel bandwidth or no room for packet retransmission. If, say, nominal airtime of at most 50% is desired, the intersection point with corresponding airtime line indicates the minimum master clock required, in this case it is around 3 MHz. The horizontal distance to the 100% airtime line illustrates the available room for packet retransmission.

When extrapolating the properties of the proposed communication system, it is important to keep in mind that the total power consumption of the system will scale linearly with the master clock. When selecting larger payload sizes, the depth of the FIFO should be scaled accordingly to ensure standalone operation during communication black-outs. Increasing the FIFO size will expand the layout area of the system and affect the static power consumption due to larger amount of registers.

6. Performance comparison

Table 5 shows the performance summary of the implemented circuit and compares it with other low-power RFID baseband pro-

cessor implementations using Figure of Merit (FoM) defined as

Proposed FOM =
$$\frac{\text{Uplink(kbps)}}{\text{Area}(\text{mm}^2) \cdot \frac{\text{Pow.cons.}(\text{nW})}{\text{Clock}(\text{MH}_2)}}.$$
(5)

In relation to other works, our results show an improvement in terms of effective bit rate per product of (compensated) power consumption and core area, which demonstrates the benefit of strictly application-specific system design. It should be noted that our results are based on simulation and do not take on-chip implementation into account.

7. Conclusion

This paper presents a custom implementation of an inductive link communication protocol especially targeted for telemetry data transfer in the context of implants. The proposed protocol provides the means to communicate with an external reader and mitigate data loss while utilizing minimal hardware resources. This design target was achieved by incorporating only the functionality which is necessary for reliable data transmission. The throughput of the envisioned reader-implant system under different channel conditions was estimated, and the optimum packet size for each test case is estimated. The suggested error correction mechanism is shown to increase the optimal packet size and hence the channel throughput for any BER value. The scalability of system bit rate and airtime was discussed and recommendations for increasing throughput were given. With selected link parameters, the hardware footprint of the proposed implant hardware was shown to occupy only 0.0048 mm² of chip area. The transient simulation with a 0.5 V supply and a master clock of 845.7 kHz shows a relatively steady power consumption of 306 nW throughout the communication cycle. The implemented communication system provides uplink rate of 12 kbit/s for reliable 1 kS/s 12-bit ADC transmission, and allows for up to 7 ms of standalone operation during communication black-outs. The achieved results indicate that the proposed implant baseband processor fits well in the constrained requirements of a medical implant design, in terms of both area and power consumption [83], therefore leaving sufficient resources for the signal acquisition front-end.

Declaration of Competing Interest

The authors declare that they do not have any financial or non-financial conflict of interests.

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