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Effects of Heavy Ion and Proton Irradiation on a SLC NAND Flash Memory

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Abstract—Space applications frequently use flash memories for mass storage data. However, the technology applied in the memory array and peripheral circuitry are not inherently radiation tolerant. This work introduces the results of radiation test campaigns with heavy ions and protons on a SLC NAND Flash. Static tests showed different failures types. Single events upsets and raw error cross sections were presented, as well as an evaluation of the occurrences of the events. Characterization of effects on the embedded data registers was also performed.

I. INTRODUCTION

Flash memory is a non-volatile memory (NVM) technology introduced in the late 1980's, which has found widespread adoption in the industrial and consumer electronics market. Flash memory cells rely on a single floating-gate Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) for information storage. These transistors possess two gates: an insulated floating gate (FG) located immediately above the channel, and a control gate (CG) located above the FG. Using one of several possible carrier injection mechanisms, the FG can be charged (programmed) or discharged (erased). The presence of charge in the FG partially screens the electric field from the CG, leading to a change in the threshold voltage of the transistor [1]. Depending on the quantity of charge which can be injected in a FG, and on the precision of the measurement of a cell's threshold voltage, each cell can be used to store one bit (single-level cell, SLC) or several bits of information (multiple-level cell, MLC). Two main architectures exist for flash memory array: NOR flash, where each cell is independently connected to a bit line (which enables random-access functionality and fast read operation), and NAND flash, where cells are connected in series (which enables higher storage density).

Compared to other NVM technologies, Flash memory suffers from poor access latency (in the order of microseconds)

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and read/write speed, as well as low endurance due to gate oxide degradation during cell program and erase. However, because each memory cell is made up of only one transistor, flash technology enables extremely high storage density and low cost-per-byte, which has made it the technology of choice for mass data storage.

Since flash memory cells rely on electric fields and charge trapping, they are inherently sensitive to ionizing radiation: when a charged particle goes through a charged floating gate, it can cause it to discharge, thus corrupting the stored information [2]. This failure mechanism, called single-event upset (SEU), is a major concern for space applications, where high radiation environments can lead to rapid accumulation of errors in flash devices, beyond the mitigation capacity of error-correction codes (ECC). Furthermore, the peripheral circuitry of flash devices, which is used to access, read and write to the memory array, is manufactured using CMOS technology, which is also sensitive to various single-event effects (SEEs) [3].

Heavy-ion and Total Ionizing Dose test results in four different Flash memories are presented in [4], the authors highlight the sensitivity difference of the memories in a radiation environment, comparing three different architectures: SLC, MLC, and TLC (triple-level cell). Also, [5] presents three different kinds of permanent effects under heavy-ion irradiation in the same SLC NAND Flash memory that is the target of this work; these failures are non-recoverable with a power cycle. The response of MLC and SLC NAND Flash memories to low-energy protons are exploited in [6], showing that MLC NAND Flash memories are sensitive to low-energy protons, but, on the contrary, the SLC NAND Flash cells in the same technology presented not to be sensitive.

In this paper, we report the findings of a study on effects of heavy ion and proton irradiation on an SLC NAND flash memory's memory array and data registers.

II. EXPERIMENTAL SETUP

A. The Flash Memory Device

The memory tested in this study was the MT29F32G08ABAAA, a 32 Gib Asynchronous SLC

NAND flash memory manufactured by Micron Technology. Its memory array is composed of two planes with 2048 blocks. A block is composed of 128 pages, each page is divided in 8192 columns, and each column stores one 8-bit word. For the irradiation test campaigns, all specimens were delidded via chemical means and passed functional tests, ensuring that all the memories were fully operational before the irradiation. Fig. 1 presents a top-down photograph of the delidded device.

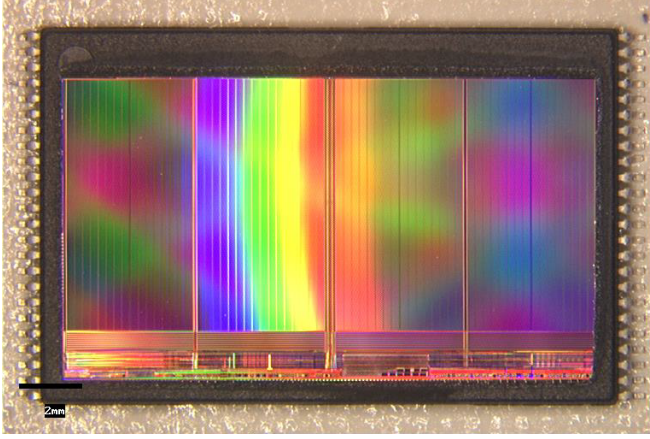


Fig. 1. Top-down photograph of the SCL NAND flash.

B. Test Facilities

Heavy-ion tests were carried out in two test campaigns (TC). The first test campaign (TC9) was performed at the Grand Accélérateur National d'Ions Lourds (GANIL, Caen, France). A broad xenon beam was degraded to reach an LET (Linear Energy Transfer) in silicon of 26.75 MeV.cm²/mg at the memory surface at normal incidence. The TC9 values presented in Table I were provided by the GANIL facility.

The second test campaign was realized at the RADiation Effects Facility (RADEF) at the University of Jyväskylä, Finland. In this TC, memories were tested in a ranging from 1.8 to 60 MeV.cm²/mg using the broad beam with different sources. The beam incidence angle was varied from 0° to 30° to reach the effective LET values presented in Table I, which were calculated using SRIM tool [7].

Protons tests were conducted during a test campaign (TC15) at Paul Scherrer Institute (PSI, Switzerland). Table II presented the source characteristic.

Fig. 2 represents the LET spectrum of all particles encountered over one year around solar minimum on an orbit at a 600 km altitude and 98.7° inclination (this includes solar energetic particles, trapped particles and galactic cosmic rays). This illustrates that the ions used in these experiments are representative of the most ionizing particles in the low Earth orbit radiation environment; while relatively rare, these particles are the most likely to induce errors in electronic devices. The interested reader can turn to [8] for more ample information on the space radiation environment.

TABLE I
FACILITIES AND BEAMS USED FOR HEAVY-ION IRRADIATION.

Facility	Ion	Energy (MeV)	Effective LET (@ DUT surface) (MeV.cm ² /mg)	Range to Bragg peak in Si (μm)
GANIL TC9	Xe	6005	26.75	700
	N	139	1.8 and 2.1	202
RADEF TC13	Ne	186	3.6 and 4.2	146
	Ar	372	10.1 and 11.7	118
	Fe	523	18.5 and 21.4	97
	Kr	768	32.1	94
	Xe	1217	60.0	89

TABLE II
FACILITY AND BEAM USED FOR PROTON IRRADIATION.

Facility	Proton	Energy (MeV)	Effective LET (@ DUT surface) (MeV.cm ² /mg)	Range to Bragg peak in Si (μm)
PSI TC15	H	50.8	9.7x10 ⁻³	12,620
		101	5.8x10 ⁻³	42,360
		200	3.6x10 ⁻³	138,630

C. Test Setup

The test setup is described in Fig. 2, where the devices under test (DUTs) is placed on a daughter board that is connected to a motherboard featuring an FPGA-based controller. The controller system is connected to a host computer to provide the capability to send commands to perform different functions on the DUT (e.g., read and write operations), and to store the received log data with operation status and bit error data. The controller part was not exposed to radiation sources to ensure the reliability of the tests. Fig. 3 presents the overview of the test setup.

Since the test campaigns have a limited duration, to guarantee the capability to perform all the required tests, only 512 Mib of the 32 Gib of the memory capacity were considered, reducing the execution time of each run and maintaining a sufficient area for observation of failure mechanisms. Furthermore, functional tests were performed between the runs to ensure the full functionality of the memory.

III. RESULTS AND DISCUSSION

A. Static Mode Test

The static mode test consists of a write operation using a known data pattern (i.e. solid '0', solid '1' and checkerboard patterns), followed by the irradiation of the device. Subsequently, the memory is read back, and corrupted bits are identified. The tests were performed using heavy ions and protons and resulted in three different types of failures: isolated single bit upsets (SBUs), small clusters of word errors, and vertical lines (VLs).

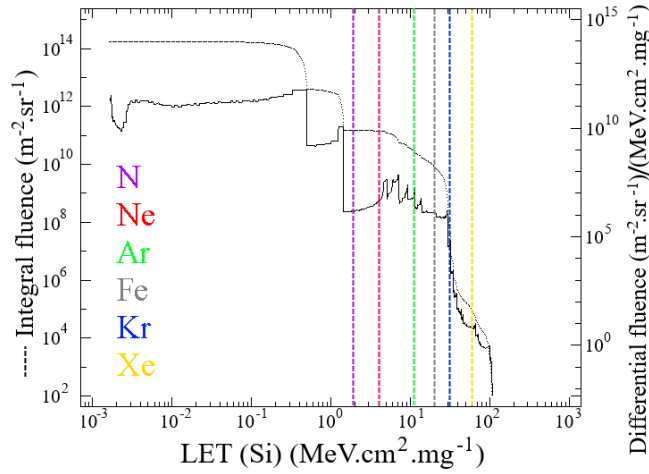


Fig. 2. LET in silicon of particles accumulated over 1 year around solar minimum on a 600 km orbit with 98.7° inclination. Calculated using AP8, SAPHIRE, CREME96 and ISO-15390 models via SPENVIS [9]. The dashed coloured lines indicate the LETs of ions used at RADEF, for comparison.

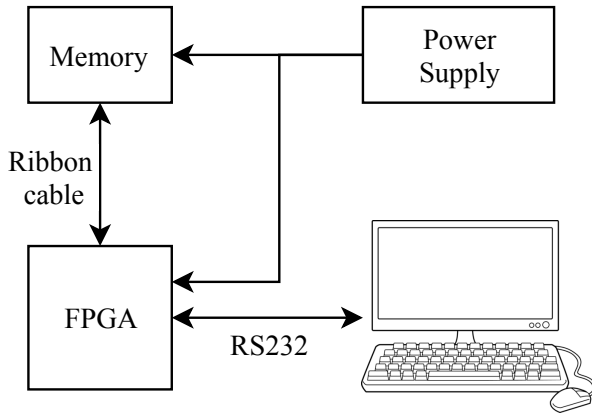


Fig. 3. Schematic of the experimental set-up for radiation testing of memories.

The static tests under heavy ions were performed at LETs from 1.8 up to 60 MeV.cm²/mg with a fluence range from 1.0x10⁴ up to 1.5x10⁵ cm⁻². The resulted data were post-processed using house-made scripts that identifies the failures types.

Static tests performed with Nitrogen using the solid '0' pattern resulted in 1 SBU at a LET of 1.8 MeV.cm²/mg and fluence of 3.0x10⁴ cm⁻², and respectively 2 SBUs at a LET of 1.8 and 2.1 MeV.cm²/mg at a fluence of 1.5x10⁵ cm⁻². Also, irradiation results with Neon using the solid '0' at a fluence of 1.0x10⁵ cm⁻² presented respectively 46 and 50 SBUs at a LET of 3.6 MeV.cm²/mg, and 11 and 18 SBUs at a LET of 4.2 MeV.cm²/mg. At those LETs, no errors were recorded when using the solid '1' pattern, and just isolated SBUs were detected.

Tests performed with the other heavy ions resulted in both isolated SBUs, small clusters and vertical lines. Individual VLs affects all the blocks within the memory plane, leading in continuous errors in a column in all the pages of a sequence

of blocks (all even blocks or all odd blocks). In this event type, the data pattern tends to be the same for all affect pages, resulting in a huge amount of errors in the data read.

The small clusters are characterized as a single or a double bit upset that were observed along two to ten vertically lined-up errors (i.e., the affected words are all at the same column position at adjacent line addresses). Neither diagonal nor horizontal clusters of errors were detected. These errors occur randomly across the entire bitmap. An interesting characteristic of those small clusters of errors is that the failing bit within the words is generally the same, and are generally SBUs. However, double bit upsets were identified once at LETs of 18.5 and 26.75 MeV.cm²/mg, 13 times at 32.1 MeV.cm²/mg and 147 times at 60 MeV.cm²/mg.

Examples of such error type are presented in Fig. 4. A detailed example is presented in Table III, where after a test using a solid '0' pattern, the readback and check operation identified four SBUs with the same data pattern in the same block and column, varying the page address consecutively. This failure type started to appeared at an LET of 10.1 MeV.cm²/mg, suggesting that the threshold for the occurrence of small clusters is between 4.2 and 10.1 MeV.cm²/mg.



Fig. 4. Close-up on a bitmap generated after static mode tests and showing the shape of single word errors or small cluster of errors.

TABLE III
EXAMPLE OF A READ BACK CHECK OPERATION IDENTIFYING A SMALL CLUSTER OF WORD ERRORS.

Block	Page	Column	Data Read
26h	60h	0D63h	02h
26h	61h	0D63h	02h
26h	62h	0D63h	02h
26h	63h	0D63h	02h

Isolated SBUs and upset clusters occurred only for solid '0' and checkerboard, and never for solid '1' data background tests. This behavior is in line with previous results, such as those reported in [10], stating that during beam irradiation, floating gate cells are more resilient to bit flips when storing a '1' (floating gate with no charge) than when storing a '0' (charged floating gate). These errors can all be removed by an erase operation, which discharges the floating gate (whereas a PC does not). Read cycles made after a PC all reveal about the same number of errors. These fluctuations are due to borderline cells, i.e., cells which have their floating gate at an intermediate value of charge after irradiation, which makes the result of reading access uncertain (intermittent errors) [11].

These small MCU clusters occurring along the bit line with almost the same error pattern can be explained by the action of a single particle hitting the memory plan. Charge sharing can also possibly occur, leading to several bits being upset in a single word. Secondary particles generated at angles may also be the cause of these vertical clusters, considering that spacers separate the columns and prevent/reduce the horizontally-shaped clusters.

In order to plot the SEU cross section for the tests under heavy ions, an isolated SBU, or an MCU cluster, or a VL is treated as one event. Besides the normal incidence angle, we use a tilt of 30° to increase the effective LET, then, the estimate cross section (σ) is defined as

$$\sigma = \frac{N/\cos(\theta)}{F \times M} \quad (1)$$

where N is the number of events, θ is the incidence angle, F is the beam fluence in particles/cm², and M is the number of bits [8]. The SEU cross section was fitted using the 4-parameter cumulative Weibull function

$$\sigma(LET) = \sigma_{SAT} \left(1 - \exp \left[- \left(\frac{LET - LET_{th}}{W} \right)^s \right] \right) \quad (2)$$

where σ_{SAT} is the saturation cross section, LET_{th} is the LET threshold, W and s are the width and shape parameters of the Weibull distribution [12, 13]. Fig 5 presents the acquired results.

It can be seen that the trend of this cross section appears to be compatible with a Weibull curve. The cross section of checkerboard and anti-checkerboard pattern is also plotted and was performed only at one LET (26.75 MeV.cm²/mg).

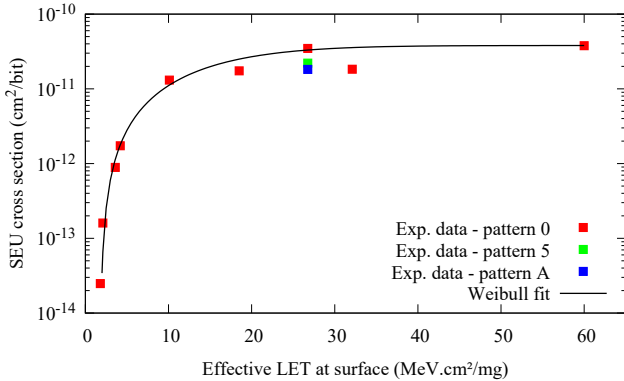


Fig. 5. SEU cross section calculated by dividing the number of SEU by the fluence and the tested memory size (i.e., 512 Mib). The LET threshold was estimated at 1.8 MeV.cm²/mg in order to fit the data with a Weibull curve. The Weibull parameters used are: $W = 16$, $S = 1.6$, $\sigma_{sat} = 3.8 \times 10^{-11}$ cm²/byte, $LET_{th} = 1.8$ MeV.cm²/mg.

In addition to the cross section of the SEU, for an application point of view, it is interesting to evaluate the number of errors identified regardless of the event that caused it. Fig. 6 presents the raw error cross section counting each bit in error without performing any clustering, in this case the number of events N is equal the number of bits upset.

The cross section presented in Figs. 5 and 6 show the same behavior for a LET up to 4.2 MeV. For LETs from 10.1 MeV upwards, since the events that imply a considerable quantity of errors (such as the VLs) start to occur, the raw error cross section results in a higher order of magnitude.

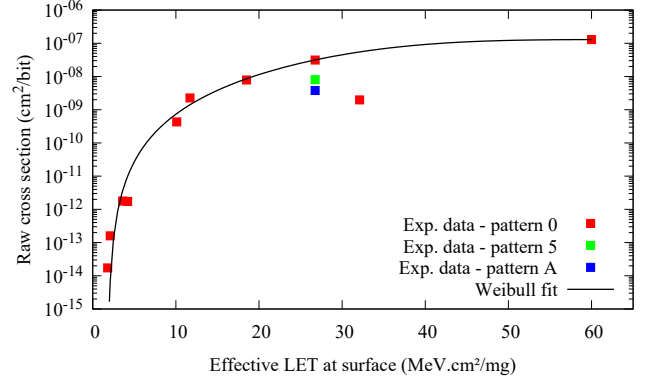


Fig. 6. Raw error cross section calculated by dividing the number of bit errors by the fluence and the tested memory size (i.e., 512 Mib). The LET threshold was estimated at 1.8 MeV.cm²/mg in order to fit the data with a Weibull curve. The Weibull parameters used are: $W = 36$, $S = 3.5$, $\sigma_{sat} = 1.3 \times 10^{-7}$ cm²/byte, $LET_{th} = 1.8$ MeV.cm²/mg.

Fig. 7 presents a ratio between the occurrence of an event type by the total number of events in a determined LET. Only isolated SBUs occurred for LETs under 4.2 MeV.cm²/mg. For higher LETs, the three different types of events appeared. Small clusters started to become more frequent than the isolated SBUs with the LET increase, showing that particles with a higher linear energy transfer are capable of upsetting more cells.

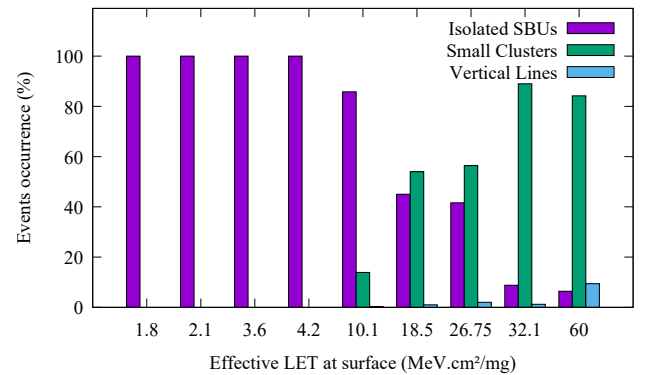


Fig. 7. Ratio of event type occurrence for different LETs.

Tests under proton irradiation presented the same types of failure of the ones with heavy ions. The errors were identified in the experiments with the solid '0' pattern. No bit flip occurred when a solid '1' were used. At an energy of 50.8 MeV and fluence of 8.8×10^{10} cm⁻², were identified 55 isolated SBUs, one small cluster (2 lined up SBUs) and one VL. At 101 MeV and fluence of 5.8×10^{10} cm⁻², occurred 38 isolated SBUs and 1 small cluster (2 lined up SBUs). For an energy level of

200 MeV, at a fluence of $1 \times 10^9 \text{ cm}^{-2}$, occurred 7 SBUs and 1 small cluster (2 lined up SBUs) and at a fluence of 4×10^9 were identified 4 isolated SBUs. However, at a fluence of 1.1×10^{11} , occurred 45 isolated SBUs, 2 small clusters (respectively, 2 lined up SBUs and 3 lined up SBUs) and 4 VLs.

B. Static Data Register Mode Test

During this test, a checkerboard or a solid '1' pattern was written on one page of the memory. Then, instead of reading the memory, the sequence command was interrupted in order to keep the data stored on the data registers. Subsequently, the memory was irradiated, and a reading operation was finally performed to check the data register.

Tests under proton irradiation at energies of 50.8 and 101 MeV resulted in 13 and 10 SBUs respectively. Concerning the runs at 200 MeV, a fluence variation from 7.48×10^8 up to 1.01×10^{10} was achieved, resulting in different amounts of SBUs that increased with the increase of the fluence.

Tests under heavy-ion irradiation were carried out at LETs of 1.8, 2.1, 3.6, 4.2, 10.1, 18.5, 32.1 and 60 $\text{MeV.cm}^2/\text{mg}$. The acquired results can be classified into two groups. The first group is characterized by the detection of few errors, while the other is characterized by the failure of the entire data register (i.e., 8192 words).

Irradiation at an LET of 1.8 and 2.1 $\text{MeV.cm}^2/\text{mg}$ resulted in no errors, whether using the checkerboard or solid '1' pattern. At 3.6 and 4.2 $\text{MeV.cm}^2/\text{mg}$ few errors (between 1 and 6 failing words) started to appear, however, there was no occurrence of an entire fault in the data register. From a let of 10.1 $\text{MeV.cm}^2/\text{mg}$ upwards, the errors involving an upset of the entire data register began to appear.

In the first type of failure (sparse errors in the data register), most of the failing words presented only one bit in error with exceptions in:

- 1) at 4.2 $\text{MeV.cm}^2/\text{mg}$, one word had 3 bit flips.
- 2) at 10.1 $\text{MeV.cm}^2/\text{mg}$, one word had 2 bit flips.
- 3) at 18.5 $\text{MeV.cm}^2/\text{mg}$, seven words had 2 bit flips and one word had 5 bit flips.

Considering the tests with the buffer just partially failing, the word cross section follows a Weibull curve, as depicted in Figure 8.

Similar experiments testing the data register were made by [11] on another NAND Flash part, which found a cross section an order of magnitude lower than evidenced by our tests.

Concerning the entire data register failing, this event occurred twice on the six runs at a LET of 10.1 $\text{MeV.cm}^2/\text{mg}$, five of the eight runs at a LET of 18.5 $\text{MeV.cm}^2/\text{mg}$, and once out of the three runs at 60 $\text{MeV.cm}^2/\text{mg}$. A closer look at the number of bit errors per word (8 bits), 4 bits were upset in most words when using a checkerboard pattern. This can be seen in Figure 9 which shows data from a test using an LET of 18.5 $\text{MeV.cm}^2/\text{mg}$; conversely, tests with a solid '1' pattern returned errors in all bits of all words. These errors tend to lead to the conclusion that during the irradiations, the control logic ruling the reset function of the data register produced unwanted asynchronous resets and all bits were set to

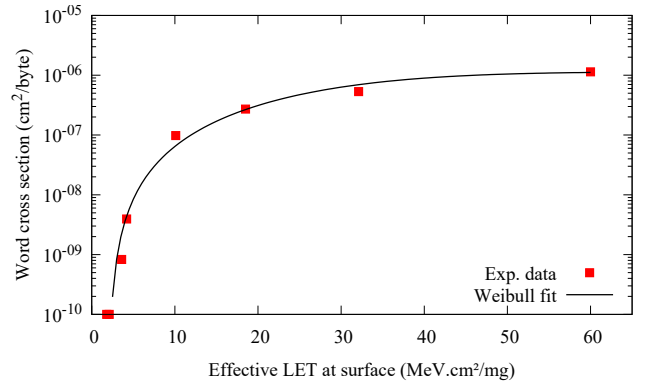


Fig. 8. Word cross section of the data register calculated by dividing the number of failing words by the fluence and the buffer word size (i.e., 8192 words). The LET threshold was guessed at 2 $\text{MeV.cm}^2/\text{mg}$ in order to fit the data with a Weibull curve. The Weibull parameters used are: $W = 31$, $S = 2.1$, $\sigma_{sat} = 1.14 \times 10^{-6} \text{ cm}^2/\text{byte}$, $LET_{th} = 2 \text{ MeV.cm}^2/\text{mg}$.

'0'. As mentioned in the memory datasheet, a reset command to clear the data register content exists, supporting the above assumption.

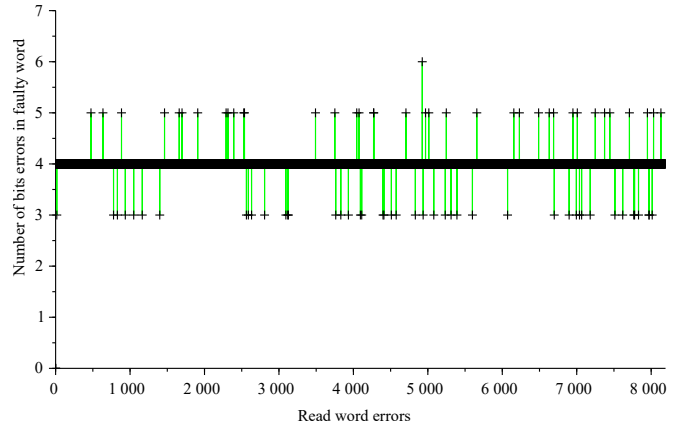


Fig. 9. Number of data register bits falling in each failed word, in static mode, using a checkerboard pattern, at a surface LET of 18.5 $\text{MeV.cm}^2/\text{mg}$.

Concerning the errors with 3, 5 and 6 bit flips in some words within the full faulty data register, this can be explained with the time occurrence of the faulty data register reset. When the reset occurs closer to the beginning of the irradiation, all data register cells are set to '0', and further irradiation generates other bit flips that modify the error pattern within the words. Conversely, the closer the faulty reset is to the end of the irradiation, the more regular the error pattern is. It happens with 8 bit flips for solid '1' and 4 bit flips for checkerboard pattern data background.

IV. CONCLUSION

Effects from heavy-ion and proton irradiation in a Micron SLC NAND Flash were analyzed. Test campaigns results presented different kinds of failures. Tests in static mode showed vertical lines of errors that affects all pages of a sequence of blocks. Also, Isolated SBUs and small clusters

of errors were identified, it is worth noting that these events showed an intermittent behavior in consecutive read operations, exposing recoverable V_{th} shifts due to trapping charges [11]. The memory SEU and raw errors cross sections under heavy-ion irradiation were determined in a range from 1.8 up to 60 MeV.cm²/mg, and proton irradiation results were also described.

Static tests on the data register allowed characterizing the sensitivity of its register as well as observing the occurrence of unwanted reset events that resulted in a complete failure in the data register. A word cross section as a function of LET was defined from the results without a reset event.

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