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Fast and Ultra-Clean Approach for Measuring the Transport Properties of Carbon Nanotubes

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In this work, a fast approach for the fabrication of hundreds ultra-clean field-effect transistors (FETs) is introduced, using single-walled carbon nanotubes (SWCNT). The synthesis of the nanomaterial is performed by floating-catalyst chemical vapor deposition (FC-CVD), which had been employed to fabricate high-performance thin-film transistors (TFTs). Combined with palladium metal bottom contacts, the transport properties of individual SWCNTs are directly unveiled. The resulting SWCNT-based FETs exhibit a mean field-effect mobility, which is 3.3 times higher than that of high-quality solution-processed CNTs. This demonstrates that the hereby used SWCNTs are superior to comparable materials in terms of their transport properties. In particular, the on-off current ratios reach over 30 million. Thus, this method enables a fast, detailed and reliable characterization of intrinsic properties of nanomaterials. The obtained ultra-clean SWCNT-based FETs sheds light on further study of contamination-free SWCNTs on various metal contacts and substrates.

1. Introduction

Low-dimensional carbon allotropes and hence also the CNTs play an important role in nanotechnology.[1] In particular, their low effective mass with the corresponding high carrier velocity, make CNTs and graphene one of the most ideal electron transport systems available.[2] In addition to fundamental transport studies about the novel quantum phenomena[3–7], tremendous efforts have been put into the application of CNTs as next-generation electronic devices.[2,8–11] One of the important achievements in CNTs-based electronics has been the fabrication of ultraclean devices.[1,7,12,13] In such devices, the nanotubes are not exposed to any fabrication chemicals, thereby retaining their pristine material quality. The corresponding transport experiments immediately show better reproducibility. However, the fabrication of these devices requires either high temperature, or sophisticated positioning instruments, or both. To this end, these conditions prevent ultraclean devices from being used as a routine characterization method for pristine nanomaterials.

FC-CVD is a synthesis method known to produce high-quality SWCNTs[14–16] for TFTs with high mobility.[9,17] During the production in a FC-CVD reactor, the SWCNTs are carried by a clean carrier gas, thus avoiding the exposure to any fabrication chemicals. However, in contrast to the extensively investigated solution-separated[18–21] and substrate-grown[22–27] CNT-based FETs, no such device has ever been fabricated directly from FC-CVD grown nanotubes. Furthermore, to the best of our knowledge there has not been an established method to explore their transport properties as single-CNT-based devices. Up until now, the transport property of FC-CVD SWCNTs remained unknown. Therefore, the question still remained, whether FC-CVD produces rather defective CNTs as it is the case in solution processes, or defect-free CNTs as in supported CVD processes.[3–6,22–27]

To electrically characterize the FC-CVD grown SWCNTs, a specific process has been developed for the fabrication of ultra-clean SWCNT-based FETs. This method takes advantage of the FC-CVD process, supported by the clean carrier gas, which combines the SWCNT

synthesis with FET fabrication, while maintaining ultra-cleanness. This one-step technique with the link within the process gives far more freedom of substrate choice, as well as the choice of channel materials, highlighting the importance of this study. As a result, palladium contacts[12] are used to obtain Ohmic contact for intrinsic mobility measurements, which reveals the transport properties of FC-CVD-grown SWCNTs. In addition to that, an effective simulation method for density control has been developed, which ensures successful fabrication. This method is faster and has higher throughput than previously reported ultraclean methods, which allows the fabrication of hundreds of devices from as-synthesized SWCNTs within a total duration of 3 hours. Hence, this improvement reduces not only the fabrication workload, but also enables a reliable routine for device characterization of such nanomaterials.

2. Results and discussions

2.1. Batch fabrication of ultraclean devices

Figure 1a shows the fabrication process of the test chip throughout this work. In the first step, arrays of contacts are prefabricated, using standard photolithography and lift-off techniques. This results in a test chip, consisting of a 20 row by 50 column array of contacts, which act as bottom contacts for the subsequently deposited FC-CVD CNTs. Hence, the chip is referred to as the bottom-contact array. Numerous FETs can be formed from these pairs of contacts after the deposition of SWCNTs. An optical micrograph of the prefabricated contact array is shown in Fig. 1c and a scanning electron micrograph of an as fabricated FET channel is shown in Fig. 1d. In the fabrication process, the SWCNTs are grown inside the FC-CVD reactor with carefully controlled synthesis conditions. The as synthesized nanotubes are carried to the outlet of the reactor by the carrier gas and deposited directly onto the bottom-contact array. A thermophoretic precipitator[28] has been used, which allows to keep the substrate at near-ambient conditions and the SWCNTs to be deposited directly from the outlet of the reactor.

Thus, as already mentioned, this deposition process is free of chemicals contaminants and high temperatures can be avoided, ensuring ultra-cleanness and compatibility with various substrates. After the deposition of SWCNTs, the substrates were annealed to improve the SWCNT-metal contacts. Subsequently, the transport characteristics have been analyzed, using a probe station (**Figure 1b**).

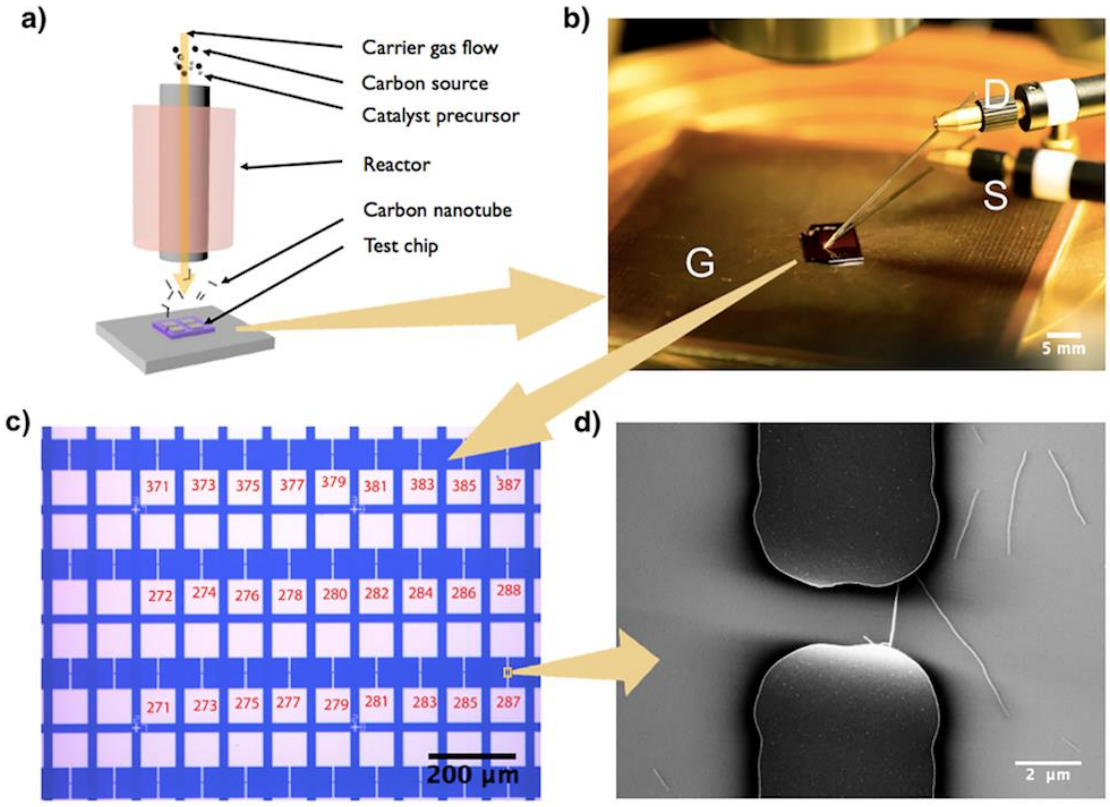

Figure 1. Device fabrication and characterization. (**A**) Schematic of the solution-free synthesis and device fabrication procedure using FC-CVD SWCNTs. CNTs are synthesized and deposited onto the test chip with pre-patterned contacts. (**B**) Image of a test chip placed on a probe station for electrical characterization. Two electrical probes connect to the source and the drain contacts respectively, a conductive plate connects to the silicon substrate from the bottom, serving as a commonly used back gate. (**C**) Optical micrograph showing one randomly chosen section of the test chip. The red numbers indicate the serial for addressing a single

SWCNT device, enabling retrieval of devices by their serial number. (**D**) A micrograph of a working device channel with one SWCNT bridging the metal contacts, taken with a Scanning Electron Microscope (SEM). The designed channel length is 2 μm. Nanotubes are deposited on top the of contacts.

2.2. Preliminary electrical characterization of CNT-based devices

The preliminary characterization of all 1000 pair of contacts on one chip can be done within 12 hours on a semiautomatic probe station. Transfer curves (drain current (I_d) versus gate to source voltage (V_{gs}) curve) were measured for each pair of contacts. The on-current (I_{ON}) and the off-current (I_{OFF}) were extracted from each transfer curve. I_{ON} was defined to be the maximum measured drain current (I_D, under a source-drain bias (V_{ds}) of -1 V unless otherwise specified), while I_{OFF} is defined as the minimum of $|I_D|$.[29] A device was considered 'working', when I_{ON} > 10 pA, and a working device was further categorized into semiconducting (I_{ON}/I_{OFF} > 100, as shown in **Figure 2a**) or metallic (otherwise, as shown in **Figure 2b**). A small number of defective devices (typically 0~5 for each chip), either short-circuited (I_{ON} > 1 mA) by lift-off residue or with a leaky dielectric material (I_g > 10 pA), were observed in some cases and excluded from further analysis.

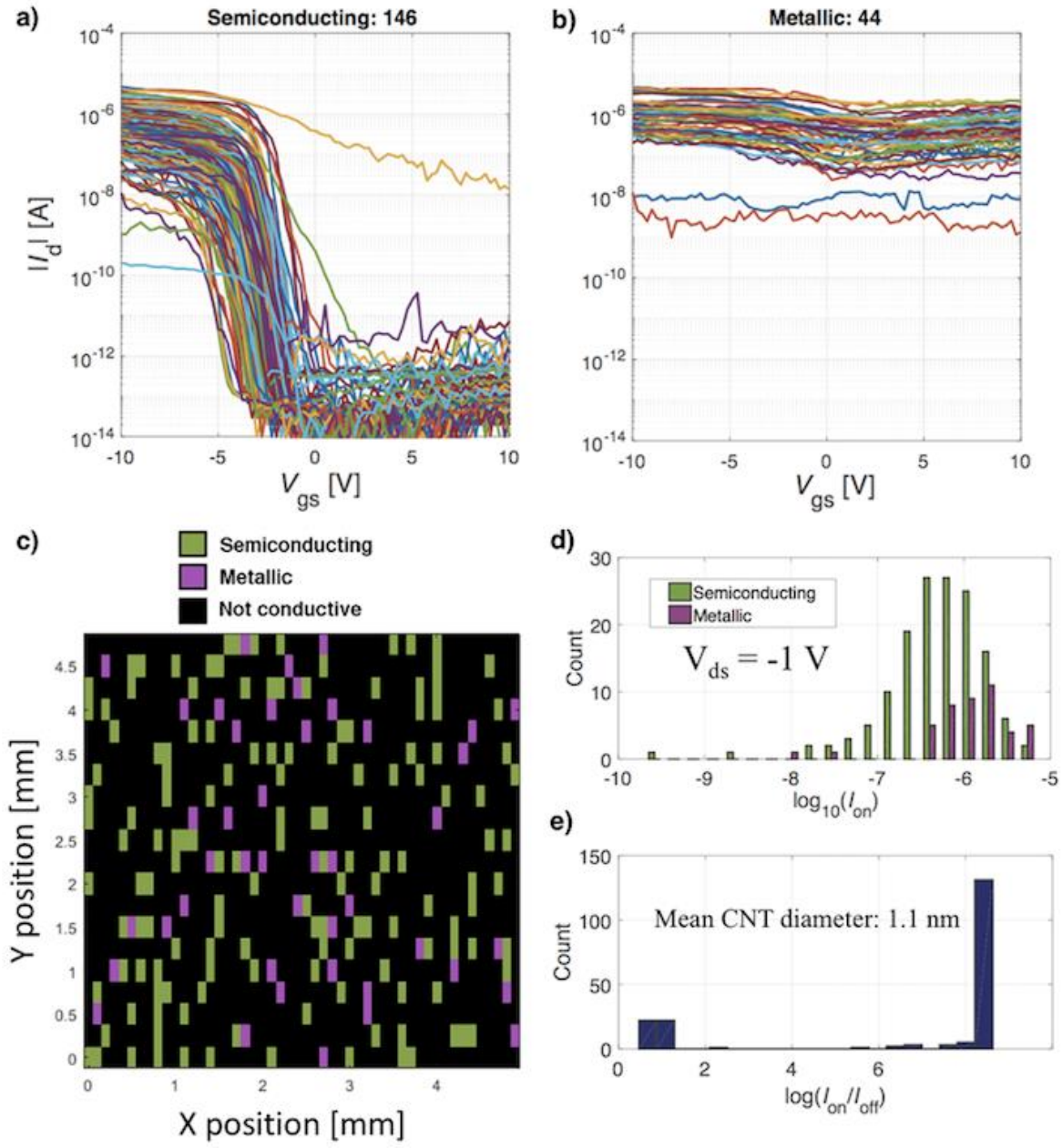

Figure 2. Experimental results from one array of 1000 devices. Transfer curves of semiconducting (A) and metallic (B) devices with V_{ds} = -1 V. (**C**) Visualization of the measured type of 20 by 50 devices. Operating devices are observed evenly over the 5 mm^2 active test area. Black cells denote devices with I_{ON} less than 10 pA. (**D**) The distribution of I_{ON} for semiconducting (green) and metallic (purple) devices. (**E**) The distribution of I_{ON}/I_{OFF} ratios. A clear distinction between semiconducting devices and metallic devices can be observed in this sample with 1.1 nm-mean diameter CNTs from a CO reactor, indicating that semiconducting and metallic devices can be clearly distinguished by I_{ON}/I_{OFF}.

Figure 2 shows the preliminary characterization results of one test chip, fabricated using FC-CVD SWCNTs with a mean diameter of 1.1 nm.[16] Out of 1000 pairs of contacts, 144 semiconducting devices and 44 metallic devices were recognized on the bottom-contact array. The mean I_{ON} for V_{ds} = -1 V bias voltage was 0.70 μA and 1.43 μA for semiconducting and metallic devices, respectively.

The I_{ON}/I_{OFF} ratios of working devices present a clear bimodal distribution indicative of metallic and semiconducting devices (**Fig 2e**). I_{ON}/I_{OFF} may be inaccurate for values over 10^6, due to the fast integration time in the preliminary characterization. The ratio of the number of semiconducting devices over the total number of working devices (device ratio) is of particular interest, since the ratio can be used to indicate the percentage of semiconducting CNTs among the whole population.[27] Due to the random CNT deposition procedure in this experiment, the working devices and their electronic types are randomly distributed throughout the test chip (as shown in **Fig 2c**). However, according to the law of large numbers[30], when the number of working devices is statistically significant, this ratio will stabilize and can serve as a reliable means of characterizing the deposited CNTs (see **Fig 3e**).

2.3. Effect of random deposition on the reliability of this method

The effects of the random CNTs deposition process on the repeatability and precision of the results were investigated using Monte Carlo simulations.[31,32] In these simulations, CNTs were modeled as line segments with uniformly distributed orientations, positions and log-normally distributed lengths (as shown in **Figure 3a** and **3b**). The length distribution was based on previous studies[33], to follow a log-normal distribution: $X = e^{\mu+\sigma Z}$, where μ and σ are two parameters of the log-normal distribution related to mean and deviation and Z is a standard normal variable. The probability density function is thus $f_X(x) = \frac{1}{x} \cdot \frac{1}{\sigma\sqrt{2\pi}} \exp\left(-\frac{(\ln x-\mu)^2}{2\sigma^2}\right)$. With these assumptions, the CNTs population with a given density and distribution parameters

(characterized by μ and σ, which are extracted from actual CNT samples, characterized by SEM) can be effectively simulated with the probability of forming a working device.

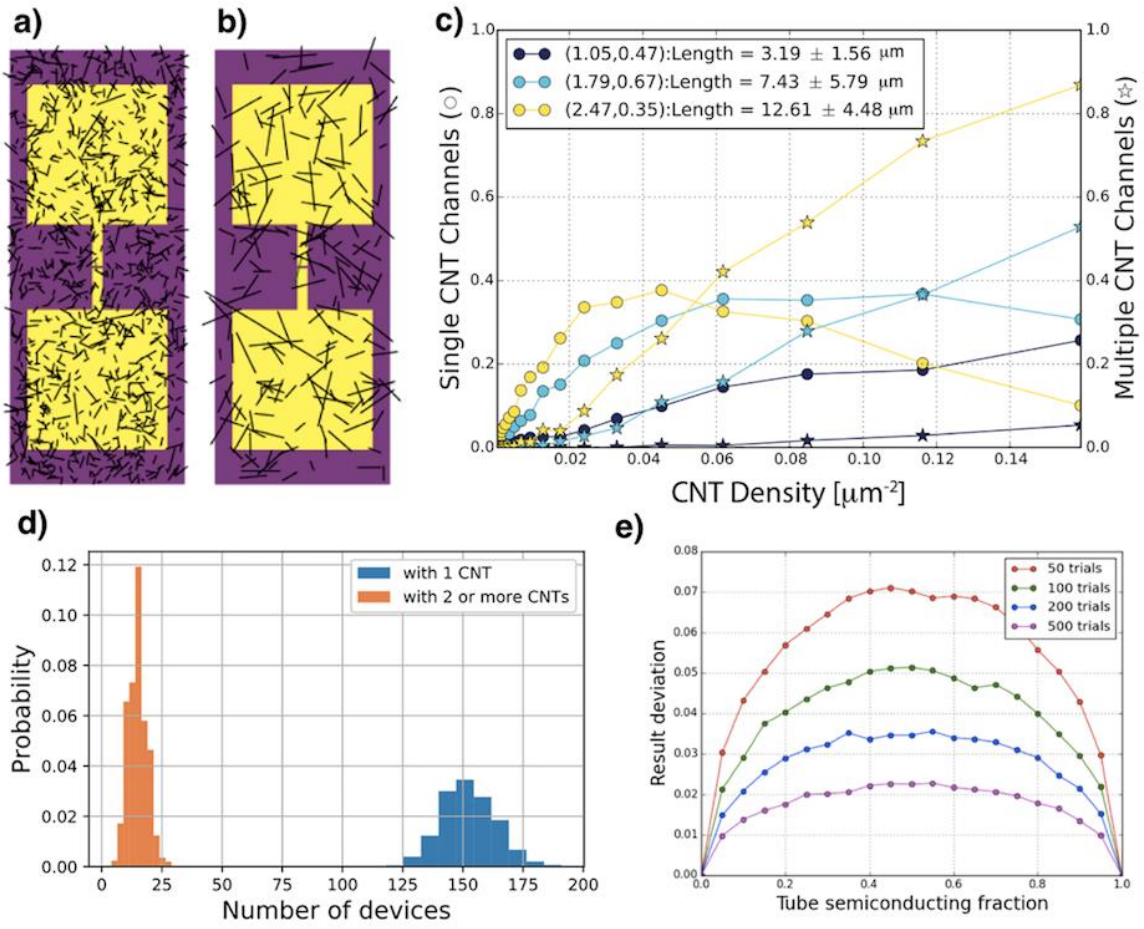

Figure 3. Determination of the reliability and precision of this method. (**A**), (**B**) Monte Carlo simulation of CNT deposition with two different CNT length distributions. (**C**) Based on the simulation, the probabilities of depositing a single tube or multiple tubes in a channel are dependent on both, CNT density and CNT length distribution. This implies the need to measure the CNT length distribution first, in order to get an appropriate number of working devices. The left Y axis represents the fraction of single-CNT channels (circle) and the right axis the fraction of multiple-CNT channels (star) among all devices on the chip. The legend shows lognormal parameters (μ, σ) along with the mean length ± standard deviation. (**D**) The distribution of the number of working devices at a typical density. The deviation in the number of working single-

CNT devices is around 20 under a typical configuration, which means a sample size of over 150 can be obtained on a single chip without an unacceptably high fraction of multiple-CNT devices. (**E**) The simulated precision of the method characterized by the standard uncertainty as a function of semiconducting ratio of underlying CNTs with different sample sizes. For 200 working devices, the standard uncertainty is less than 4%.

A CNT deposition simulation is carried out for 1000 devices, resulting in the number of single-CNT channels and the number of multiple-CNTs channels. These two numbers are important, since it is preferable for most of the channels to be single-CNT channels in terms of individual nanotubes characterization. Performing a series of CNTs deposition simulations with varying CNTs density can advise on the number of working devices (**Figure 3c**), obtained from a specific CNT length distribution. The number of single-CNT channels first increases with the density of deposited CNTs, then decreases as more channels become occupied by multiple CNTs. The number of working devices is well predicted by this simulation. Thus, the device placement simulation is useful for determining the targeted CNTs density. The simulation indicates that the optimal nanotube density is far below the percolation threshold $\rho_{min} = \frac{5.64}{\langle L_{CNT} \rangle^2}$[34]34], meaning that the deposited CNTs do not form a conductive network. Thus, there is no need to etch away the CNTs, as it is performed in percolation thin-film transistors.[9,17] The repeatability of the number of working devices can be investigated by performing the CNT placement simulation for 1000 times (**Figure 3d**), obtaining the distribution of working device numbers. As the result shows, 150 to 220 single-CNT-channel devices can be fabricated with a 95% chance, while obtaining simultaneously only around 25 multiple-CNT-based devices (**Figure 3e**). Hence, the repeatability of this method for obtaining hundreds of devices is practically acceptable.

The key parameters for a characterization method are its precision and accuracy. The standard uncertainty (standard deviation of parallel measurement results) of the device ratio mentioned above, is dependent on the number of working devices, *i.e.* the sample size in the experiment. For a typical experiment with around 200 working devices, the standard uncertainty is less than 4% (**Figure 3e**). To experimentally illustrate the precision of this method, three different densities on three different replicas of the same array design and same synthesis condition have been deposited. The first sample has 367 devices identified as semiconducting and 91 devices as metallic, with the semiconducting fraction of 80.1%. The second sample has 146 semiconducting and 44 metallic devices, with the fraction of 76.8%. The third sample has 31 semiconducting and 6 metallic devices, with the fraction of 83.8%. Although the number of devices differs, the ratio remains stable within the calculated error range (**Figure 3e**). This precision number also works with other Bernoulli-trial-based characterization methods, such as electron diffraction and Raman spectroscopy for identifying the ratio of semiconducting devices. For a more detailed explanation, see supplementary information (Figure. S2-S4). As pointed out in previous studies,[20] such a medium-scale device fabrication method is not enough for measuring the semiconductor enrichment of highly purified solution-processed CNTs. However, this method is precise enough to detect selective treatment conditions for FC-CVD SWCNTs.

The accuracy of a metrological method is determined by how close the result is to the reference value. In the case of the device ratio, the reference value should be the actual percentage of semiconducting CNTs of all the CNTs deposited. However, an accurate measurement technique for the actual percentage value in the experiment has not been developed, yet. The closest reference value is the semiconducting fraction from electron diffraction data of a certain synthesis condition, which accuracy is also not exactly known.[16] The device ratio is different from the electron diffraction ratio (76.8% to 83.8% versus 67%).

Nevertheless, several factors that contributed to the discrepancy between the device ratio and the percentage of semiconducting SWCNTs has been identified within this work. First, the presence of channels with more than one SWCNT would generate a negative bias to the ratio and affect the detailed characterization. Fortunately, the multiple-SWCNTs devices can be limited to a small percentage by controlling the SWCNTs density. The multiple-SWCNTs channels can also be identified by SEM and excluded from further analysis. The effect of multiple-SWCNTs in one bundle should be similar to multiple-SWCNTs channels. Therefore, the effect of bundles can be minimized by using only individual-SWCNTs in this experiment.[15] The second factor is the existence of junction devices. This contributes to a positive bias of the device ratio and is believed to be the main cause of the discrepancy. The third factor is that the method tends to capture more longer-SWCNTs rather than random sampling, which can be verified by the SWCNTs placement simulation (see supplementary material S1). This factor would contribute to a bias, for example, if the semiconducting SWCNTs are on average longer than the metallic ones. Further efforts in synthesis and characterization are needed to resolve this issue.

Nevertheless, the device ratio is a useful indicator for the semiconducting enrichment of a FC-CVD SWCNTs population. Especially, when the metallic fraction is still significant, as already used in earlier reports on other CNT types.[20,27]

2.4. Unveiling the transport properties of FC-CVD SWCNTs

In this part of the manuscript, the focus will be on the semiconducting CNTs-based device studies. The hereby presented transistor array method is compatible with various types of FC-CVD CNTs. To illustrate the compatibility, larger-diameter FC-CVD SWCNTs(d ~ 1.5 nm), grown with ethylene as the carbon feedstock, have been used.[35] In the literature, the mean diameter of SWCNTs for measuring mobility is 1.5 nm or larger.[18,19] To have a reasonable

comparison of carbon nanotube quality to previous studies, the FC-CVD SWCNTs with a 1.5 nm diameter were used for further analysis.

The surface morphology of these devices was studied with an atomic force microscope (AFM, Veeco Dimension 5000, Switzerland; operated in tapping mode). As shown in **Figure 4a**, no fabrication process contamination could be observed on the silicon oxide surface. A number of devices exhibit I_{ON}/I_{OFF} of over $10^{7.5}$ (**Figure 4b**), which is larger than the values reported previously.[19,22]

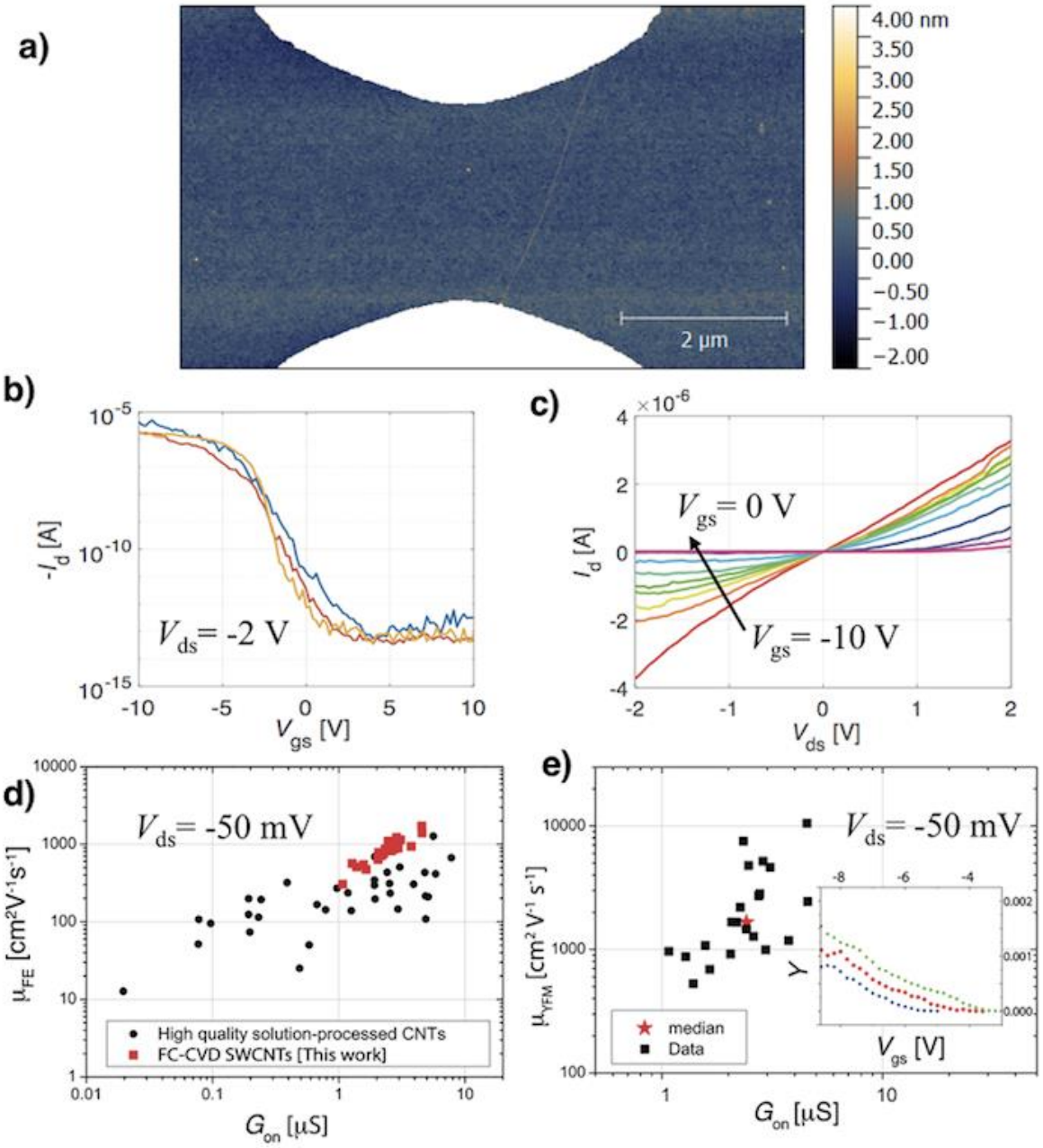

Figure 4. Electrical characterization of devices and imaging of device channel. (**A**) AFM image of the device morphology, signifying the cleanness of the device. This cleanness ensures a reliable characterization of intrinsic properties. (**B**) Typical transfer curves with I_{ON}/I_{OFF} higher than $10^{7.5}$, indicating very low leakage currents in these SWCNTs-based transistors. (**C**) I_D *vs.* V_{SD} curves for various V_G, indicating Ohmic conduction of the device. (**D**) Field-effect mobility statistics of SWCNTs (mean diameter = 1.5 nm) reveals the mean mobility to be 866 $cm^2V^{-1}s^{-1}$. It is 3.3 times higher than that of high-quality solution-processed CNTs in the reference.[19] (**E**) Y-function method of the same set of SWCNTs reveals intrinsic mobility close to the theoretical limit[24], suggesting favorable CNT quality. Inset: three devices with different I_{ON} and threshold voltages, but similar slope of Y-V_{gs} curves, which indicates similar extracted mobility.

One of the most widely used metrics for describing semiconductor quality is the charge carrier mobility μ. Particularly, it is valid for device channel lengths, longer than the carrier mean free path (long channel devices).[2] To accurately evaluate the intrinsic CNT mobility, the contacts of CNTs to the metal electrodes are required to have linear I_D-V_{DS} characteristics (Ohmic, as shown in **Figure 4c**). Thus the devices that deviate from linear conductivity due to a small CNT diameter[22] or other non-idealities have been excluded. Devices with more than one CNT in the channel, indicated by SEM observation, were also excluded from the analysis.

First, the field-effect mobility of these devices has been extracted by the regular peak trans-conductance method:[18,19,24,25]

$$\mu = \frac{L}{c_G V_{DS}} \frac{dI_D}{dV_{GS}} \quad (1)$$

$$c_G = \left[c_q^{-1} + \frac{\ln(\frac{2h}{r})}{2\pi\epsilon} \right]^{-1} \quad (2)$$

Where c_G is the gate capacitance per unit length in a rod-to-plate geometry, h is the oxide thickness, r the CNT radius, ε is the dielectric constant of the oxide layer, and c_q = 0.4 nF m^{-1} is the quantum capacitance per unit length. The channel length L is assumed to be the designed length of 2 μm. This value would contribute to some under-estimation of the mobility, since the actual channel lengths along the CNTs are often longer, if the random alignment of the nanotubes and the non-ideality of photolithography are taken into account, as shown in **Figure 4a**.

The extracted mobility of 21 Ohmic semiconducting devices is 866 ± 333 cm^{2}V^{-1}s^{-1}. The mean mobility is 3.3 times higher than that of high-quality solution-processed SWNT-based transistors (200 cm^{2}V^{-1}s^{-1}), measured using similar methods.[19] The data from FC-CVD CNTs overlaps with that from solution-processed CNTs in the G_{ON}-μ_{FE} plot (G_{ON}= I_{ON}/V_{DS}). Additionally, it also overlaps with the 'higher mobility' region of the scatter plot of solution processed CNTs, as shown in **Figure 4d**. The data is more uniform and exhibits an obvious linear trend, in accordance with the classical definition of charge carrier mobility $\mu = \sigma/q$ [25], where σ is the conductivity and q is the charge density. The linear G_{ON}-μ_{FE} data indicates a more uniform carrier concentration and contact resistance in FC-CVD CNTs than in solution-processed CNTs. The highest μ_{FE} for these devices is similar to the solution processed CNTs (1719 cm^2/Vs *versus* 1380 cm^{2}V^{-1}s^{-1}) found in the reference,[19] suggesting that the best solution-processed CNTs can be similar to FC-CVD CNTs. However, due to sonication or other treatment processes, a large proportion of solution processed CNTs exhibit only inferior mobility. Furthermore, the extracted mobility of 866 cm^2/Vs is also in agreement with the mobility of FC-CVD CNTs in percolation TFTs, using a rigorous capacitance model (1027 cm^{2}V^{-1}s^{-1}).[17] Unlike solution-processed CNT-based devices, which mobility is limited by their defected lattice structure[18], the mobility of FC-CVD CNT-based TFTs is more limited by external factors, such as nanotubes density and CNT-CNT contact. Thus, there is greater potential for improvement.

Although the peak trans-conductance method already provided concrete evidence of good FC-CVD SWCNTs quality, the mobility obtained in this way is affected by CNT-metal contact resistance. Comparatively short channel of the device[24] has also an adverse effect on the obtained mobility. The influence of contact variation can be excluded using the Y-function method (YFM)[18] and a more intrinsic measure of the nanotube quality can be obtained:

$$Y = \frac{I_d}{\sqrt{g_m}}\sqrt{V_{DS}G_m}(V_{GS} - V_T), g_m = \frac{dI_D}{dV_{GS}}. \quad (3)$$

The intrinsic field effect mobility (μ_{YFM}) can be extracted from the slope of the Y–V_{GS} curve: $\mu_{YFM} = \frac{G_m L}{c_g}$, where the definitions of c_q and L are the same as in Eq. 1 and 2 for the peak-transconductance method. The threshold voltage V_T is obtained from the x-axis intercept of the Y-function plot.

The μ_{YFM} is uniformly higher than the values, obtained by the peak trans-conductance method for all investigated devices, with a mean of 2674 $cm^2V^{-1}s^{-1}$ and the maximum value of 10518 $cm^2V^{-1}s^{-1}$, as shown in **Figure 4e**. This extracted mobility is comparable to other reported resultsfor aligned[36,37] and kite[24] CVD CNTs at room temperature. According to the theoretical analysis by Zhou *et al*., 2674 $cm^2V^{-1}s^{-1}$ for 1.5 nm mean diameter of the nanotubes at room temperature on SiO_2 substrate is close to the theoretical limit. The mobility in this case is mainly limited by scattering from the substrate.[24]

From the Y-function method, a resistance value (R_s) of the individual FC-CVD SWCNTs-based FETs can be extracted. The extracted contact resistance of the above analyzed devices with their means and standard deviations are calculated to be 373 ± 132 kΩ, accounting for the major ON-state resistance in the devices. According to a previous study, using conductive AFM, the resistance along FC-CVD SWCNTs is around 8.7 kΩ μm^{-1}.[31] Which is the major resistance is the CNT-metal contact resistance. This contact resistance is much larger

than the one of the solution-processed CNTs in the CNT-at-bottom geometry (30 ± 20 kΩ)[18], while the ON-state conductance is comparable to other devices of similar CNT diameter.[19,22,24]

It is worth noting that the obtained SWCNTs mobility is significantly limited by the surface polar phonons on SiO_2.[38] A higher mobility can be achieved using either cryogenic temperature or different substrates[39], by suspending the SWCNT or by applying SWCNTs with a larger diameter.[24,25] The mobility in this experiment is obtained in ambient conditions at room temperature on regular SiO_2 substrate. To the best of our knowledge, this shows that the electronic quality of semiconducting FC-CVD SWCNTs is close to the best quality of carbon nanotubes obtained so far.

We would like to point out that this method is not intended for circuit applications at this moment. However, it is proven to be a useful method for inspecting the quality of the SWCNTs. In fact, for integrated circuit (IC) applications, high semiconducting purity, high I_{ON}- and V_T uniformities etc. are required. Thus, single-CNT-based devices are not a good choice. Nevertheless, with the help of this method for optimization of the synthesis conditions, it is possible to obtain better channel materials for thin-film applications.

The ultraclean single-SWCNT-based devices, obtained by this method, can also be used for ongoing investigations in the field of novel quantum-device technology and in-situ studies. The yield of metallic or semiconducting devices can be improved as application might require. One way is introducing SWCNT alignment by gas flow or electric field.[19,40] Another way is tuning the metallic to semiconducting ratio of the source FC-CVD SWCNTs.[41] For applications that tolerate multiple SWCNT channels, such as *in situ* TEM devices, the device yield can be well above 50% (as is indicated in Figure 3c), so far as the density of SWCNTs is below the percolation threshold. In a broader scenario, this fabrication method and simulation technique can be utilized to investigate other nanomaterials in gas- or solution-phase. The key issue is that

both, the nanomaterial itself and the surface of metal contacts need to be clean enough for reproducible and stable electrical conductivity.

3. Conclusion

In this work, a novel method for the fabrication of ultraclean SWCNT-based devices is reported. Hundreds of devices on one single chip offer repeatable and exhaustive inspection of the CNTs distribution, allowing to study not only the typical property, but also the variation range in a single batch. With the help of this method, the superior transport property of FC-CVD SWCNTs has been presented. The I_{ON}/I_{OFF} was shown to reach values higher than $10^{7.5}$. The field-effect mobility is similar to the one of other high-quality CVD-grown CNTs, in particular 3.3 times higher than solution-processed CNTs of similar mean diameter. This indicates that FC-CVD SWCNTs offer the highest electronic quality, compared to other values for CNTs reported in literature. As a result, FC-CVD SWCNTs can by all means be preferred for thin-film applications, where mobility still matters, and for quantum sensors, which require less defect sites.[7]

Furthermore, an effective simulation method has been proposed to obtain the optimal deposition density. Despite the randomness of deposition, the probability for the successful fabrication of 100 single-SWCNT-based devices is higher than 95%. Further, with the presented characterization technique with unbiased sampling of 100 samples, the precision of the obtained value is better than 5%. This limitation also applies to Raman and TEM diffraction, meaning that for higher characterization performance, a larger sample size is needed. Hereby, it is important to emphasize the speed and the throughput of this method, which is by all means an advantage in achieving such high precision.

4. Experimental Section

Synthesis of SWCNT: Thinner SWCNTs (mean diameter: 1.1 nm, length: 3.19 ± 1.56 µm) were grown using a FC-CVD process at 880 ℃ with spark-discharge generated iron particle as catalyst and carbon monoxide (CO, 99%; Oy AGA AB, Finland) as carbon source. A detailed description of the SWCNT growth system has been published earlier.[16]

Thicker SWCNTs (mean diameter: 1.5 nm, length: 12.61 ± 4.48 µm) were grown using the FC-CVD process with ferrocene as the catalyst precursor and ethylene as the carbon feedstock. A detailed description of the SWCNT growth system has been published earlier.[35]

Device fabrication: Device arrays were fabricated on boron-doped p^{++} silicon wafers with a 100 nm thermal oxide layer (Electrokem Oy). The silicon substrate was used as a common back-gate for all devices. Electrical Ti/Pd (5 nm/25 nm) contacts were patterned by photolithography and electron beam evaporation. Then, the deposited chip was annealed in ambient conditions at 200 ℃ for 2 hours.

Device characterization: Electrical characterization was carried out using a Suss Microtech PA150 probe station, equipped with tungsten carbide needles with an Agilent 4156B precision semiconductor parameter analyzer, both controlled by a home-made LabVIEW program.

SEM imaging was performed using Zeiss sigma VP SEM in high vacuum mode.

AFM imaging was performed using Veeco Dimension 5000, operated in tapping mode.

Criteria for statistical analysis: For preliminary characterization, the transfer characteristics of all 1000 devices were carried out. A small number (0~5 on each chip) of defective devices, either short-circuited by lift-off residue (I_{ON}>1 mA) or with dielectric material (I_g > 10 pA), were excluded from analysis. The remaining devices were further categorized into “no CNTs in channel” (I_{ON} < 10 pA), semiconducting CNTs (I_{ON}/I_{OFF}> 100) or metallic CNTs ($I_{ON}/I_{OFF} \leq$ 100).

Ohmic devices were determined by comparing the ON-state conductance under two different drain biases (V_D = -0.05 and V_D = -0.5, ON-state conductance within ±7% to be considered as Ohmic). Devices with more than one CNT in the channel by observation with the help of SEM

imaging were also excluded from the analysis. All Ohmic individual semiconducting devices were included in the calculation of field-effect mobility and contact resistance.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript. N. W., P. L. and E. I. K. proposed the idea of the project. N. W. designed and performed the main experiments and wrote the manuscript draft. P. L. and A. H. participated in the FC-CVD CNT synthesis and deposition. S. A., A. T. K. and N. W. participated in the electrical characterization and data analysis. Y. T. helped with the characterization of the material. P. L., A. L., Q. Z., Y. L. and E.-X. D. participated in the figure processing and manuscript preparation. A. L., Y. O. and E. I. K. participated in the manuscript polishing.
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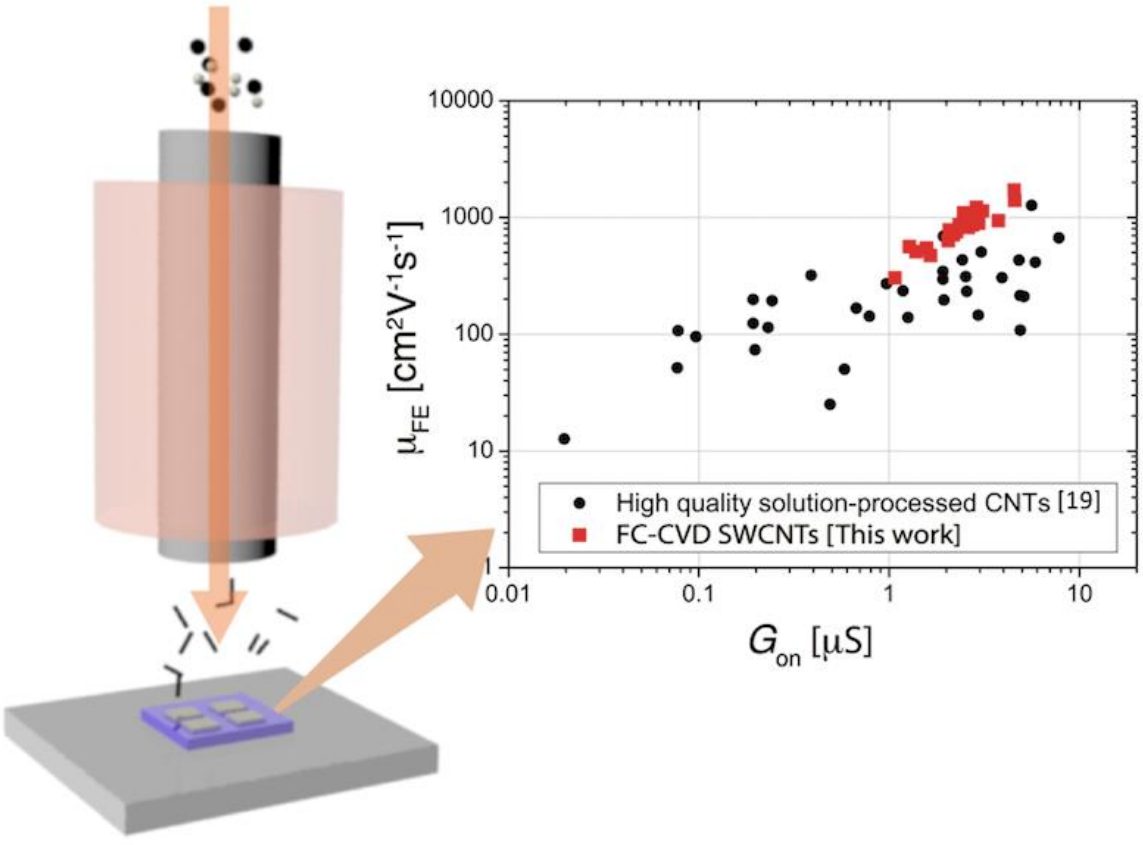
A method was proposed to fabricate hundreds of ultraclean field-effect transistors from floating-catalyst chemical vapor deposition grown single-walled carbon nanotubes. High mobility and on-off ratio were obtained, revealing the high-quality of this type of carbon nanotube among those from other synthesis methods. This method is suitable as a routine for probing intrinsic properties of nanomaterials.

Keyword ultraclean carbon nanotube devices, one-dimensional nanomaterials, charge carrier mobility, bottom contact, floating-catalyst chemical vapor deposition

Nan Wei[*]*, Patrik Laiho, Abu Taher Khan, Aqeel Hussain, Alina Lyuleeva, Saeed Ahmed, Qiang Zhang, Yongping Liao,Ying Tian, Er-Xiong Ding, Yutaka Ohno , Esko I. Kauppinen*[*]

Fast and Ultra-Clean Approach for Measuring the Transport Properties of Carbon Nanotubes

ToC figure

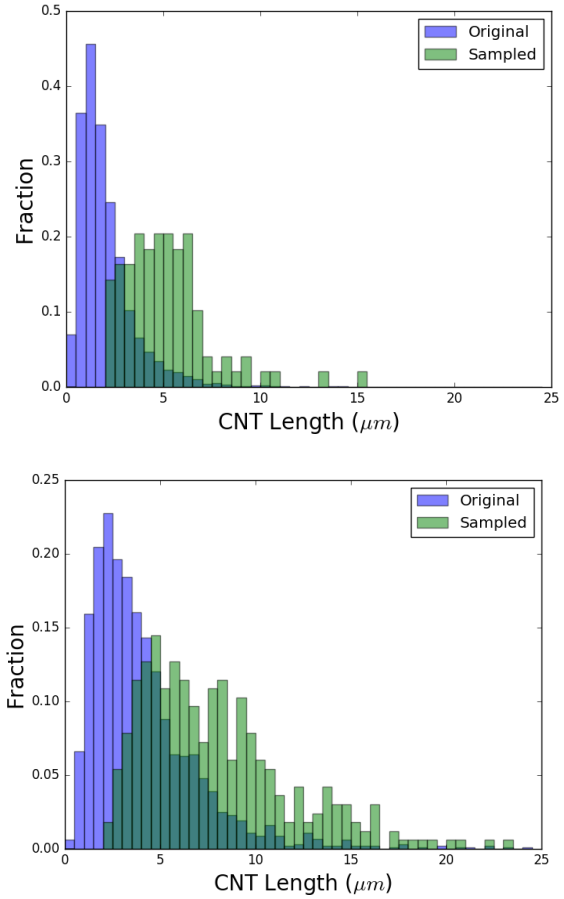


Supporting Information

Fast and Ultra-Clean Approach for Measuring the Transport Properties of Carbon Nanotubes

Nan Wei[*], *Patrik Laiho, Abu Taher Khan, Aqeel Hussain, Alina Lyuleeva, Saeed Ahmed, Qiang Zhang, Yongping Liao,Ying Tian, Er-Xiong Ding, Yutaka Ohno , Esko I. Kauppinen*[*]

S1: Non-uniform sampling toward longer CNT lengths



Simulated length statistics of all carbon nanotubes, deposited on a substrate and CNTs forming FETs of (a) 2 micron mean and (b) 4 micron mean SWCNTs.

Since the SWCNTs must be longer than the channel length to bridge the source and drain, the sampling is selective in terms of tube length. This selectivity can be characterized using the previous model. Simulations reveal that the mean length of sampled tubes is about 2 times of the original deposited CNTs, with the mean length of CNTs being between 2 and 6 μm, and the spread factor of around 0.6.

As a result of this selectivity, the ratio obtained may be different from the one, using other methods. The obtained semiconducting ratio is always higher than after using the TEM diffraction method, which sampling selectivity is not yet clear.

S2: Bayesian analysis of the proportion of semiconducting SWCNTs

For comparison, the outcomes of the measurements reported in this article can be analyzed, as well as any Bernoulli-trial-based characterization method, also in a Bayesian framework. If θ_S is defined as the proportion of semiconducting SWCNTs in a population and, in the absence of *e.g.* a physically based model of why certain values of θ_S would be more likely, we use a flat *Beta(1,1)* distribution as the prior distribution, the posterior distribution for θ_S is[2]

$$p(\theta_S|s) \sim Beta(s+1, n-s+1)$$

after observing *s* semiconducting SWCNTs in *n* trials. Plots of the posterior distributions for the three samples reported here, and for comparison, the electron diffraction (ED) based characterization of similar d = 1.1 nm SWCNTs reported in Mustonen *et al.*, are shown in Fig. S1.

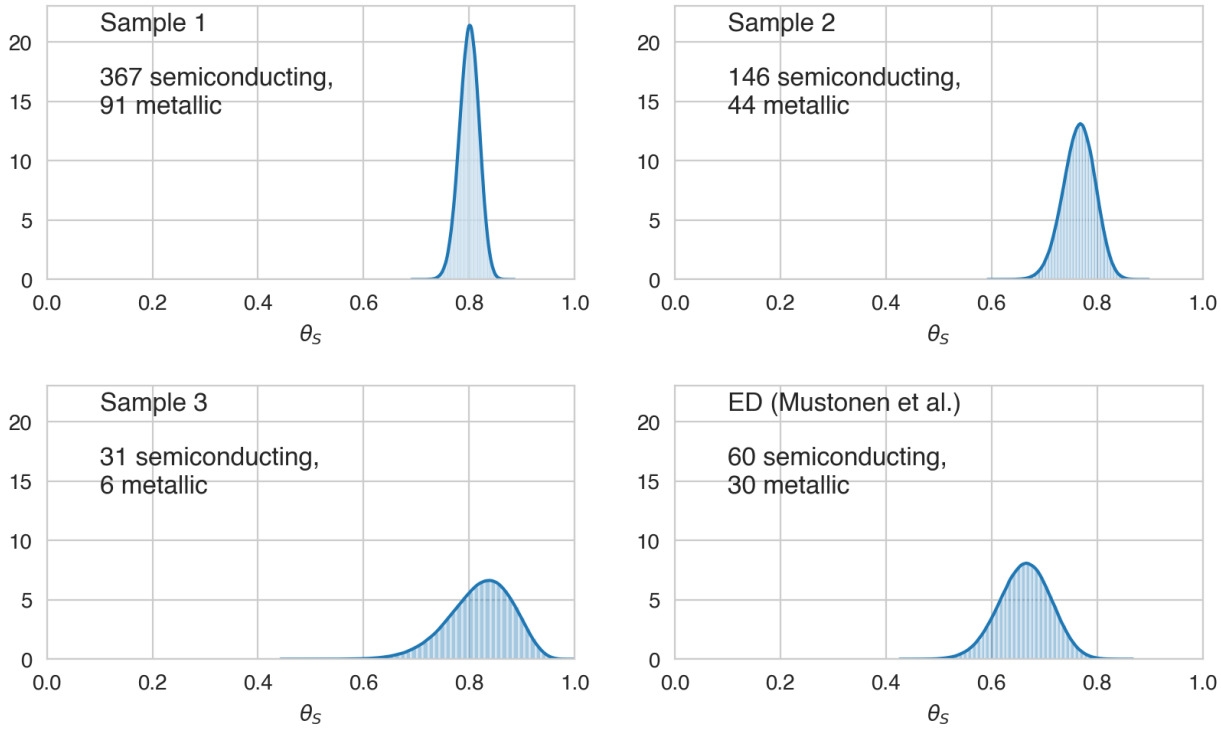


Figure S2. Visualizations of the posterior distributions of θ_s for the three samples reported in the article and the ED based characterization reported in Mustonen *et al.*, using a non-informative prior distribution.

For comparison of multiple samples, their posterior distributions can be summarized through the highest posterior density (HPD) interval, defined as the narrowest interval containing a specific amount of the probability density. The 95% HPD intervals, in correspondence with common statistical practice, for the posterior distributions of θ_S measured from the three samples reported and for the ED based characterization reported in Mustonen *et al.*[1] are shown in Fig. S2. We observe a significant difference (non-overlapping intervals) in the case of Sample 1 and the ED based characterization; possible mechanisms for this difference are discussed in the main article.

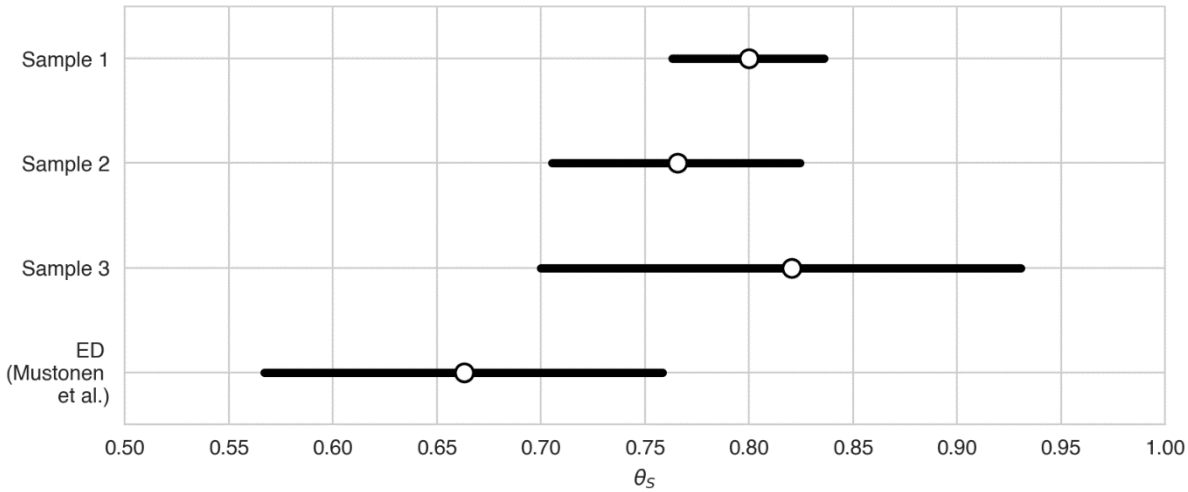


Figure S3. 95% highest posterior density intervals of θ_s for the three samples reported in the article and the ED based characterization reported in Mustonen *et al.*

Because the measured θ_S of individual samples may be biased depending on *e.g.* the density of the deposited SWCNTs, it can also be beneficial to pool the measurements of multiple samples, collected from an individual SWCNT synthesis or post-synthesis treatment condition, using a hierarchical Bayesian model. In this treatment, the sample-wise semiconducting SWCNT proportions θ_S is modeled as conditionally independent given the prior parameters α, β. Following Gelman *et al.*[2], one possibility is to use the reparameterization $\alpha = \kappa\phi$, $\beta = \kappa(1-\phi)$ and use the hyperpriors

$$p(\phi) \sim Uniform(0,1),\ p(\kappa) \sim Pareto(1,1.5),\ \kappa > 1,$$

in which case ϕ represents the population-wide semiconducting SWCNT proportion, out of which the sample-wise proportions θ_S are drawn. Inference from the hierarchical model can be done using Markov Chain Monte Carlo (MCMC) sampling; an implementation of the model in the Stan probabilistic programming language[3] is included below.

```
data {
   int<lower=0> N; // points of data
   int<lower=0> Y[N]; // successes
   int<lower=0> trials[N]; // trial
   int<lower=0> samples; // samples
   int<lower=1,upper=samples> labels[N];
}
parameters {
   real<lower=0, upper=1> phi;
   real<lower=1> kappa;
   vector<lower=0,upper=1>[samples] theta;
}
model {
   phi ~ uniform(0,1);
   kappa ~ pareto(1, 1.5);
   for (i in 1:samples) {
      theta[i] ~ beta(phi * kappa, (1 - phi) * kappa);
   }
```

```
    Y ~ binomial(trials,theta[labels]);
}
```

If data from the samples 1-3 is used to fit the hierarchical model, the parameter κ is not well determined by the combination of the data and the $Pareto(1,1.5)$ hyperprior used, because the limited amount of data cannot constraint the variance in the population enough.[4] Posterior plots of ϕ and κ are presented in Figure S3. Despite this shortcoming, the hierarchical model could be useful in the analysis of outcomes from future studies using a similar experimental setup or another Bernoulli-trial based characterization method, such as ED based characterization from multiple samples of the same synthesis condition.

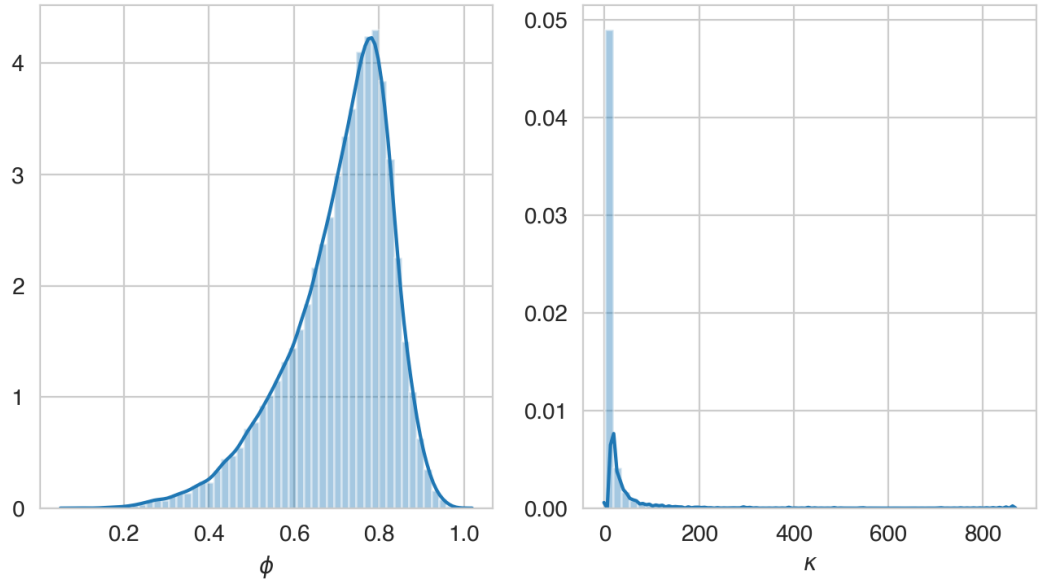


Figure S4. Visualizations of the posterior distributions of the hierarchical model parameters ϕ and κ, using data from the three samples reported in the article.

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