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Enhanced thermally aided memory performance using few-layer ReS$_2$ transistors

ABSTRACT

Thermally varying hysteretic gate operation in few-layer ReS$_2$ and MoS$_2$ back gate field effect transistors (FETs) is studied and compared for memory applications. Clockwise hysteresis at room temperature and anti-clockwise hysteresis at higher temperature (373 K for ReS$_2$ and 400 K for MoS$_2$) are accompanied by step-like jumps in transfer curves for both forward and reverse voltage sweeps. Hence, a step-like conductance (STC) crossover hysteresis between the transfer curves for the two sweeps is observed at high temperature. Furthermore, memory parameters such as the RESET-to-WRITE window and READ window are defined and compared for clockwise hysteresis at low temperature and STC-type hysteresis at high temperature, showing better memory performance for ReS$_2$ FETs as compared to MoS$_2$ FETs. Smaller operating temperature and voltage along with larger READ and RESET-to-WRITE windows make ReS$_2$ FETs a better choice for thermally aided memory applications. Finally, temperature dependent Kelvin probe force microscopy measurements show decreasing (constant) surface potential with increasing temperature for ReS$_2$ (MoS$_2$). This indicates less effective intrinsic trapping at high temperature in ReS$_2$, leading to earlier occurrence of STC-type hysteresis in ReS$_2$ FETs as compared to MoS$_2$ FETs with increasing temperature.

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Recently, two-dimensional (2D) layered materials have attracted significant research interest for memory applications. Thermally assisted non-volatile memories (NVMs) have been demonstrated using monolayer and few-layer MoS$_2$. In several other reports, large hysteresis in transistor transfer curves, normally undesirable for device performance, has been utilized for NVM applications. All of these reports use MoS$_2$ as the channel or as the charge trapping layer. In thermally assisted NVMs, locally generated heat is exploited for switching between different memory states. MoS$_2$ has shown excellent switching characteristics compared to other transition metal dichalcogenides (TMDs). Low off current ($I_{off}$) and a high on/off current ($I_{on}/I_{off}$) ratio (due to a large bandgap) along with a low sub-threshold slope and high effective mass are some of the advantages of MoS$_2$, which make it a desirable switching material for memory applications. Among the TMDs, ReS$_2$ has also garnered significant attention recently since it behaves as decoupled monolayers stacked on top of each other due to the lack of interlayer coupling and weak interlayer registry. Hence, ReS$_2$ remains a direct bandgap semiconductor ($E_G = 1.5$ eV) from monolayer to bulk, showing no direct to indirect bandgap crossover as is shown by other TMDs, making it a preferred material for optoelectronic applications.

With the increasing packing density of field effect transistors (FETs) on a single wafer, high performance ICs can reach an operating temperature (T) of 370–530 K (Ref. 14), making it important to understand and exploit the changes that occur in the properties of 2D materials at high T. Thermally assisted memory is one such application where locally generated heat is exploited to aid the switching between RESET (RST/STATE 0) and WRITE (WR/STATE 1) states. It can enable embedded in-memory computing that has emerged as a key hardware bottleneck for artificial intelligence/machine learning technologies. However, in-memory computing requires more computational power per unit volume of data storage in the RAM and parallel...
This work was previously reported for monolayer MoS\textsubscript{2} FETs.\textsuperscript{1} Here, we report anti-clockwise (ACW) hysteresis at high T. A similar behavior has been previously reported for MoS\textsubscript{2} and MoS\textsubscript{2} as the channel materials. The TMD sheets were mechanically exfoliated (using adhesive blue tape) from bulk crystals on heavily doped p-type silicon substrates with a 280 nm SiO\textsubscript{2} layer on top.\textsuperscript{23,24} Source/drain electrodes were then patterned using electron beam lithography followed by metal deposition. 10 nm Cr and 100 nm Au were used to form source/drain metal contacts with the flakes.

Figures 1 and 2 show the conductance (G) vs back gate voltage ($V_{GS}$) curves for varying T. Figures 1(d) and 2(d) define the RST, RD, and WR operations for the ReS\textsubscript{2} and MoS\textsubscript{2} memories, respectively.

### Table I. Comparison of memory parameters obtained in this work with the previous reports on thermally assisted memory using MoS\textsubscript{2} as the channel material.

<table>
<thead>
<tr>
<th>References</th>
<th>Material</th>
<th>Operating temperature (K)</th>
<th>Operating voltage ($V_{p-p}$)</th>
<th>RST-to-WR window ($\Delta V_{th}/V_{p-p}$)</th>
<th>RD window</th>
<th>Hysteresis type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Monolayer, MoS\textsubscript{2}</td>
<td>490</td>
<td>$-40 \text{ V to } +40 \text{ V}$</td>
<td>0.44</td>
<td>5.5</td>
<td>STC + ACW</td>
</tr>
<tr>
<td>21</td>
<td>Monolayer, MoS\textsubscript{2}</td>
<td>350</td>
<td>$-30 \text{ V to } +15 \text{ V}$</td>
<td>0.50</td>
<td>7</td>
<td>CW</td>
</tr>
<tr>
<td>22</td>
<td>Multilayer MoS\textsubscript{2}</td>
<td>300</td>
<td>$-30 \text{ V to } +30 \text{ V}$</td>
<td>0.1</td>
<td>—</td>
<td>CW</td>
</tr>
<tr>
<td>This Work</td>
<td>Few-layer MoS\textsubscript{2}</td>
<td>400</td>
<td>$-100 \text{ V to } +60 \text{ V}$</td>
<td>0.16</td>
<td>1.9</td>
<td>STC + ACW</td>
</tr>
<tr>
<td>This Work</td>
<td>Few-layer ReS\textsubscript{2}</td>
<td>375</td>
<td>$-100 \text{ V to } +30 \text{ V}$</td>
<td>0.58</td>
<td>7.4</td>
<td>STC + ACW</td>
</tr>
</tbody>
</table>

All the measurements reported in this work start with the FS followed by RS. We observe two significant step-like jumps in the G-$V_{GS}$ plots at high T. The first one occurs during FS at 20 V for ReS\textsubscript{2} [Fig. 1(d)] and at 35 V [Fig. 2(d)] for MoS\textsubscript{2}. The second one occurs during RS at $-76 \text{ V for ReS}\textsubscript{2}$ [Fig. 1(d)] and $-66 \text{ V for MoS}\textsubscript{2}$ [Fig. 2(d)]. As a result STC hysteresis emerges at 373 K and 400 K for ReS\textsubscript{2} and MoS\textsubscript{2}, respectively. These jumps can be prominently observed in the trans-conductance ($g_m$) curves in Figs. S1(a) and S1(b) of the supplementary material for ReS\textsubscript{2} and MoS\textsubscript{2} respectively. Along with the jumps occurring at higher T, a switch from CW hysteresis at RT to ACW hysteresis at higher T can also be observed in the transfer curves for both ReS\textsubscript{2} and MoS\textsubscript{2}.

The changing hysteresis behavior with varying T is shown in Figs. 3(a) and 3(b) via the change in threshold voltage ($V_{th}$) for FS (STATE 1, $V_{FS}^{th}$) and RS (STATE 0, $V_{RS}^{th}$) with T for MoS\textsubscript{2} and ReS\textsubscript{2}, respectively. A transition from CW ($V_{FS}^{th} < V_{RS}^{th}$) to ACW ($V_{FS}^{th} > V_{RS}^{th}$) hysteresis with increasing T can be observed. A larger hysteresis width ($\Delta V_{th} = V_{FS}^{th} - V_{RS}^{th}$) for ReS\textsubscript{2} at much lower T compared to MoS\textsubscript{2} can also be seen. As marked in Figs. 1(d) and 2(d), WR and RST operations are carried out at the end of FS and RS, respectively. A larger $\Delta V_{th}$ implies a larger RST-to-WR window, a desirable feature for distributed processing. This increases the operational T of data centers, resulting in several reliability concerns.\textsuperscript{16,17} Therefore, enabling low T memory operation in 2D materials is timely and relevant. In this study, thermally varying hysteretic gate operation, in few-layer MoS\textsubscript{2} and in few-layer ReS\textsubscript{2}, is studied and compared for memory applications. Four-terminal back gate FETs are used in this study to eliminate the contribution from contact resistance.\textsuperscript{16} Clockwise (CW) hysteresis is observed for both ReS\textsubscript{2} and MoS\textsubscript{2} at room temperature (RT), whereas anti-clockwise (ACW) hysteresis along with step-like jumps in the transfer curves leading to a conductance crossover through the forward sweep (FS, $-100 \text{ V to } +100 \text{ V}$) and reverse sweep (RS, $+100 \text{ V to } -100 \text{ V}$) directions (step-like conductance crossover hysteresis or STC hysteresis) is observed at high T. A similar behavior has been previously reported for monolayer MoS\textsubscript{2} FETs.\textsuperscript{1} Here, we observe this behavior in both few-layer MoS\textsubscript{2} at 400 K and few-layer ReS\textsubscript{2} at 375 K, attributing the RT CW hysteresis to the dominance of native intrinsic traps and the conductance crossover at high T to charge exchange between the p$^+$ Si back gate and gate oxide SiO\textsubscript{2}. The charge can be trapped in the oxide near the 2D channel/dielectric or the back gate/dielectric interface.\textsuperscript{1,19,20} However, the latter is found to be dominating at high T in these systems.\textsuperscript{18} A comparison of this work with previous reports on thermally assisted memory is presented in Table I.

We observe lower operating voltage ($V_{p-p}$), a larger RST-to-WR window, defined as $\Delta V_{th}/V_{p-p}$ (where $V_{th}$ is the hysteresis width), and a larger READ (RD) window for STC hysteresis in ReS\textsubscript{2} devices. Improved memory parameters for ReS\textsubscript{2} FETs at much lower T are attributed to a rapidly reducing effect of intrinsic traps with increasing T. This is verified by T-dependent Kelvin probe force microscopy (KPFM) measurements, which indicate the decreasing work function ($\Phi$) with increasing T.

Figure 1(a) shows an optical image (top) and a 3D schematic (bottom) of back-gated vdP FETs with the ReS\textsubscript{2}/MoS\textsubscript{2} channel. G($S$ vs $V_{GS}$) at $V_{sd} = 2 \text{ V}$ for ReS\textsubscript{2} FET showing the evolving hysteresis width with increasing T at (b) 323 K, (c) 348 K, and (d) 373 K, depicting STATES 0 and 1 corresponding to WRITE (WR) and RESET (RST), respectively.
memory operation. Hence, a larger RST-to-WR window is observed for ReS₂ compared to MoS₂. Figure 3(c) shows the ratio of \( g_m \) closer to STATE 0 (\( g_{m,RS} \) for RS and \( g_{m,FS} \) for FS) to \( g_m \) closer to STATE 1 (\( g_{m,RS} \) for RS and \( g_{m,FS} \) for FS) as marked in Figs. 1(d) and 2(d). The difference between \( g_{m,RS}/g_{m,FS} \) and \( g_{m,FS}/g_{m,RS} \) is defined as the RD window, which rapidly increases with increasing \( T \) for ReS₂ at much lower \( T \) as compared to MoS₂.

When \( T \) is increased from RT to higher \( T \), a change from CW to ACW hysteresis along with step-like jumps occurs during both FS

![Image](https://example.com/image.png)

**FIG. 2.** \( G(V) \) vs \( V_G \) at \( V_D = 0.5 \text{ V} \) for MoS₂ FET showing the evolving hysteresis width with increasing \( T \) at (a) 323 K, (b) 348 K, (c) 373 K, and (d) 400 K, indicating memory STATE 0 and STATE 1.""
Finally, T-dependent KPFM measurements were performed to confirm the proposed model. The average contact potential difference (CPD) measured for ReS$_2$ and MoS$_2$ is shown in Fig. 4(d). We define CPD by

$$\phi_{\text{sample}} = \phi_{\text{tip}} - [q \times \text{CPD}], \quad (2)$$

where $\phi_{\text{sample}}$ and $\phi_{\text{tip}}$ represent the work function of the sample and the tip, respectively, and $q$ is the electronic charge. The CPD values obtained are consistent with previous reports. CPD values for ReS$_2$ increase with increasing T, whereas they remain almost unchanged for MoS$_2$. The temperatures for crossover from CW to ACW hysteresis are marked as $T_{\text{C,CW,ReS}}$ and $T_{\text{C,CW,MoS}}$. The material with a more negative CPD value implies a larger work function and more electron depletion [Eq. (2)]. According to previous reports, gas adsorbates that act as electron acceptors are responsible for electron depletion, leading to more negative CPD. However, all the measurements in this work are carried out in a controlled nitrogen ambient, ruling out the presence of adsorbates as a possible cause for electron depletion. Therefore, we infer intrinsic trapping as the likely reason for electron depletion, resulting in more negative CPD values at RT for ReS$_2$. Moreover, intrinsic trapping can only be observed in devices with fully depleted channels; hence, at higher T, the effect of intrinsic traps is nullified and oxide trapping dominates. As shown in Fig. 4(d), $T_{\text{C,D,ReS}}$ is less than $T_{\text{C,D,MoS}}$, implying that the effect of intrinsic traps persists for much higher T in MoS$_2$ than for ReS$_2$ consistent with the proposed model. The CPD maps for ReS$_2$ are shown in Fig. 5(a) at 323 K and Fig. 5(b) at 373 K and for MoS$_2$ in Fig. 5(c) at 323 K and Fig. 5(d) at 373 K. The contrast for all the images is adjusted on the same scale, clearly showing the most negative CPD for ReS$_2$ at RT in Fig. 5(a).

To conclude, in this report, we demonstrate thermally assisted memory using back-gated vdP FETs with few-layer ReS$_2$ and MoS$_2$ as the channel materials. The transfer characteristics show a change in the hysteresis direction from CW to ACW with increasing T, along with step-like jumps in the transfer curves at higher T (STC crossover hysteresis). Memory parameters such as RST-to-WR and RD windows are compared for memory operation. The step-like jumps in the transfer curve occur at much lower T for ReS$_2$ (373 K) as compared to MoS$_2$ (400 K), making it a better choice for memory applications. These results are ascribed to a combined effect of intrinsic traps at lower T and screening of gate voltage due to electron injection from the gate into oxide trapping sites at higher T. This physical model is corroborated through T-dependent KPFM measurements that show an increase in CPD for ReS$_2$, while an almost constant CPD for MoS$_2$ with increasing T. This implies enhanced depletion of electrons in ReS$_2$ with increasing T, reinforcing the model of faster de-trapping of intrinsic ReS$_2$ traps with T and hence a lower crossover T.

See the supplementary material for the transconductance ($g_m$) vs gate voltage ($V_G$) plots at varying temperatures for ReS$_2$ and MoS$_2$ showing jumps during forward sweep and reverse sweep at high temperatures.

**REFERENCES**

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