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Comparison of Strain Effect between Aluminum and Palladium Gated MOS Quantum Dot Systems

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Abstract: As nano-scale metal-oxide-semiconductor devices are cooled to temperatures below 1 K, detrimental effects due to unintentional dots become apparent. The reproducibility of the location of these unintentional dots suggests that there are other mechanisms in play, such as mechanical strains in the semiconductor introduced by metallic gates. Here, we investigate the formation of strain-induced dots on aluminum and palladium gated metal oxide semiconductor (MOS) quantum devices using COMSOL Multiphysics. Simulation results show that the strain effect on the electrochemical potential of the system can be minimized by replacing aluminum with palladium as the gate material and increasing the thickness of the gate oxide.

Keywords: strain; MOS quantum dot; COMSOL

1. Introduction

Gate-defined semiconductor quantum dots form a promising platform for quantum computation [1]. Recent studies of metal oxide semiconductor (MOS) quantum dots have shown confinement of individual electrons [2–4] and coherent manipulation of electron spin states [5–7]. However, the formation of unintentional dots is observed in most of these studies [2–7]. Such a phenomenon is undesirable and causes a variety of problems, as these disorder dots can capacitively couple to the gate confined quantum dot and disrupt both transport and charge sensing measurements. Since the observation of these dots is reproducible, mechanical strain due to different coefficients of thermal expansion (CTEs) of fabricated materials cooled to cryogenic temperatures is a likely candidate [8]. Such thermal strain may cause tensile stress (positive strain) or compressive stress (negative strain) on crystal band structures [8,9], subsequently modifying the energy levels within the conduction band. Significant stress/strains will lead to the formation of unintentional dots that can be detrimental to the operation of the intentional dots. There are various methods for avoiding unintentional dots in a quantum dot system [10] and reducing strain from room temperature down to < 1 K [11]. Moreover, the modulation of the conduction band due to strain can also be compensated to a limited degree through variation of voltages applied to the gates [12,13].

In this paper, we focus on the comparison of two quantum dot architecture models based on non-tunable [2] and tunable [3] single dot systems which are electrostatically defined via multiple stacked gates. We emphasize on the use of palladium (Pd), replacing aluminum (Al) as the metallic gates to reduce strain in MOS interface at sub-Kelvin temperatures. Pd is chosen due to ease of fabrication process and much smaller CTE by nature as shown in Table 1. Pd films deposited via physical vapor deposition (PVD) can result in smaller grain size [14], enabling better gate definition

with critical dimensions of 10–15 nm, while Al gates are limited by grain boundaries of ~30 nm [15]. Table 1 also shows the density of Pd is much higher than Al, which also means Pd fundamentally has smaller grain size compared to Al since grain size is a function of sintered density where the grain size correlates to the inverse square-root of fractional porosity [16]. Silicon remains the substrate of choice due not only to its compatibility with mature nano-fabrication technology, but also the ability to isotopically purify the silicon and suppress the Si-29 nuclear spin in silicon that will prolong the electron spin coherence [17–19].

2. Methods

The quantum dot architectures are modeled and simulated in three dimensions (3D) using COMSOL Multiphysics [20]. For strain computation, the workflow of the COMSOL model builder starts by opening the "Model Wizard", followed by the selection of space dimension and adding a physics option, in our case, the 3D and solid mechanics under "Structural Mechanics" node respectively. After this, specific geometries are created, and material based on Table 1 are selected to build the quantum dot architectures. Here, time-varying material properties are not considered, therefore the "Stationary" study method is selected to analyze the strain effects of cooling after the system reaches steady state.

Since the main study is related to strain caused by CTE mismatch among the materials, the thermal expansion sub node is added to prescribe the deformation of the constrained boundary caused by changes in temperature. Thermal strain, ϵ_{th}, as shown in Equation (1) is used for the computation of elastic strain components ϵ_x, ϵ_y and ϵ_z. This equation depends on the CTE of the material, α, the final temperature to be simulated, T (1 K), and the initial strain-free reference temperature, T_{ref} (300 K).

$$\epsilon_{th} = \alpha\left(T - T_{ref}\right). \tag{1}$$

In the constrained boundary's condition, the expansion of the materials is restricted. The elastic strains produced are due to thermal expansion and the reaction stress components δ_x, δ_y, and δ_z [21]. Denoting Poisson's ratio by v and Young's modulus by E, and assuming Hooke's law applies, then:

$$\begin{aligned} \epsilon_x &= \frac{1}{E}\left[\delta_x - v\left(\delta_y + \delta_z\right)\right], \\ \epsilon_y &= \frac{1}{E}\left[\delta_y - v(\delta_x + \delta_z)\right], \\ \epsilon_z &= \frac{1}{E}\left[\delta_z - v\left(\delta_x + \delta_y\right)\right]. \end{aligned} \tag{2}$$

Table 1. Material properties specifications at T = 300 K.

Material	Density, ρ (kg/m^3)	Young's Modulus, E (GPa)	Poisson's Ratio, v (kg/m^3)	Coefficient of Thermal Expansion, α ($\times 10^{-6}$/K)	Reference
Palladium	12,020	73	0.44	11.8	[22]
Aluminum	2700	70	0.35	23	
Aluminum Oxide	3900	300	0.22	5.4	[8]
Silicon	2300	130	0.27	2.6	
Silicon Dioxide	2200	73	0.17	0.49	

For simplicity, the room temperature (T = 300 K) materials properties which includes density, Young's modulus, Poisson's ratio, and coefficients of thermal expansion (CTE) as shown in Table 1, is considered to compute the elastic strain components. These strain data are subsequently used to calculate the change in energy of the conduction band, ΔE_C as shown in Equation (3), where Ξ_u and Ξ_d

are the uniaxial and dilatation deformation potentials [23]. Here, Ξ_u and Ξ_d are set at the potential of 10.5 eV and 1.1 eV respectively [24].

$$\Delta E_C = \Xi_u \, \epsilon_z + \Xi_d \left(\epsilon_x + \epsilon_y + \epsilon_z\right). \tag{3}$$

From Equation (3), the conduction band changes by approximately 1 meV for every 0.01% strain in ϵ_z. Since the charging energy in a quantum dot is approximately 2–6 meV [2,3], there is a possibility of the formation of unintentional dot if the strain magnitude of ϵ_z is greater than 0.02%.

Figure 1 shows (a) non-tunable and (b) tunable single dot structures where the materials used for the upper gate (UG), lower gate (LG), and plunger gate (PG) are based on Al or Pd. The Si-bulk dimensions are defined with respect to length × width × height at 600 nm × 600 nm × 150 nm, while SiO_2 thickness is set at 10 nm above the Si-bulk which forms intrinsic stress of -200 MPa [25]. In Figure 1a, the dimensions of the UG is set at 400 nm × 50 nm × 80 nm, while the LG is a cylindrically shaped gate with 12.5 nm radius with 400 nm in length, insulated with aluminum oxide (Al_2O_3) of 3 nm. Similarly, in Figure 1b, the PG size is the same as the LG. The gap between the two LGs in Figure 1 is intentionally set at 30 nm to closely represent the structures in [2] and [3]. The strain of both structures is simulated for a change in temperature of 300 K to 1 K. Same study is also carried out for the silicon dioxide (SiO_2) thickness which is set 10 nm, then repeated with 30 nm and 50 nm. The variation of SiO_2 thickness is studied as it has the lowest CTE, hence, thicker SiO_2 may reduce strain [8].

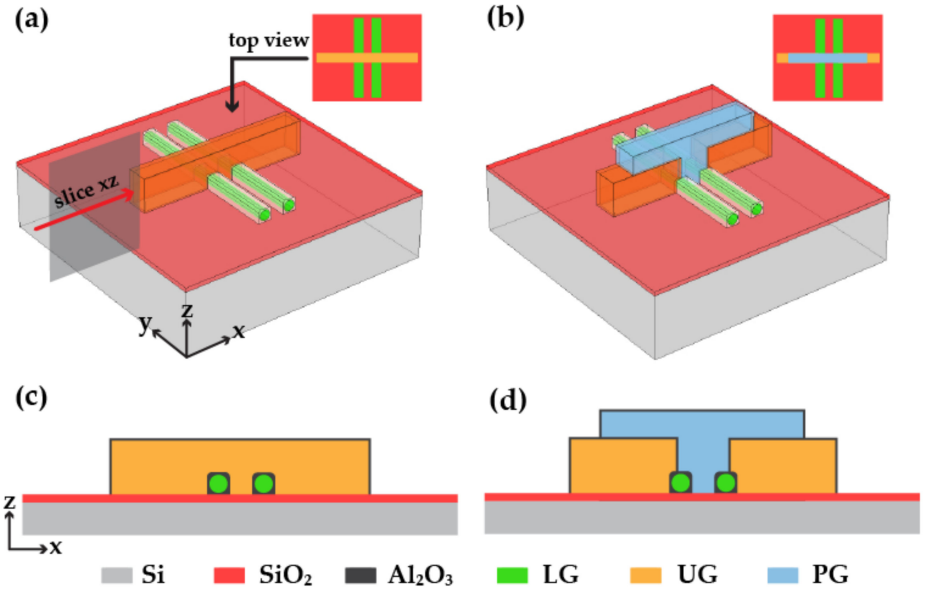

Figure 1. Modeled single quantum dot architectures. (**a**) Colored three dimensions (3D) and top views and (**c**) cross-section views of the non-tunable single quantum dot with only one upper gate (UG) used to define the quantum dot as well as the electron reservoirs. (**b**) Colored 3D and top views and (**d**) cross-section views of the tunable single quantum dot with the UG split in two to control the electron reservoirs while the plunger gate (PG) is used to independently define the quantum dot.

3. Results and Discussion

Systematic studies for a change in temperature from 300 K to 1 K are carried out to compare the strain effects on models shown in Figure 1. Strain results observed across Figure 2a,b and Figure 3a,b show that CTE mismatches among metal (Al or Pd), and Al_2O_3 and SiO_2 create stresses that propagate into the Si-bulk. Al or Pd is always in tensile stress while Al_2O_3 is in compressive stress. This is due to the Al_2O_3 preventing the Al or Pd from contracting. These stresses then propagate through the SiO_2

into the Si-bulk. Note that the CTE mismatch from the SiO_2 and intrinsic stress from the SiO_2 only results in uniform strain and cannot form unintentional dots.

All simulated results are extracted 1 nm below the Si–SiO_2 interface, close to the expected peak of the quantum dot wavefunction [23]. Firstly, Figure 1a model with Al gates are simulated at 10 nm SiO_2 thickness where the positive and negative strains results for all x, y, and z components are shown in Figure 2c. Note that the actual gate-defined quantum dot is formed in the Si–SiO_2 interface in between $x = \pm 15$. Based on Figure 2c, large negative strains are observed between x = −40 and +40 especially regions with stacked materials Si/SiO_2/Al/Al_2O_3. Similarly, when the Al gates are replaced by Pd gates, the trend is the same, however, with reduced negative strain, as shown in Figure 2d. This also means Pd can reduce compressive stress of Al_2O_3 due to lesser CTE mismatch.

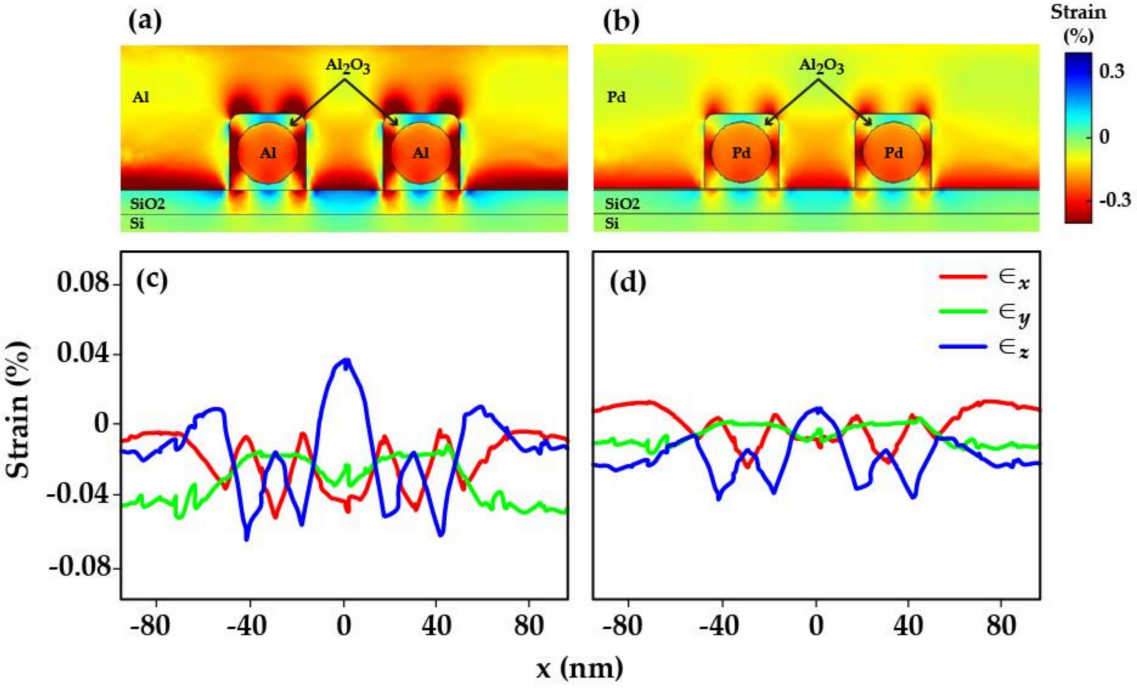

Figure 2. Simulated strain for Al and Pd gates on Si-bulk based on Figure 1a model at the SiO_2 thickness of 10 nm. (**a**,**b**) are the cross-section strain $\in_z$ cut at xz axis plane, while (**c**,**d**) are the strain components $\in_x$, $\in_y$ and $\in_z$ at 1 nm below the Si–SiO_2 interface for Al gates and Pd gates, showing the effect of strains from CTE mismatch of Al–Al_2O_3 and Pd–Al_2O_3, respectively.

At this stage, unintentional dots are apparent as the average strain magnitude $\in_z$ is still much larger than 0.02%. Based on previous studies, the strain effects can be manipulated by varying the SiO_2 thickness [8]. Figure 4a,c show the strain and conduction band respectively for both Al and Pd, at the SiO_2 thickness of 10 nm, 30 nm, and 50 nm. As the SiO_2 thickness increases, the overall strain reduces significantly shifting the unintentional dots from x = −40 and +40 to x = −30 and +30. However, it is important to note that thicker SiO_2 may require larger voltages across all the metallic gates and may eventually cause leakage currents between the gate to gate layer [26].

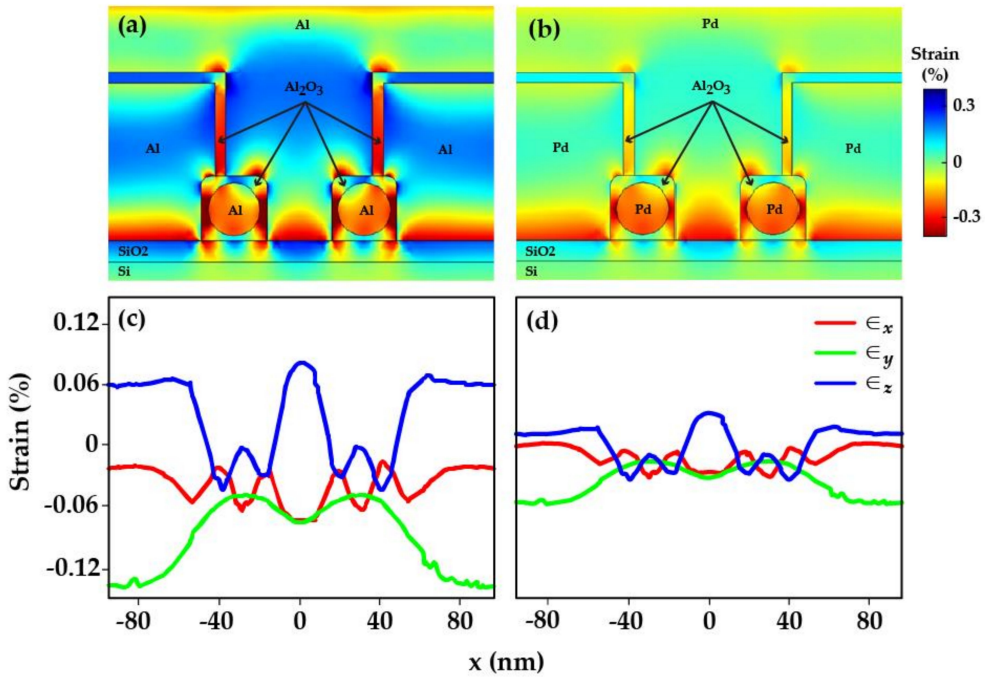

Figure 3. Simulated strain for Al and Pd gates on Si-bulk based on Figure 1b model at the SiO_2 thickness of 10 nm. (**a**,**b**) are the cross-section strain $\in_z$ cut at *xz* axis plane, while (**c**,**d**) are the strain components $\in_x$, $\in_y$ and $\in_z$ at 1 nm below the Si–SiO_2 interface for Al gates and Pd gates, showing the effect of strains from CTE mismatch of Al–Al_2O_3 and Pd–Al_2O_3, respectively.

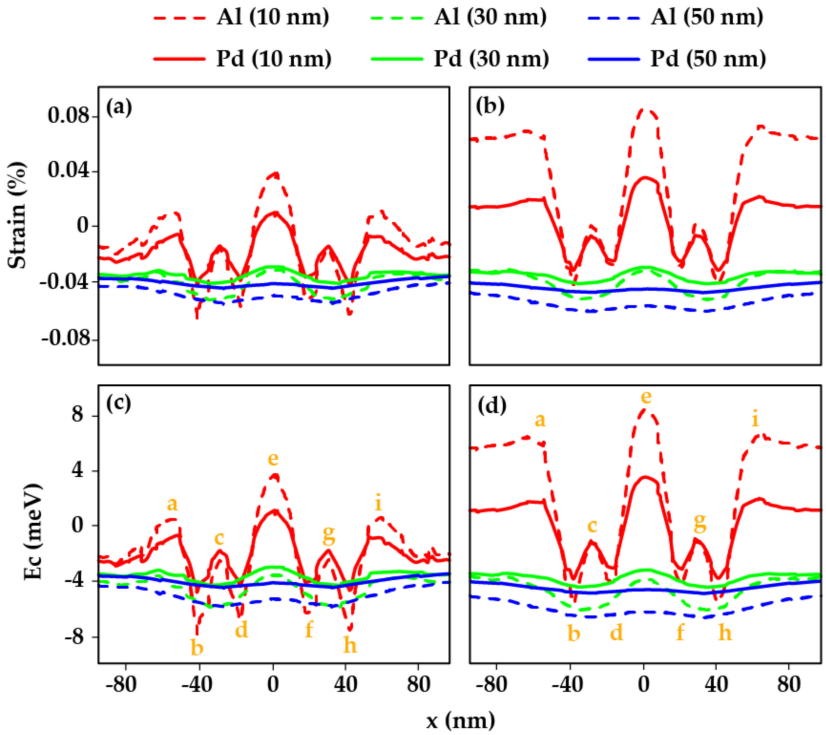

Figure 4. (**a**,**b**) Strain $\in_z$ comparison of Al vs Pd gates on Si-bulk at the SiO_2 thickness of 10 nm, 30 nm and 50 nm for Figure 1a,b models respectively. (**c**,**d**) Calculated conduction bands for Al vs Pd based on (**a**,**b**) simulated strain results respectively at the SiO_2 thickness of 10 nm, 30 nm and 50 nm. The peaks and valleys of the conduction bands are indicated by a – i (in orange) to calculate the average change in conduction bands due to CTE mismatch.

Next, the Figure 1b model is studied using the same method. By splitting the UG and using the PG to define the quantum dot, lesser negative strain is observed as shown in Figures 3 and 4b. This is mainly due to additional Al_2O_3 formed vertically on top of the LG, creating lesser compression force. Based on the strain results, the conduction band is calculated as shown in Figure 4c. As compared to the Figure 1a model, the formation of unintentional dots is not so apparent and can be avoided by setting the SiO_2 thickness to 30 nm or 50 nm.

Further comparisons on the changes around the peaks and valleys of the conduction band for Al and Pd at different SiO_2 thickness, labelled a–i (orange colored) in Figure 4c,d, are tabulated in Tables 2 and 3 respectively. The magnitudes for the peaks and valleys are added to show the severity of the band bending in the conduction band, where a larger value indicates higher possibility of unintentional dots forming around the labelled regions. The average magnitude change of Pd is approximately two times smaller than Al, indicating Pd should be selected over Al to reduce the effect of strains on conduction band.

Table 2. Changes in magnitude of the conduction band peaks (a, c, e, g, and i) and valleys (b, d, f, and h) based on Figure 4c. Energy differences between Al and Pd are calculated for SiO_2 at 10 nm, 30 nm, and 50 nm.

SiO_2 (nm)	|a| + |b| (meV)	|d| +|e| (meV)	|e| + |f| (meV)	|h| + |i| (meV)	Average (meV)
10 - Al	7.90	9.92	10.6	8.57	9.25
10 - Pd	5.22	5.12	5.55	5.24	5.28
Δ 10 (Al-Pd)	2.68	4.8	4.95	3.33	3.97
30 - Al	1.39	1.71	1.87	1.32	1.57
30 - Pd	0.52	0.98	1.08	0.64	0.81
Δ 30 (Al-Pd)	0.87	0.73	0.79	0.68	0.76
50 - Al	0.92	0.45	0.19	0.95	0.63
50 - Pd	0.5	0.28	0.12	0.52	0.36
Δ 50 (Al-Pd)	0.42	0.17	0.07	0.43	0.27

Table 3. Changes in magnitude of the conduction band peaks (a, c, e, g, and i) and valleys (b, d, f, and h) based on Figure 4d. Energy differences between Al and Pd are calculated for SiO_2 at 10 nm, 30 nm, and 50 nm.

SiO_2 (nm)	|a| + |b| (meV)	|d| +|e| (meV)	|e| + |f| (meV)	|h| + |i| (meV)	Average (meV)
10 - Al	12.06	12.25	12.49	10.88	11.92
10 - Pd	5.71	6.52	6.61	4.92	5.94
Δ 10 (Al-Pd)	6.35	5.73	5.88	5.96	5.98
30 - Al	1.92	1.47	1.28	1.00	2.84
30 - Pd	0.84	0.84	0.69	0.51	0.72
Δ 30 (Al-Pd)	1.08	0.63	0.59	0.49	2.12
50 - Al	0.53	0.2	0.23	0.42	0.35
50 - Pd	0.26	0.12	0.13	0.21	0.18
Δ 50 (Al-Pd)	0.27	0.08	0.10	0.21	0.17

4. Conclusions

We show that strain from smaller CTE mismatches and thicker SiO_2 can significantly reduce the formation of unintentional dots in a quantum dot system. A much smaller positive–negative strain is observed across the models with Pd gates as compared to Al gates. Note that even Al is currently widely used as the gates, whereas Pd may give a smaller positive–negative strain especially for multi-stacked gates architectures. In terms of minimizing the formation of unintentional dots, the recommended SiO_2 thickness should be set to at least 30 nm or above. We acknowledge that, while we simulated for a change in temperature of 300 K to 1 K instead of 450 K to 1 K as reported by the authors in [8], our results show a similar trend at an acceptable lesser strain. The shortcoming of this simulation is that we were unable to clearly explore the temperature dependence of the CTE for all

the materials due to lack of information on the CTE over the entire simulated thermal range. Although the material parameters used in the simulations are fixed at room temperature, the reported results can still be used to closely represent the actual condition of quantum dot systems at T = 1 K.

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