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A wideband blocker-resilient direct delta sigma receiver with selective input-impedance matching

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Abstract
This paper presents a wideband blocker-tolerant direct $\Delta\Sigma$ receiver (DDSR). Blockers are attenuated through selective input impedance matching and reduced gain design. The selective input impedance profile provides a low impedance at blocker frequencies enabling blocker attenuation, while the in-band impedance is boosted to matched condition through an up-converted positive feedback from the DDSR output. In addition, with the help of reduced gain design, near band blocker gain is minimized, further improving the blocker resilience. The receiver is designed for configurable operation from 0.7–2.7 GHz and a baseband bandwidth of 10 MHz. Simulated in a 28 nm technology, the DDSR demonstrates a maximum noise figure of 6.2 dB, and achieves a peak SNDR of 53 dB with an out-of-band 1 dB input compression point of -11 dBm at a 100 MHz offset.

Keywords Blocker tolerance · Selective impedance matching · Tunable bandpass filtering · Low noise amplifier · Direct delta sigma receiver

1 Introduction

Wireless receivers for emerging radio access standards such as 5G and LTE-A demand a reconfigurable operation on multiple frequency bands and across a wireless spectrum of several GHz. To meet this required reconfigurability, several digital intensive architectures have been envisioned [1–4]. Among these, one showing promising performance is the direct-$\Delta\Sigma$-receiver (DDSR). The architecture was first presented in [5] and investigated further in [6–10].

The wideband DDSR architecture differs from conventional direct conversion receivers by embedding RF front-end units as part of a delta-sigma-modulator (DSM) loop-filter. As shown in Fig. 1, the DDSR brings the outermost loop of the feedback type $\Delta\Sigma$ modulator to the output of a low noise amplifier (LNA). In this way, signal discretization already begins at RF and the DSM loop filter performs the functions of both baseband filtering and quantization noise shaping.

Inherently, such wideband receivers are exposed to high power out-of-band (OB) blockers. If not attenuated, these blockers may completely saturate the receiver and make reception non-linear. Traditionally, OB blocker resilience has been achieved by utilizing external off-chip filtering. However, as external filters are generally non-tunable and bulky, multiple filters are required to cover wide range of receiver bands. Two widely used on-chip alternatives for improving blocker resilience in wideband receivers are: (1) applying N-path filtering at the LNA output and (2) low-noise transconductance amplifier/mixer first arrangements [2, 6, 9, 11–16]. However, as will be explained later, these techniques have certain blocker rejection limitations such as not addressing the OB linearity degradation due to receiver input transconductor swing range limitation.

In this paper we propose a blocker resilient DDSR which attenuates blockers at both the input and output

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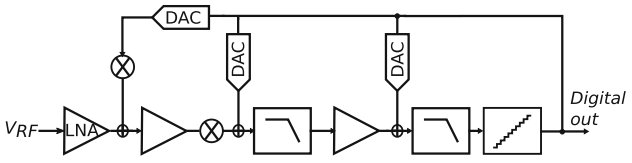

Fig. 1 Generic block diagram of the direct $\Delta\Sigma$ receiver. The RF stages are included in the $\Delta\Sigma$ modulator (DSM) loop-filter, thus minimizing the number of stages in the receiver

nodes of LNA. The additional bandpass filtering at LNA input is achieved through design of a low-intrinsic input impedance LNA, which provides OB voltage attenuation when driven by source impedance higher than LNA input impedance. On the other hand, at the desired signal frequency, input impedance is boosted to matched condition by implementation of positive upconverted feedback from the DDSR output. Additionally, we follow an approach of reduced receiver gain design which results in an improved near-band compression point. Evaluated with detailed simulations in a 28 nm technology, the proposed selective input impedance matching and reduced gain design approach demonstrates state-of-the art blocker tolerance, when compared with recently published DDSRs.

The paper is organized as follows. Section 2 describes the limitations of blocker rejection with basic N-path filtering and how rejection can be improved with our proposed solution of selective input impedance and reduced gain design. Section 3 details the design method for the proposed DDSR while Sect. 4 covers its transistor level implementation details. We finalize the discussion with performance evaluation results in Sect. 5 and conclusions in Sect. 6.

2 Blocker rejection for a DDSR

2.1 Blocker rejection at the DDSR input

In DDSRs blocker rejection is usually achieved by implementing N-path filtering technique at the LNA output [5, 6]. However, there are two limitations with this approach. First, the gain/loss of far-away blockers is limited by the N-path mixer switch resistance (R_{SW}) and the LNA transconductance ($g_{m,LNA}$) which should both be minimized. These parameters cannot be reduced indefinitely due to limitations on local oscillator (LO) drive power consumption and LNA noise contribution. Second, filtering is implemented only at LNA output, neglecting the filtering requirement at the input. Without input filtering and provided the low blocker gain at the LNA output due to filtering, the LNA transconductor input swing range limits can reach earlier then its output. Therefore, an optimum design should ideally filter the OB blockers already at the LNA input.

In order to provide on-chip bandpass filtering at the DDSR input, the input impedance (R_{IN}) needs to be frequency dependent and lower than source impedance (R_S). The relative blocker voltage attenuation is proportional to the ratio between R_S and R_{IN} at blocker frequencies. Such an input impedance profile has been demonstrated earlier in [17, 18] for LNA-first receivers and in [19] for mixer-first receivers. However, in both LNA-first and mixer-first designs, the selected input impedance profile was chosen to reduce the noise contribution of the front-end. The authors did not report the possibility of blocker attenuation through optimizing the input impedance profile. In this paper, we utilize this impedance profile to provide additional blocker voltage attenuation already at the DDSR input.

2.2 Blocker rejection through optimized gain design

In a typical down-conversion receiver, gain is needed for two reasons: First, it suppresses noise contributions from the later stages of the receiver. From this point of view, implementing gain more than the minimum required to suppress the noise contribution of later stages does not bring any benefit from noise perspective. Second, gain is needed so that the weakest input signal appearing at the analog-to-digital converter (ADC) input is sufficiently greater than the quantization noise of the ADC. For DDSRs, however, this ADC input range requirement is different and needs further explanation.

Figure 2 presents a comparison of the typical output spectrum for a Nyquist-rate ADC based receiver and that of a DDSR. Typically, a Nyquist-rate ADC for a receiver is designed to meet certain signal-to-noise and distortion ratio (SNDR) requirement dictated by the communication standard. The maximum SNDR achieved by the ADC is limited on upper side by full-scale linear voltage swing range (V_{FS}) and on the lower side by the noise floor. A typical ADC design process starts from V_{FS} and the required SNDR is achieved by pushing the ADC's quantization noise floor down by increasing the ADC resolution. After defining this resolution, sufficient gain needs to be applied in the receiver chain so that the amplified receiver thermal noise level at the ADC input is higher than the quantization noise floor. This ensures that the quantization noise does not contribute significantly to the overall receiver noise. Analytically we can calculate the minimum gain (G) requirement for Nyquist-ADC based receivers as:

$$G = P_{FS} - SNR_{tar} - SNR_{min} + 174 - 10log(f_{BW}) \quad (1)$$

where P_{FS} is the ADC full-scale power in dBm, SNR_{tar} is the required SNR for a given specification, SNR_{min} is the

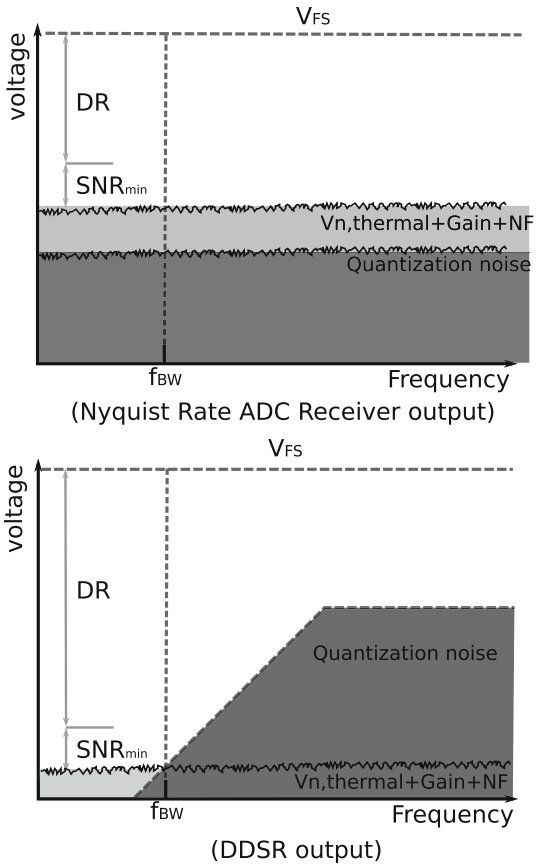

Fig. 2 Comparison of gain requirement for (top) a typical receiver with a Nyquist rate ADC and (bottom) a DDSR

minimum acceptable SNR for an acceptable reception, and f_{BW} is the required channel bandwidth.

In contrast, the DDSR design begins from the in-band thermal noise floor level at the input of the receiver. The amount of gain that is applied in the in the DDSR is selected solely based on what is needed to ensure that the LNA is the most significant noise contributor. The resolution of the quantizer and the loop filter order are then designed so that the in-band quantization noise is sufficiently lower than the amplified thermal noise. This ensures that the minimum amount of gain is applied in the receiver.

Now let us consider how the lower gain helps to achieve optimized blocker rejection in DDSR design. High power blockers can make the receiver operation non-linear if they are strong enough to reach the swing range limitations of the designed RF and BB amplifiers. Any additional gain for blockers will result in amplifier swing range limitations being reached earlier. Therefore, whenever gain is applied in the receiver, it should be selective so that only desired signals are amplified and blockers are attenuated. Usually this is done in receivers through RF and/or BB filtering. However, filtering profiles for a single stage are generally limited to first-order roll-off after the cut-off frequency. This means that any near-band blockers will not be suppressed adequately by a single filtering stage. A higher number of filtering stages with partitioned gain can be employed for reasonable suppression of near-band blocker signals. However, after a certain limit, increasing the number of stages becomes impractical due to increased power consumption. Another way to solve this problem is to implement higher-order filtering schemes such as in [15]. However, higher-order filtering still provides limited near-band blocker attenuation. Considering this limited roll-off of RF and BB filters, we propose to suppress the near-band blocker signals with minimum possible gain. This is easy to achieve in DDSRs, as the absolute power of DSM quantization noise is much lower than thermal noise floor due to the inherent noise shaping of DDSR.

Based on the aforementioned discussion, our proposed DDSR consists of optimized receiver gain design together with tunable bandpass filtering at the RF input. We now detail the design of proposed the DDSR.

3 DDSR design

Figure 3 shows the block diagram of the proposed DDSR. In comparison to the traditional DDSR architecture, the proposed architecture differs in the front-end design. We intentionally design the intrinsic input impedance (R_{INT}) of the front-end to be lower than the antenna source impedance (R_S) while at the desired frequency this R_{INT} is boosted to matched conditions by the application of up-converted positive feedback from the DDSR output (Fig. 5). As explained earlier, lower R_{IN} at blocker frequencies helps to reduce blocker voltage gain already at the DDSR input.

Apart from attenuating the blockers from selective impedance profile, the proposed DDSR is designed with only the minimum closed loop gain (A_{CL}) required to suppress the noise contribution of later stages. The A_{CL} gain is defined from the LNA input to DDSR output including the input impedance mismatch effects. As explained earlier, this reduced gain helps to achieve better near-band blocker rejection. An A_{CL} of 20 dB is selected in this case which will suppress the noise contribution from later stages to about 10 ×. This means that later DDSR stages can be designed with much lower current. For such a case, combined noise factor (F_{tot}) of stages after the LNA can be derived as:

$$F_{tot} = 1 + (F_{RX} - F_{LNA})A_{CL} \quad (2)$$

here A_{CL} should be put on linear scale, and F_{RX} is the target NF of receiver. To achieve such F_{tot}, we can

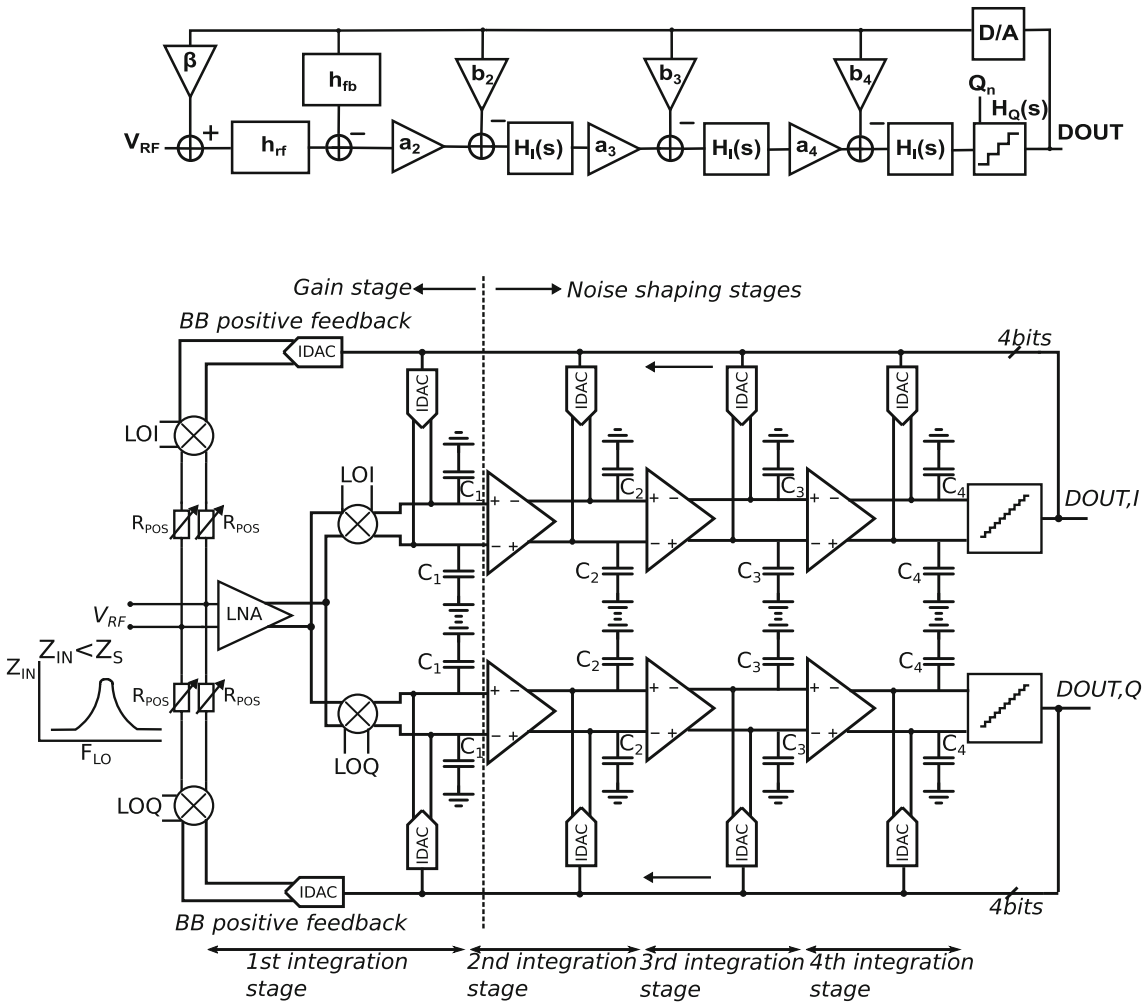

Fig. 3 (Top) Block level representation of the proposed receiver, and (bottom) implementation of the proposed wide-band DDSR architecture. Blockers are attenuated through low LNA input impedance (R_{IN}), while positive feedback from BB increases R_{IN} to matched condition for the desired frequency

approximate the later stage minimum required transconductance as:

$$g_m \approx \frac{\eta}{R_S(F_{tot}-1)} \tag{3}$$

where η is process and channle-length dependent constant.

After the selection of A_{CL}, and referring to Fig. 4 for parameter definitions, the DDSR design is split into four steps: (1) the value of the positive feedback factor (β_{req}) and the DDSR open loop gain without the positive feedback (A_{OL}) are solved which provide the desired impedance match and A_{CL}. (2) The loop-filter is designed with the calculated A_{OL} specification. (3) we take into account the non-idealities of the N-path filter and demonstrate how the DSM coefficients are implemented in the circuit. Finally, in (4) positive feedback is implemented with a value of required feedback factor (β_{req}) from step one that matches R_{IN} to R_S and raises A_{OL} to A_{CL} (Fig. 5). In the

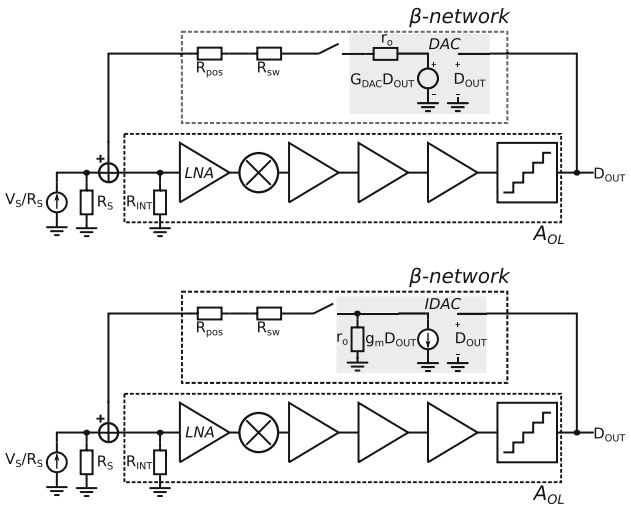

Fig. 4 Simplified small signal model of positive feedback loop excluding the mixer upconversion effects (top) voltage mode DAC implementation (bottom) Current steering DAC implementation

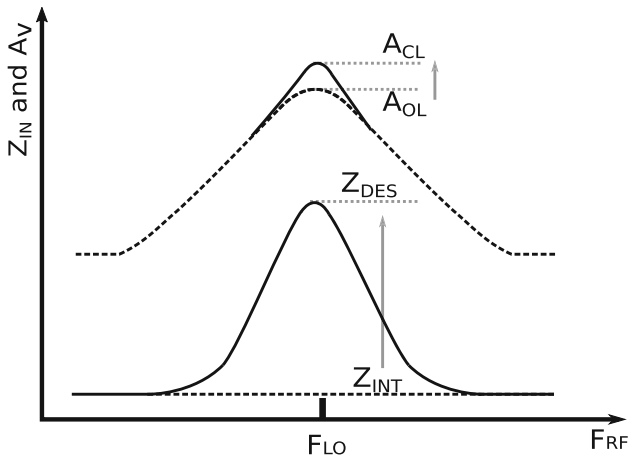

Fig. 5 Design procedure for implementation of positive feedback in the proposed DDSR. Loop gain of DDSR is first designed for gain A_{OL} and intrinsic input impedance of R_{INT}. Implementation of positive feedback increases the loop gain from A_{OL} to desired closed loop gain A_{CL} and raises R_{IN} to the desired matched input impedance R_{DES}

following, we explain the four design steps of the proposed DDSR in detail.

3.1 Positive feedback loop design

The purpose of the positive feedback loop in the proposed DDSR is to boost R_{IN} to matched conditions. The loop consists of an upconverting passive mixer in series with resistance (R_{POS}). The digital BB output of the DDSR can be fed to the upconverting passive mixers either through a current-steering digital to analog converter (IDAC) or a low output-impedance voltage-mode DAC. In the following text we provide the design procedure with both IDAC and DAC implementations.

3.1.1 Case-I, DAC implementation

As explained, the positive feedback loop boosts R_{IN} to matched conditions. However, the implementation of positive feedback also increases the gain of the DDSR and consequently reduces the bandwidth. Therefore, the initial open loop gain of DDSR without positive feedback (A_{OL}) should be designed to be lower than target A_{CL} = 20 dB.

In order to find the starting A_{OL} and the required value of positive feedback factor β_{req} that gives the matched input impedance and A_{CL} = 20 dB, the small-single model presented in Fig. 4 can be used. The presented model does not consider passive mixer upconversion losses, therefore, some deviation of analytical results from simulated response is expected. Nevertheless, for quadrature passive mixers with 25% duty-cycle, the difference is not large and results can be used with reasonable accuracy. For the presented model, a simple shunt-shunt positive feedback analysis with DAC gain (G_{DAC}) of unity provides [20]:

$$\beta_{req} \approx \frac{R_{INT}R_S - R_S(R_S||R_{DES}) - (R_S||R_{DES})R_{INT}}{(R_S||R_{DES})R_{INT}R_S - A_{CL}R_{INT}R_S^2}, \quad (4)$$

where R_{INT} is the intrinsic input impedance of the DDSR front-end and R_{DES} is the desired R_{IN} for a matched case. In addition, A_{CL} should be put on linear scale in all derived equations of the presented model. Provided that the calculated β_{req} is lower than the maximum theoretical $\beta_{req} < 1/A_{OL}$, a stable implementation of β_{req} is possible. The positive feedback factor β can be implemented by design as:

$$\beta \approx \frac{1}{R_{POS} + R_{SW} + r_o}, \quad (5)$$

where R_{SW} is the passive mixer switch resistance and r_o is the output impedance of DAC. This means that β_{req} can be achieved by controlling the value of R_{POS} in the positive feedback loop.

Based on β_{req}, we can calculate the starting open-loop gain A_{OL} that will result in A_{CL} = 20 dB after the implementation of positive feedback.

$$A_{OL} \approx \frac{A_{CL}R_S}{(1 + A_{CL}R_S\beta_{req})(R_S||R_{INT}||1/\beta_{req})}. \quad (6)$$

where the calculated A_{OL} is in linear scale. As a design example we select R_{INT} = 15 Ω, R_{DES} = 50 Ω, G_{ADC} = 1 and R_S = 50 Ω. These values are extracted from the implemented circuits in DDSR and represent what can be practically be achieved. For example, reducing R_{INT} to be lower than 15 Ω will increase the power consumption of LNA substantially. Based on the chosen parameters, the required feedback factor from Eq. ?? is $\beta_{req} \approx 0.005$. In other words, $R_{POS}+R_{SW}+r_o$ of 200 Ω is required. Based on the calculated β_{req}, Eq. 4 suggests A_{OL} = 13.3 dB.

3.1.2 Case-II, IDAC implementation

As presented in Fig. 4, the IDAC implementation in the positive feedback path can be modeled with a voltage controlled current source having a transconductance $g_{m,IDAC}$ and output resistance r_o. Following a simple shunt-shunt feedback analysis, we can solve the value of positive feedback factor β that gives the required input impedance match and closed loop gain A_{CL}.

$$\beta_{req} \approx \frac{(R_S||R_{DES})(1/(ro + R_{SW}) + 1/R_{INT} + 1/R_S) - 1}{A_{CL}R_S}, \quad (7)$$

Provided that β_{req} is lower than the maximum theoretical $\beta_{req} < 1/A_{OL}$, a stable implementation of β_{req} is possible.

The positive feedback factor β can be implemented by design as:

$$\beta \approx \frac{ro}{ro + R_{POS} + R_{SW}} g_{m,IDAC}, \tag{8}$$

This means that the required value of feedback factor can be achieved by controlling $g_{m,IDAC}$ and R_{POS} (Fig. 4).

Based on β_{req}, we can calculate the starting open-loop gain A_{OL} that will result in A_{CL} = 20 dB after the implementation of positive feedback as:

$$A_{OL} \approx \frac{A_{CL}R_S}{(1 + A_{CL}R_S\beta_{req})(R_S||R_{INT}||(R_S + R_{POS} + ro))}. \tag{9}$$

where the calculated A_{OL} is in linear scale. As a practical design example, we select, R_{INT} = 15 Ω, R_{DES} = 50 Ω, R_S = 50 Ω, R_{SW} = 32 Ω, r_o = 2 KΩ and R_{POS} = 200 Ω. These values are extracted from the implemented circuits in proposed DDSR and represent what can be practically be achieved. In implementation section, we will elaborate more the reason to choose these parameters values. Based on the chosen parameters, the required feedback factor from Eq. 5 is $\beta_{req} \approx 0.005$. In other words, $g_{m,IDAC}$ of 5.5 mS is required. Based on calculated β_{req} Eq. 7 suggests A_{OL} = 13.3 dB.

Both, DAC and IDAC feedback structures are valid choice for positive feedback implementation. However, in order to be consistent with other baseband IDAC based feedbacks in proposed DDSR, we choose an IDAC-based positive feedback implementation.

3.2 Loop-filter design

Based on the calculated value of A_{OL}, the next step is to design the DDSR loop-filter. As has been focus of the discussion, blockers are the main concern when designing a DDSR. Thus, it is also natural that we emphasize the signal transfer function (STF) in the loop-filter design. The cascade of integrators in feedback topology (CIFB) is well suited for a DDSR thanks to its well-defined and non-peaking STF. The poles of the low-pass STF and high-pass noise transfer function (NTF) are identical, meaning that we can choose to design either the STF or NTF, which then fixes the other. We choose to design the STF, while keeping in mind the requirements for quantization noise shaping. Gain needs to be applied in the first stage, so that the noise performance requirement of the later stages can be relaxed. Based on the previous section, we select A_{OL} = 13.3 dB gain in this case. For the out-of-band, we want to keep the applied gain to a minimum and therefore the first pole of the STF needs to be at channel bandwidth (f_{BW}).

Next, we need to calculate the number of additional noise shaping stages after the LNA required for fulfilling the quantization noise shaping requirement. The number of these stages can be calculated to be [6]:

$$n = \frac{log\left(\frac{\Delta^2}{6f_s kTA_{CL}F_{RX}}\right)}{2log\left(\frac{f_{NSP}}{f_{BW}}\right)} \tag{10}$$

where Δ is the quantizer step size, f_S is the sampling frequency, k is Boltzmann constant, T is the temperature in Kelvins (T = 300 K is used), A_{CL} is the required receiver power gain after the implementation of positive feedback, F_{RX} is the noise factor of the receiver excluding quantization noise, f_{BW} is BB bandwidth cutoff frequency, and f_{NSP} is the combined noise shaping pole cutoff frequency. The closed loop gain of the receiver was targeted to be A_{CL} = 20 dB, while the parameters Δ, F_{RX}, f_s and f_{NSP} still remain undefined.

In order to keep the focus of the paper on the positive feedback, we utilize an ideal 4-bit quantization and feedback with a clock delay added to emulate the required time for buffering and transistor switching. The differential input range for the quantizer is selected to be 600 mV, so that it is not the limiting factor for receiver linearity and thus we can calculate that Δ = 40 mV. Noise factor F_{RX} is set by the device noise of amplifiers and the mixers, dominated by the noise of the first amplifier in the chain. For calculating the number of noise shaping stages, we use NF = 5 dB i.e. F_{RX} = 3.1623, which is based on steady-state AC simulations when the discrete feedback is replaced by ideal continuous-time feedback.

The selection of the sampling frequency f_s is critical in a DDSR. This is because the loop-filter contains mixers, that need to operate across the receiver frequency range. If no additional filtering is implemented for the feedback signal that is fed to the mixer nodes, LO frequencies that are not multiples of $f_s/2$ will cause the quantization noise to fold to the in-band and potentially desensitize the receiver [5]. The severity of this effect is dependent on the absolute level of the quantization noise at LO frequency and its harmonics. In order to avoid this issue, we have locked the f_s to LO frequency (f_{LO}). The f_s will thus vary between 0.7–2.7 GHz.

A parameter that still remains undefined is the combined noise shaping pole cutoff frequency f_{NSP}. In addition to being the key factor in determining the required number of stages, f_{NSP} also affects the stability of the loop. The lower limit for f_{NSP} is f_{BW} as the number of stages increases to infinity. As a first order analysis, we can reason that the upper limit is $f_s/4$, as the quantization noise removed from below this frequency has to fit between $f_s/4$ and $f_s/2$, leading to the stability criteria of 3 dB out-of-band gain for

the NTF. As we approach the upper limit, the high-frequency gain of the NTF increases [21]. A high NTF gain will decrease feedback loop resilience against non-idealities, such as the excess-loop delay or clock jitter [22]. To navigate this trade-off, we select f_{NSP} to be 10 times f_{BW}, or 100 MHz, which is 1/7–1/27 of the f_s.

Calculating the number of noise shaping stages from Eq. 10 with the chosen parameters gives n = 2.44–2.73 i.e. 3 stages. The resulting loop filter has a total of four stages where the first one provides gain and filtering and the following three ensure that the inband quantization noise is shaped below the thermal noise level. Next, the loop-filter coefficients need to be determined. Implementing an A_{OL} = 13.3 dB and the chosen bandwidth requires that when normalized to f_{BW}, $a_1 = 9.25$ and $b_1 = 1$. In order to avoid peaking, Butterworth coefficients are used in the noise shaping stages. The initial coefficients of the noise shaping stages are first normalized to f_{BW} and then scaled so that $a_k = G_k b_k$, where G_k is the gain of respective DSM filter stage. This results in dynamic range scaling, setting the dc gain of each noise shaping stage to unity. The initial and the scaled coefficients are listed in Table 1.

Based on above calculated coefficients, the STF of the proposed DDSR can be derived as:

$$\frac{a_2 a_3 a_4 h_{rf} H_I^3}{1/H_Q + a_2 a_3 a_4 h_{fb} H_I^3 + a_3 a_4 b_2 H_I^3 + a_4 b_3 H_I^2 + b_4 H_I}, \tag{11}$$

where H_I is the integrator transfer function. For an ideal integrator it is 1/s.

3.3 Loop filter implementation

Figure 3 shows the block diagram of the proposed DDSR. The first integration stage consists of the LNA, down-converting passive mixers and integration capacitances at the baseband, which form an N-path filter. The second, third and fourth stage are implemented as g_mC integrators. The noise performance of each stage is dependent on their transconductance g_m, and thus the LNA and the g_m stages are designed first. The LNA performance sets the noise figure to be roughly 5 dB, while the later stages are designed so that their contribution is minimal. Based on the designed g_m of the stages, we can calculate the capacitances $C_{1\text{-}4}$ of the DSM loop filter and the feedback transconductances $g_{m,\ fb,1\text{-}4}$ as [10, 23]:

$$C_1 = \frac{\sqrt{2}}{\pi^2} \frac{g_{m,LNA}}{a_1 2 f_{BW}} \frac{R_{LNA}}{R_{LNA} + R_{SW}}, \tag{12}$$

$$C_{2-4} = \frac{g_{m,2-4}}{2\pi a_{2-4} f_{BW}}, \tag{13}$$

$$g_{m,fb,2-4} = \frac{g_{m,2-4}}{G_{2-4}}, \tag{14}$$

$$g_{m,fb,1} = \frac{h_{RF}/(2A_{OL} - 1)}{h_{fb}}, \tag{15}$$

$$h_{RF} = \frac{\sqrt{2}\pi g_{m,LNA} R_{LNA} R_{BB} R_{SH}}{4R_{BB}(R_{LNA} + R_{SH} + R_{SW}) + \pi^2 R_{SH}(R_{LNA} + R_{SW})}, \tag{16}$$

$$h_{fb} = \frac{4R_{BB}(R_{LNA} + R_{SW})}{2R_{LNA} + 2R_{SW} + R_{BB}}, \tag{17}$$

$$R_{SH} = \left(\sum_{n=3,7,11..}^{\infty} \frac{1}{n^2 R_S^*(nf_{LO})} + \sum_{n=5,9,13..}^{\infty} \frac{1}{n^2 R_S(nf_{LO})} \right)^{-1} \tag{18}$$

where R_{LNA} is the output impedance of LNA, R_{BB} is the parallel combination of C_1 impedance and input impedance of first BB amplifier, $G_{2\text{-}4}$ is the gain of respective DSM stages, h_{RF} is the transfer function from the LNA input to the first BB output, h_{fb} is the transfer function for the negative DSM feedback from DDSR output to first BB input and R_{SH} represents the virtual shunt impedance representing the power dissipation due to baseband signal upconversion.

The final values of the circuit parameters are provided in Table 2.

Table 1 Loop-filter coefficients

Coefficient	a_1	a_2	a_3	a_4	b_1	b_2	b_3	b_4
Initial	9.25	1	1	1	1	1	2	2
Scaled	9.25	5	10	20	1	5	10	20

Table 2 Circuit parameters

Parameter	Value
$g_{m,LNA}$ [mS]	80
$g_{m,2}$ [mS]	23
$g_{m,3}$ [mS]	2.6
$g_{m,4}$ [mS]	2.6
C_1 [pF]	28
C_2 [pF]	73.2
C_3 [pF]	4.14
C_4 [pF]	2.07
$g_{m,fb,1}$ [mS]	2.6
$g_{m,fb,2}$ [mS]	23
$g_{m,fb,3}$ [mS]	2.6
$g_{m,fb,4}$ [mS]	2.6

3.4 Positive feedback implementation

Finally, positive feedback is implemented across the designed DDSR loop-filter. The required feedback factor β_{req} is implemented by selecting a proper value for $g_{m,IDAC}$ and R_{POS}. The resulting closed loop gain is equal to the required A_{CL} = 20 dB and the input matched. However, the implementation of positive feedback reduces the bandwidth of the proposed DDSR. In order to circumvent the problem, the N-path capacitance C_1 needs to be scaled with a scaling factor of A_{OL}/A_{CL} to match the desired bandwidth. The final value of C_1 can be found as:

$$C_{1,scaled} \approx C_1 \frac{A_{OL}}{A_{CL}} \tag{19}$$

where A_{OL} and A_{CL} are open and closed-loop gains on linear scale.

Based on the system model and design equations presented earlier, Fig. 6 plots the required analytical transfer function for the proposed receiver.

4 System implementation

The DDSR is designed for an receiver gain of 20 dB. The RF front-end consists of a transconductor implementation with a parallel combination of common-gate CG and push-pull common-source CS amplifiers [16]. A common-gate amplifier is a valid choice as he input impedance can be easily controlled through common-gate transconductance. Figure 7(a) shows the circuit diagram of the designed transconductor. The parallel CG and CS combination increases the transconductor gain, and the push-pull configuration helps to achieve better large signal linearity. To maximize output voltage swing range of the transconductor, the output common-mode voltage is set to half of the supply voltage by implementing a common-mode feedback loop. Blocker filtering at the transconductor input is achieved by designing a low intrinsic input impedance

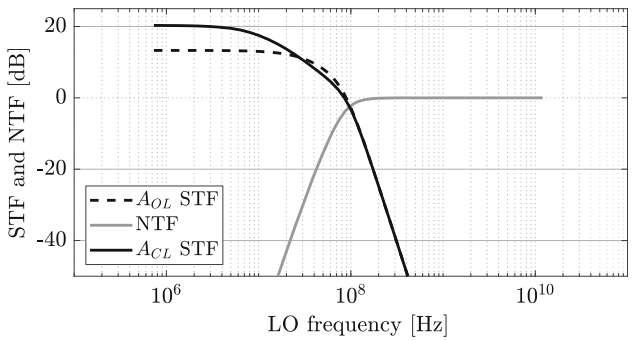

Fig. 6 Analytical transfer function of the proposed receiver based on the system model and design equations

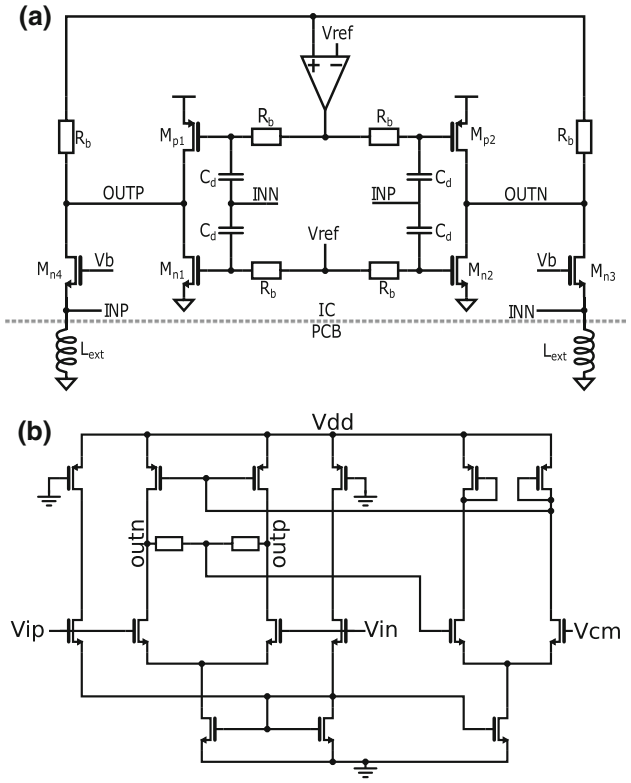

Fig. 7 Implemented circuits **a** common-gate common-source (CG–CS) transconductor **b** baseband transconductor

(R_{INT}) of the transconductor while for desired frequency R_{INT} is boosted to match source impedance (R_S) through implementation of up-converted positive feedback from the baseband (BB) output.

Ideally, the intrinsic input impedance of the LNA should be 0 Ω. However, due to practical limitations of LNA transconductor power consumption, differential intrinsic input impedance is designed to be 30 Ω. This intrinsic impedance is then boosted to matched condition by the positive feedback from the DDSR output to RF nodes through passive quadrature mixers. The amount of positive feedback can be controlled through positive feedback IDAC's transconductance $g_{m,IDAC}$ and series resistance R_{POS}. Based on the analytical derivations from previous sections, we choose a $g_{m,IDAC}$ = 5.3 mS. As implementation of positive feedback is prone to instability, process corner simulations were carried out, for the chosen $g_{m,IDAC}$, to ensure the stability of the system in all process corners.

Downconversion mixers in the main signal path were implemented as quadrature passive mixers driven with 25% duty cycle LO waveforms. Transistors with a large aspect-ratio of 48/0.03μm are implemented in the main path downconversion mixers. This ensured a small switch resistance of 8 Ω for better attenuation at far away offsets from f_{LO}. As there was no such requirement of smaller R_{SW} for the positive feedback mixers, their aspect ratio was

selected to be four times smaller than main path mixers (12/0.03μm i.e. R_{SW} = 32 Ω).

The later integrators were implemented with consecutively higher noise contribution. This is because once the gain is implemented in the system, later stages noise contribution is reduced by the amount of added gain. Therefore, there is no need for the later stage noise contribution to be low. Figure 7(b) shows the implemented dynamically-biased BB transonductors. All baseband amplifiers are designed with the same configuration as shown in Fig. 7(b) with the small exception of designing the first baseband transconductor with a transconductance of 23 mS and bias current of 3.8 mA. This is about 10 × higher the the bias currents of later baseband stages to ensure reduced noise contribution from the first baseband amplifier. Capacitors C_1–C_4 implement the required BB bandwidth bandwidth cutoff frequency (f_{BW}) and noise shaping pole cutoff frequency (f_{NSP}) in the DSM loop filter. Their values were selected based on the calculations from the previous section and are provided in Table 2.

The quantizer and feedback DACs were implemented as behavioral models. Nevertheless, the most important non-idealities of quantizer and feedback DAC such as clock-delay between DAC and quantizer and noise of DAC transistors were added to closely match the simulated behavior with real circuits.

5 Performance evaluation

The proposed DDSR was evaluated in a 28 nm fully-depleted silicon-on-insulator (FD-SOI) process through transient and steady-state AC simulations. The DDSR is reconfigurable from 0.7–2.7 GHz with a f_{BW} of 10 MHz. Further, based on our previous implementation [6], we added estimated values I/O pad capacitances, bondwire inductances, s-parameter models of 20 nH off-chip RF-chokes, and clock delay between the quantizer and IDACs in order to match the simulated results more closely to the real scenario.

The spectrum of the DDSR output bit stream for an input signal and blocker power of − 43 dBm is shown in Fig. 8. A few key points can be observed. First, the desired in-band signal is amplified with about A_{CL} = 20 dB of receiver gain. Second, the blocker at 73 MHz offset from f_{LO} is filtered by the baseband filtering response, and third, the quantization noise is shaped by the DDSR feedback loop such that the in-band quantization noise is lower than thermal noise floor.

Figure 9 shows the simulated steady-state AC analysis results of DDSR gain and S_{11}. As desired, A_{CL} = 20 dB is observed within the 20 MHz RF bandwidth. Further, a

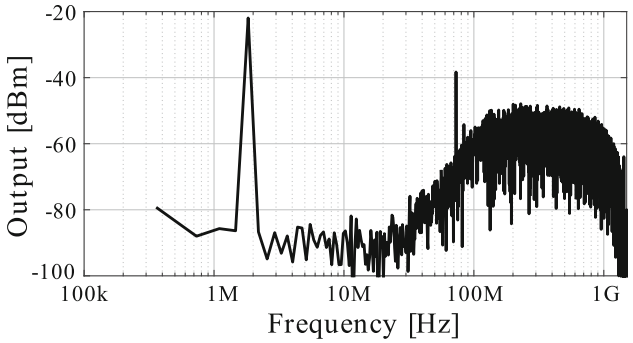

Fig. 8 Output spectrum at $f_{LO} = f_S$ = 1.5 GHz, P_{IN} = − 43 dBm@f_{LO} + 1.83 MHz, $P_{BLOCKER}$ = − 43 dBm@f_{LO} + 73 MHz and f_{BW} = 10 MHz

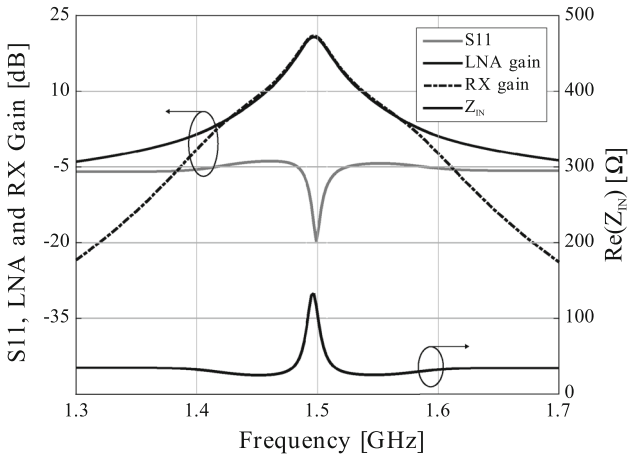

Fig. 9 Simulated S_{11}, LNA and BB gain for f_{LO} = 1.5 GHz

differential out-of-band input impedance of 30 Ω can be seen needed for blocker attenuation at LNA input.

Figures 10 show the receiver SNDR versus input signal and blocker powers. the receiver achieves a maximum SNDR of 53 dB at P_{IN} of − 43 dBm. Further, we observe a decrease in SNDR from at blocker input powers greater than − 35 dBm for an input signal power of − 80 dBm. At low signal powers, the difference between ideal and simulated SNDRs is approximately equal to receiver NF.

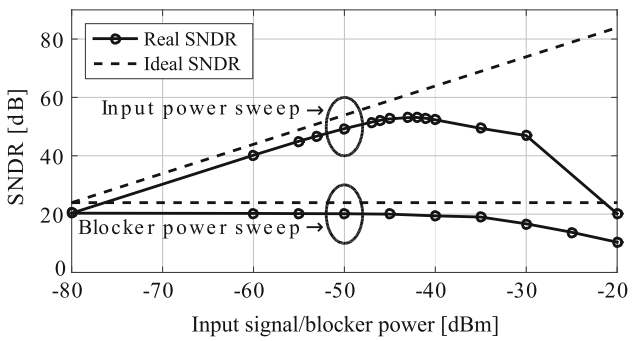

Fig. 10 SNDR versus input and blocker power for f_{LO} = 1.5 GHz

Figure 11 presents a comparison of the simulated SNDR for cases when f_S = 1.5 GHz and $f_S = f_{LO}$. It can be seen that for a constant f_S = 1.5 GHz, SNDR degrades from its maximum value for $f_{LO} \neq nf_S/2$, here n is an integer number. This degradation occurs due to the quantization noise upconversion effect inherent in DDSR architectures [5]. However, in the proposed structure, the degradation of SNDR due to quantization noise upconversion is much more severe than in a traditional DDSR. This is due to bringing the DDSR feedback to the input of receiver rather than to the LNA output. As there is no preceding gain stage before this input, the upconverted quantization noise effect is more severe on achieved SNDR. The problem was solved in the final design by choosing $f_{LO} = f_S$ for the entire band of operation. As can be seen in Fig. 11, this ensures that the degradation of SNDR due to quantization noise upconversion effects is minimal.

Figure 12 presents the SNDR versus clock delay for two different sampling frequencies of f_S = 0.7 GHz and 1.5 GHz. The clock delay is defined from the rising edge f_S to the instant when output of IDAC begins to change. It can be seen that the DDSR loop is able to handle about 70 ps of delay, in the worst case f_S = 0.7 GHz, before the SNDR begins to degrade rapidly. At higher sampling frequencies, DSM loop is able to handle much longer delays than 70 ps. This is because a higher sampling frequency brings the response more close to a continuous time filter with more resilience towards clock delay. While the delay of 70 ps is still implementable in the given process, the process variations can increase the delay to be higher than 70 ps. Therefore, a better solution for worst case scenario of f_S = 0.7 GHz will be to lock $f_S = 2f_{LO}$. Locking $f_S = 2f_{LO}$ for the worst case scenario minimizes SNDR degradation due to quantization noise upconversion.

In addition to clock delay, the supply noise can also affect the maximum SNDR of the receiver. Figure 13

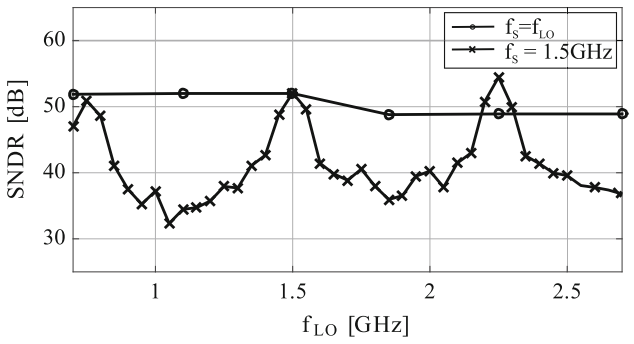

Fig. 11 A comparison of SNDR versus f_{LO} for cases when f_S = 1.5 GHz and when $f_S = f_{LO}$. The quantization noise upconverison effect degrades the SNDR for $f_{LO} \neq nf_S/2$. The problem resolved by locking $f_S = f_{LO}$

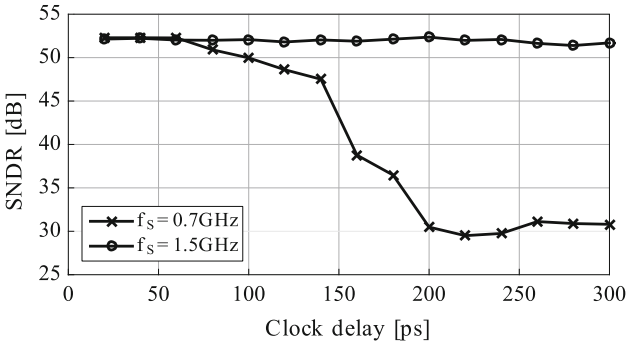

Fig. 12 SNDR versus clock delay for the two different sampling frequencies of f_S = 0.7 GHz and 1.5 GHz. DDSR loop is able to handle about 70 ps delay, in worst case of f_S = 0.7 GHz, after which the SNDR starts to degrade rapidly

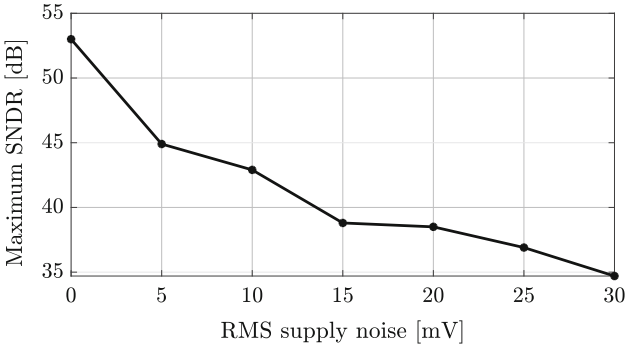

Fig. 13 Maximum SNDR versus RMS supply noise of the receiver

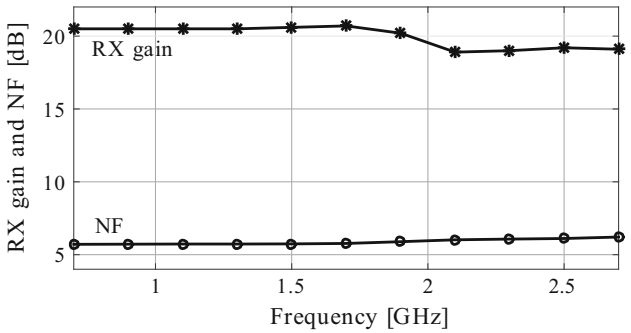

Fig. 14 RX gain and noise figure across the 0.7–2.7 GHz operating band

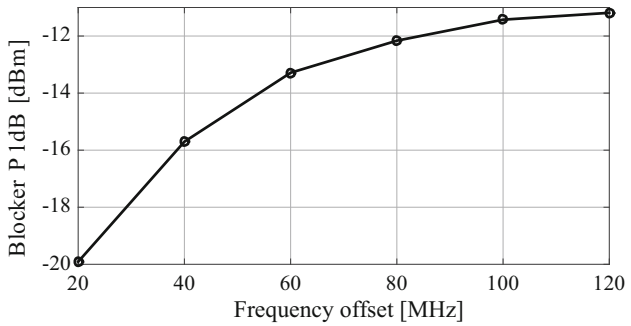

Fig. 15 Blocker compression point (BCP) versus frequency offset for the proposed receiver at f_{LO} = 1.5 GHz

Table 3 Performance summary and comparison

	This work[f]	[9]	[6]	[5]	[11]
Carrier frequency (GHz)	0.7–2.7	0.6–3	0.7–2.7	0.9	0.1–1.5
Gain (dB)	20	50	–	40	38
Noise figure (dB)	5.6–6.2	2.4–3.5	5.9–8.8	6.2	1.5–2.9
Blocker input P1dB[a] (dBm)	$-11.5@10f_{BW}$	$-20@10f_{BW}$	$-14@10f_{BW}$(2	$-18@20f_{BW}$	$-17@10f_{BW}$
OB IIP3 (dBm)	$0@10f_{BW}$	$-10@10f_{BW}$	$-4@10f_{BW}$[b]	–	–
Peak SNDR (dB)	53	52	43	56	–
BB bandwidth (f_{BW}) (MHz)	10	10	7.5	28[c]	2
Power (mW) @ supply voltage (V)	25@1[e]	35.5–53.5@1.2	90@1.1	80@1.2	11@0.7,1.2[d]
Architecture	LNA first DDSR	LNTA first DDSR	LNA first DDSR	LNA first DDSR	Mixer first receiver
Process	28 nm FDSOI	65 nm CMOS	40 nm CMOS	65 nm CMOS	65 nm CMOS

[a]Blocker offset normalized to BB bandwidth (f_{BW})

[b]Extrapolated value

[c]Usable BW with acceptable NF is limited to 4 MHz

[d]at RF

[e]Power consumption of receiver excluding quantizer and IDACs

[f]Simulated response

shows the performance of receiver SNDR under the presence of supply noise.

Figures 14 and 15 show the simulated NF, receiver gain and blocker input compression point (BCP). The receiver achieves a BCP of − 11.5 dBm at 100 MHz offset from f_{LO} with a maximum integrated receiver NF of 6.2 dB. When compared with BCP results collected into Table 3, the proposed approach is able to promising blocker tolerance even with its lower supply voltage.

6 Conclusion

We have proposed a blocker resilient DDSR with a low intrinsic input impedance front-end. It reduces blocker gain already at the LNA input by creating an on-chip tunable bandpass response. Furthermore, we proposed a reduced receiver gain design that helps to minimize near-band blocker gain. This ensures that the voltage swing limits are pushed towards much stronger blockers. The simulated results demonstrate an OB blocker compression point of − 11.5 dBm and OB-IIP3 of 0 dBm at 100 MHz offset from the desired received frequency, with a maximum SNDR of 53 dB and a maximum NF of 6.2 dB. The results collected into Table 3 indicate that the proposed approach is able to achieve state-of-the art blocker tolerance even with its lower supply voltage.

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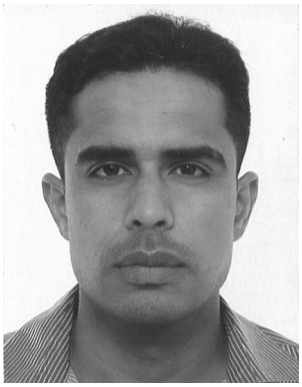

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