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Kossifos, Kypros M.; Petrou, Loukas; Varnava, Giorgos; Pitilakis, Alexandros; Tsilipakos, Odysseas; Liu, Fu; Karousios, Petros; Tasolamprou, Anna C.; Seckel, Manuel; Manessis, Dionysios; Kantartzis, Nikolaos V.; Kwon, Do Hoon; Antoniades, Marco A.; Georgiou, Julius

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Published in:
IEEE Access

DOI:
10.1109/ACCESS.2020.2994469

Published: 01/01/2020

Document Version
Publisher's PDF, also known as Version of record

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Please cite the original version:
Kossifos, K. M., Petrou, L., Varnava, G., Pitilakis, A., Tsilipakos, O., Liu, F., Karousios, P., Tasolamprou, A. C., Seckel, M., Manessis, D., Kantartzis, N. V., Kwon, D. H., Antoniades, M. A., & Georgiou, J. (2020). Toward the Realization of a Programmable Metasurface Absorber Enabled by Custom Integrated Circuit Technology. *IEEE Access*, *8*, 92986-92998. Article 9092996. https://doi.org/10.1109/ACCESS.2020.2994469

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IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received March 27, 2020, accepted April 26, 2020, date of publication May 14, 2020, date of current version June 1, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2994469

Toward the Realization of a Programmable Metasurface Absorber Enabled by Custom Integrated Circuit Technology

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This work was supported by the European Union's Horizon 2020 Future Emerging Technologies Call (FETOPEN-RIA) Project VISORSURF under Grant 736876.

ABSTRACT The realization of a programmable metasurface, enabled by a custom application-specific integrated circuit (ASIC), is presented in this paper. The ASIC is used to provide an adaptive complex impedance load to each of the metasurface unit cells. Various technology nodes are analyzed for the implementation of tunable complex impedance loading elements before one is selected for the final implementation, in which four complex loads are placed within each integrated circuit, and each load is controlled by two digital-to-analog converters. Furthermore, the ASICs populate the back of the metasurface to form a mesh network to enable programmability. The paper includes practical limitations that affect the realization, as well as an example adaptive metasurface absorber that builds upon the practical tuning range of the ASIC. Perfect absorption for both transverse electric and transverse magnetic polarization is demonstrated.

INDEX TERMS Metasurfaces, ASIC, programmable RF load, perfect absorption, reconfigurable.

I. INTRODUCTION

Metamaterials are composite materials that exhibit properties that are not found in nature. A negative refractive index is one of the many exotic properties that metamaterials possess. It was initially speculated in [1] and experimentally demonstrated in [2] that a negative refractive index can be realized when the electric permittivity and magnetic permeability are both negative. Metamaterials have also demonstrated the ability to resolve beyond the diffraction limit in free space [3] by designing the refractive index to be equal to -1, and cloaking by manipulating the electromagnetic waves around an object [4]. These are just some of highlights of the metamaterial properties. Metamaterials have since also been used to improve the performance of countless components in RF/microwave and antenna design ([5]–[8]).

Metasurfaces, the two-dimensional versions of metamaterials have gained interest by researchers in the past decade. Like their three-dimensional counterparts, they have demonstrated many exotic properties such as anomalous reflection [9]–[12], perfect absorption [13] and non-linear reflection [14]. By loading the metasurfaces with lumped elements the metasurface response can be altered [15]. These lumped elements can be replaced with tunable varactors

The associate editor coordinating the review of this manuscript and approving it for publication was Yasar Amin.

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or varistors and create electronically tunable metasurface reflectors [16], [17] and absorbers [18], [19]. Other means of obtaining tunable metasurfaces have been shown, like magnetic tunability [20], optical tunability [21] and even by exploiting the optomechanical properties of poly disperse red 1 acrylate to optically tune metasurfaces with a memory effect [22], [23].

Metasurfaces have demonstrated the ability to synthesize wavefronts through the individual design of their constituent unit cells. In [24] multi-beam reflection and simultaneous polarization conversion was demonstrated. Isoflux patterns with circular polarization were demonstrated in [25] and local multipoint distribution service patterns were demonstrated in [26].

Dynamic wavefront manipulation was also demonstrated by programmable metasurfaces. Dynamic scattering, focusing and polarization rotation was implemented in [27]. Dynamic control of the modulation of the reflection phase resulted in accurate control of the harmonic level of a non-linear reflecting metasurface [14]. Programmable metasurfaces were utilized to implement reflective [28] and transmissive [29] holograms in the microwave regime.

The conceptual design of this work was presented in [30], where individual electronically tunable complex impedance metasurface loading elements, consisting of resistive and capacitive (*RC*) elements, were embedded in each unit cell to obtain a reconfigurable multifunctional metasurface. It was shown that in using this approach, continuous control over the real and imaginary parts of the complex surface impedance can be obtained, thus enabling the shaping of the spatial profile of both the reflection amplitude and phase, leading to maximum versatility in the achievable functions. In this paper, the design methodology is presented, including the steps taken to implement the programmable metasurface concept by taking into account manufacturing and cost limitations. The programmable metasurface consists of a top textured layer, exposed to the EM waves, an intermediate ground plane layer, and two routing layers on the bottom, to provide control and power to the application-specific integrated circuits (ASIC) that are used to program the metasurface. The ASICs are populated on the bottom side in an array structure. In order to reduce the cost and to conform to tight space constraints, a single ASIC design must operate without the need for any further components. As will be subsequently elaborated upon, the ASIC contains both low-power, metasurface loading elements, as well as asynchronous circuits implementing a grid communication algorithm, as presented in [31]. This paper includes realistic loading element tunability ranges, extracted from three candidate semiconductor technology process design kits (PDKs). Furthermore, the paper outlines various metasurface PCB manufacturability issues. Finally the paper shows that the ASIC can be used to create a programmable metasurface, also known as a hypersurface [32], which demonstrates programmed perfect absorption, for a range of incident angles for both TE and TM polarizations.

II. PROGRAMMABLE METASURFACE UNIT CELL

An example unit cell topology can be seen in Fig. 1. It consists of a textured metasurface pattern on the top layer (L_1), a ground plane in the middle layer (L_2), communication and power distribution layers (L_3 and L_4), with the ASIC bonded to the bottom layer (L_4). The ASIC on the bottom layer, containing the metasurface loading elements, has four direct vias that route the RF signals between the bottom layer (L_4) and the top layer (L_1).

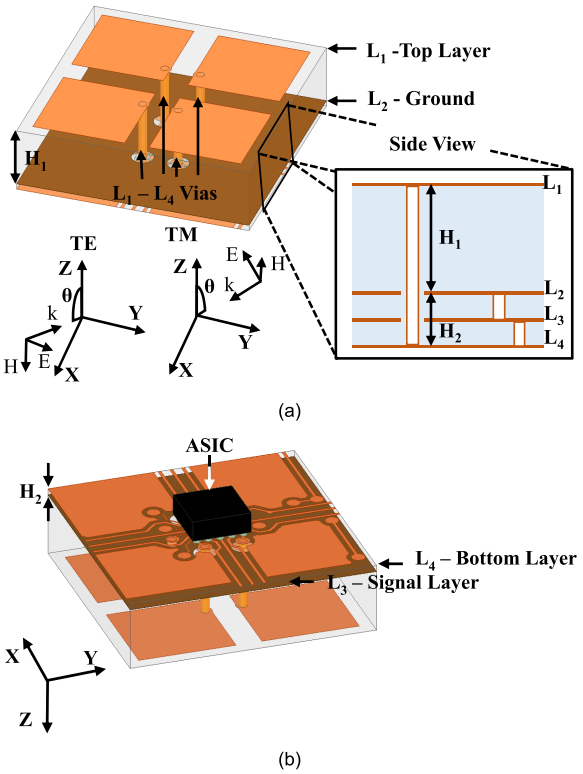

FIGURE 1. Metasurface unit cell geometry. (a) Top side of the unit cell and (b) bottom side of the unit cell showing the location of the metasurface loading application-specific integrated circuit (ASIC).

The example unit cell topology in Fig. 1, which has a subwavelength size of $\lambda/7$, is periodically repeated to form the complete metasurface that occupies a total area of $5 \times 5\ \lambda^2$, at the design frequency (5 GHz). Fig. 2 shows an array of unit cells, with the top view, (a), showing the textured square patch pattern, while the bottom view, (b), shows the metasurface loading ASIC that is placed in every unit cell.

The general topology was chosen after carefully considering other available options, e.g. the ASIC could lie on the top layer or even be embedded within the PCB. The first example was discounted since having metallic tracks that carry power and communication signals on the top layer will adversely affect the electromagnetic behavior of the metasurface. Secondly, if the ASIC were to be embedded in the metasurface PCB, it would not only need a specialized, high-cost, PCB process, but also would render the hypersurface irreparable in case of ASIC faults. Given the large number of

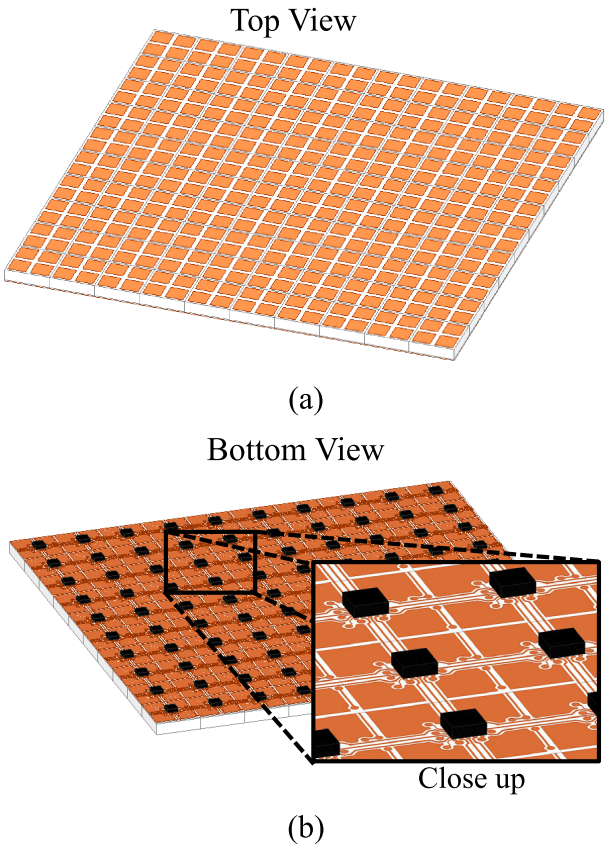

FIGURE 2. Illustration of a metasurface composed of 10 × 10 unit cells. (a) Top side and (b) bottom side showing the metasurface loading ASICs.

ASICs needed to create a hypersurface, the probability of one ASIC failing or having a dry solder joint is increased. Thus, serviceability is of paramount importance in the selection of the topology.

The design cycle of a metasurface, like the one shown in Fig. 1, requires a careful design balancing act that takes into account multiple practical constraints. The metasurface presented is designed to perform as an absorber at normal and oblique incident angles. As it will be shown in section II.A, this entails that the loading ASIC will need to cover the required *RC* range for its operation. In the current example, the range required for the resistance is relatively low, and hence works at the limits of the practical range found in IC implementations, as it is shown in Section III. This constraint can be relaxed by implementing the hypersurface on a thicker substrate (H_1) and by employing a substrate with lower dielectric losses, resulting in higher resistance value requirements. An example of the manufactured thicker PCB stack is shown in detail in Section IV.

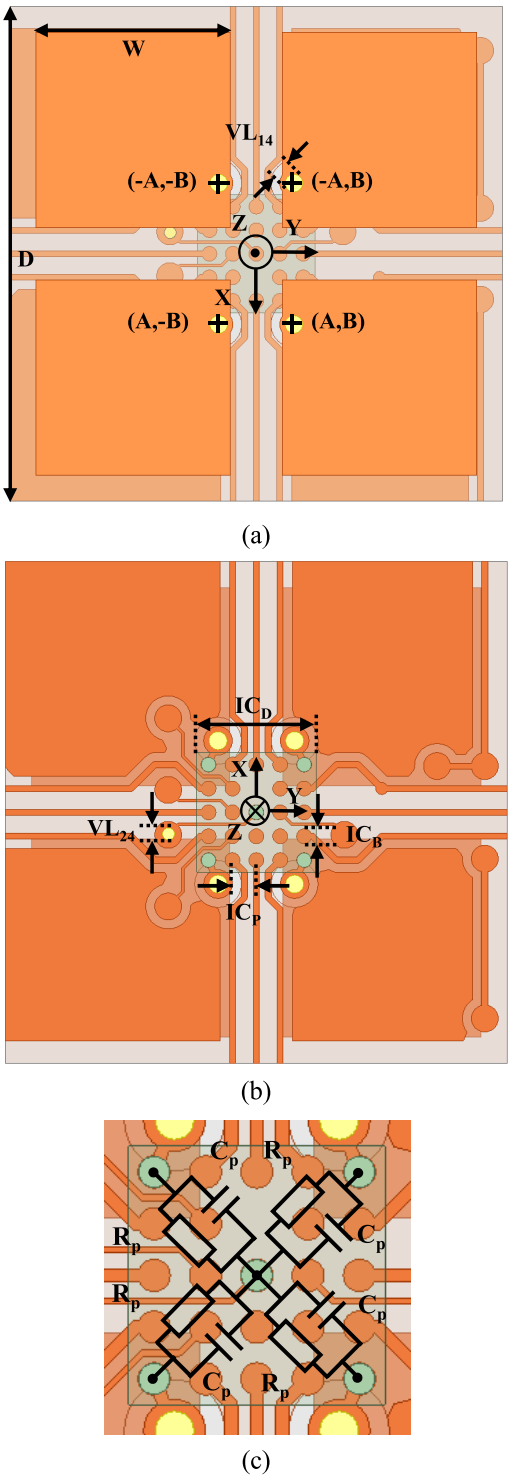

FIGURE 3. Metasurface unit cell geometry. (a) Top side, (b) bottom side, and (c) close-up of the bottom side, showing the location of the metasurface loading ASIC.

A. DESIGN OF PROGRAMMABLE METASURFACE

The example unit cell design is elaborated in Fig. 3. The details of the geometric parameters are listed in Table 1. An optimized parameter that is sensitive for the performance of the metasurface absorber is the position of the L_1-L_4 vias connecting the patches in L_1 to the ASIC terminals in L_4. As described in [33], the optimal position for an isotropic cell would be in the corner of the patches, where the surface current density is larger. Unfortunately, due to various fabri-

TABLE 1. Unit cell geometry.

Geometric parameter	Dimensions (mm)	Description
H_1	2.137	Top Substrate Thickness
H_2	0.255	Bottom Substrate Thickness
D	8.4	Period of the Unit Cell
W	3.32	Width of the Patch
A	1.2	X-Coordinate of L_1-L_4 Via
B	0.641	Y-Coordinate of L_1-L_4 Via
VL_{14}	0.30	Diameter of L_1-L_4 Via
VL_{24}	0.15	Diameter of L_2-L_4 Via
IC_D	2.00	IC Dimensions
IC_P	0.40	IC Pitch
IC_B	0.25	IC Pad Diameter

cation limitations this option was not available, so the vias were placed near the inner edge of patches along one direction, as shown in Fig. 3, so that at least one polarization would be optimally covered. The methodology for the optimization of the "free" absorber unit-cell parameters, namely the width of the patches and the period of the cell, is described in [33], under the constraints of: operating frequency, manufacturing (through via position), dielectric thicknesses, IC size and available RC range.

In Fig. 3(a) and (b) a top and bottom view of the unit cell and is shown. Fig. 3(c) depicts the connectivity of the ASIC to the metasurface from the edge pins. The ASIC in this design loads the metasurface with four parallel-connected *RC* loads, as shown in Fig. 3(c). The design of the metasurface loads, along with their control circuit will be discussed in Section III.

The IC uses wafer level chip scale packaging (WLCSP). The solder balls are also included in the simulations, and are each modelled as a cylinder of height 0.15 mm and diameter 0.25 mm. The solder ball used was alloy SAC405 in order to accurately take into account its effect on the design.

The realizable unit cell was designed by taking into account practical limitations of the ASIC and the PCB technology. These limitations include *R* and *C* ranges, cost of the semiconductor process, maximum PCB thickness, via and track sizes, and substrate losses.

As can be seen in Table 1, H_1 is much larger than H_2, in order to relax the ASIC's constraint on the realization of the resistance values, and H_2 should be small, so that the power and ground supplied to the ASIC is of good quality. The asymmetric layer stack of the PCB improves the RF performance of the metasurface, however care must be taken with an increased number of layers as they introduce additional variations in the PCB thickness.

The metasurface unit cell was co-simulated using an electromagnetic model that was combined with the lumped *RC* loads. The absorbance performance, shown in Fig. 4, was obtained through the use of circuit and electromagnetic co-simulations in CST. The unit cell simulations take into account the existence of traces and metallic fill layers that are implemented in Altium Designer and checked to comply with

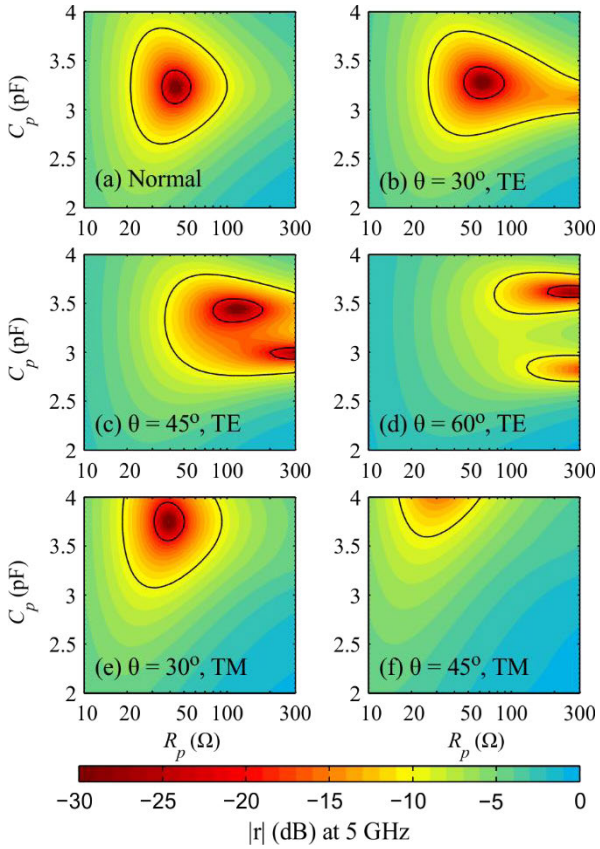

FIGURE 4. Reflection coefficient magnitude in dB at 5 GHz for (a) normal incidence, (b) TE $\theta = 30°$, (c) TE $\theta = 45°$, (d) TE $\theta = 65°$, (e) TM $\theta = 30°$ and (f) TM $\theta = 45°$.

the PCB design rules. These traces are used for signaling, power and communication. More information on the use of these traces can be found in Section IV.

The example unit cell geometry targeted a perfect absorber at a design frequency of 5 GHz. At this frequency, absorption of TE-polarized waves (see legend in Fig. 1) was studied at various angles of θ while keeping the angle $\varphi = 0°$, corresponding to the *xz*-incidence plane with reference to Fig. 3(a). The absorption of TM-polarized waves was studied at various angles of θ at an orthogonal plane with respect to the TE polarization ($\varphi = 90°$), corresponding to the *yz*-incidence plane with reference to Fig. 3(a). This discrimination between the TE and TM planes of incidence is caused by the asymmetric connection (in the *x*- and *y*-directions) of the L1-L4 vias to the metasurface patches on the top layer, as shown in Fig. 3(a). The discrimination between the TE and TM planes for y-polarized incidence arose as a tradeoff between fabrication limitations, available loading impedance ranges and our target for angle-tunable perfect absorption for at least one polarization [33]. Oblique TM polarization has narrower angle tunability due to the E-field component parallel to the vertical vias (L1-L4 and L4-L2) which gives rise to currents and mutual coupling between the lateral traces of the grounding and RF terminals (in L4). Finally, x-polarized incidence in both TE and TM planes will severely

underperform due to the trade-off mentioned; the physical reason is the large distance of the through vias to the edges of the patches along the x-axis, Fig. 3(a).

In Fig. 4(a) the reflection coefficient for normal incidence ($\theta = 0°$) is shown, indicating that perfect absorption (|r| <-30 dB) is obtained at the center of the plotted RC range. Note that the result is almost indistinguishable for TM polarization, but not identical due to the asymmetric placement (in the x- and y-axes) of the L_1-L_4 vias with respect to the metasurface patches on the top layer (Fig. 3(a)), something that was done to obtain good performance for large oblique incidence angles for at least one, the TE, polarization, see also [33].This can be seen in Fig. 4(b), (c) and (d) where the reflection coefficient for TE polarization is shown for $\theta = 30°$, 45° and 60°, respectively. It can be seen that the required resistance and capacitance for perfect absorption increase for larger oblique angles of incidence, but a very low reflection amplitude can be obtained inside the considered RC range. Note that two absorption peaks appear for larger angles and can be both exploited [33]. In Fig. 4(e) and (f) the reflection coefficient for TM polarization is shown for $\theta = 30°$ and 45°, respectively. It can be seen that the required RC combination shifts towards higher capacitances for larger oblique angles of incidence. For this polarization, the reflection dip moves outside the considered RC range for angles exceeding 45° degrees, which could prove to be a limitation in the realization of the loading-element values.

III. METASURFACE LOADING ASIC

Numerous semiconductor technologies are commercially available for the implementation of the metasurface loading ASICs. The selection of a semiconductor technology offers new challenges in the design of a suitable integrated circuit for metasurface applications. Programmable metasurface designs, shown in the literature thus far, use commercial-off-the-shelf (COTS) components as loading elements, and programmable modules such as field-programmable gate arrays (FPGAs), to individually address each unit cell [14], [27]. This type of architecture separates the high-frequency RF electronic component of the design (the unit cell loading element) from the low-frequency analog and digital component (the FPGA). Typically, the RF loading elements operate at a higher frequency and are manufactured from high-performance and costly technologies, like silicon-germanium (SiGe) and even gallium-arsenide (GaAs), while the analog and digital control circuits are manufactured on cheaper silicon technologies.

This paper aims towards the realization of a programmable metasurface architecture that addresses individually each unit cell, and is capable of providing a complex loading impedance. This functionality necessitates that the high frequency loading elements are integrated together with the analog and digital control circuits on the same chip. Ideally, in order to realize high-quality RF loading elements, the whole integrated circuit would be designed in a high-frequency SiGe or GaAs process, however the large number of integrated circuits necessary to implement a large hypersurface would render the cost prohibitively high; therefore, a technology should be selected that can provide a sufficient range for the tunable complex impedance loading elements at the design frequency of 5 GHz, while also being economically feasible.

With the envisaged large number of ASICs needed for the hypersurface implementation, the power consumption of each IC needs to be carefully considered. In [27], each individual metasurface loading element required 10 mA of current in its ON state. This might appear small, but the metasurface consists of 40 × 40 unit cells, which translates to a total current consumption of 16 A, when all 1600 loading elements are ON. In order to reduce the overall current consumption, each metasurface loading element should be implemented with a negligible current draw, and since each unit cell is locally controlled, the digital and analog part should also be designed with minimum power requirements. In [34], the importance of using asynchronous control circuits for enabling programmable and scalable metasurfaces is argued. Asynchronous circuits offer a low power consumption for controllers that are idling most of the time, as in the case of controllable metasurfaces. Additionally, and more importantly for RF applications, electromagnetic emissions from this ASIC are inherently reduced, due to the data-driven clocking, as well the fact that a location setting can be changed without clocking the entire surface. Finally, by using asynchronous clocking there is no need for a power hungry clock distribution network on the entire metasurface.

The packaging of the metasurface loading ASIC also needs to be taken in to account. The package will introduce additional parasitic affects that will reduce the overall range of the obtainable complex impedances, and can also increase the cost of the IC. For the chosen metasurface application, wafer level chip scale packaging (WLCSP) was chosen since it offers the cheapest packaging solution and introduces the least amount of parasitic affects [35], [36].

The top-level block diagram of the metasurface loading ASIC is shown in Fig. 5. It consists of four metasurface loading elements that consist of a voltage-controlled capacitor (varactor) in parallel with a voltage-controlled resistor (varistor). These LEs are connected between the outer pins of the chip and the center ground pin. The biasing for the metasurface loading elements is provided by eight on-chip digital-to-analog converters, that are set by data passed through four serial, asynchronous, unidirectional communication ports of the ASIC. These communication ports form a larger grid, within the metasurface, arranged in a Manhattan style architecture, as described in Section III B.

A. DESIGN OF METASURFACE LOADING ELEMENTS

In this section, an investigation is presented for three commercially-available candidate technologies. This is done using simulated results from Cadence Virtuoso, revealing the achievable complex impedance ranges for the metasurface loading elements. These are CMOS processes at the 350 nm,

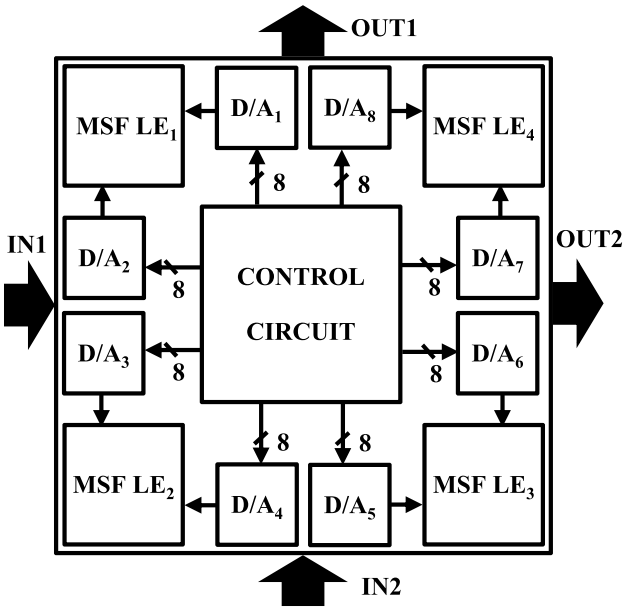

FIGURE 5. Top-level diagram of the metasurface loading ASIC showing the input/output (IN1, IN2, OUT1, OUT2), the four metasurface loading elements (MSF LEs), eight digital-to-analog converters (D/As), and the communication control circuit. The ASIC uses serial and unidirectional input/output communication.

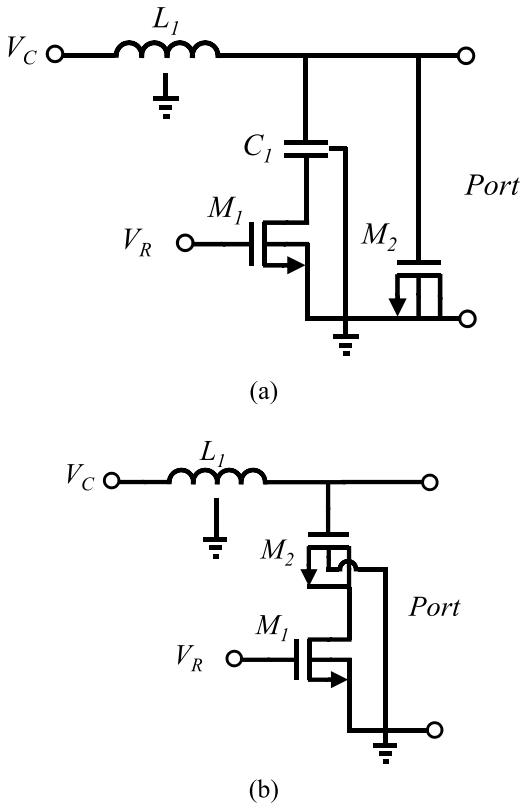

FIGURE 6. Two simplified metasurface loading element circuit topologies, (a) parallel topology and (b) series topology. Both consist of an RF choke (L_1), varistor (M_1) and varactor (M_2). The circuit of (a) includes an additional DC block capacitor (C_1).

180 nm and 65 nm technology nodes. Specialized SiGe and GaAs technologies are not investigated in this work, since they are costly and not widely available.

The metasurface loading element uses a MOSFET varactor to adjust the imaginary part of the complex impedance and a MOSFET varistor to control the real part of the complex impedance. These tunable elements can be placed either in a parallel topology (Fig. 6(a)) or a series topology (Fig. 6(b)). In both topologies the MOSFET varistor (M_1) is adjusted through a voltage supplied to its gate, V_R. The MOSFET varactor (M_2) is supplied by voltage V_C through an RF choke inductor (L_1). The parallel configuration uses an additional DC block capacitor (C_1) to prevent the biasing voltage V_C from shorting through the varistor (M_1) when V_R is applied to its gate. In both of these topologies the steady-state current draw is mainly attributed to gate leakage and is negligible.

The supplied voltages V_R and V_C are progressively increased from zero to the maximum allowed operating voltage of the technology or to a large enough voltage that does not provide any further impedance tuning. For each set of V_R and V_C voltages, this corresponds to a specific *RC* combination. Thus, by varying both V_R and V_C, an area of *RC* combinations can be created within an *RC* map, which defines the achievable *RC* values for that technology.

The *RC* area of each loading element needs to cover the optimum *RC* combinations required by the metasurface unit cell to achieve perfect absorption, which are shown in Fig. 4. This has proven difficult to achieve in simulations with the series configuration (in all three of the evaluated technologies), since the varistor (M_1) needs to have a large number of fingers to achieve the required low resistance. The large number of fingers also means that its parasitic capacitance to the substrate is also moderately large, thus effectively short-circuiting it at the design frequency.

The parallel configuration showed more promise in achieving the required low resistance. In order to evaluate the performance of each technology, each device (M_1, M_2, L_1, C_1) was adjusted to increase the parallel *RC* range and satisfy the optimum *RC* combinations.

The adjusted parallel configuration *RC* ranges can be seen in Fig. 7 (a), (b) and (c) for the 350 nm, 65 nm and 180 nm technologies, respectively. The results of Fig. 7 were obtained using data from S-parameter simulations and converting the reflection coefficient at the Port on the right-hand side of the parallel loading element circuit of Fig. 6(a) to a parallel configuration *RC* map. With this conversion to a simple equivalent parallel configuration, consisting of a simple parallel *RC* circuit, all the complex technology device models collapse into a single *RC* map that can be easily compared between the different technologies, and can be used to evaluate the metasurface performance. Constant V_R lines are shown in solid blue lines in the Fig. 7, and constant V_C lines are shown in dashed red lines.

It can be seen in Fig. 7 that for larger feature technologies the capacitance range increases, while the resistance range decreases. The reduction of the resistance range in the larger feature technologies is caused by a reduction of the quality

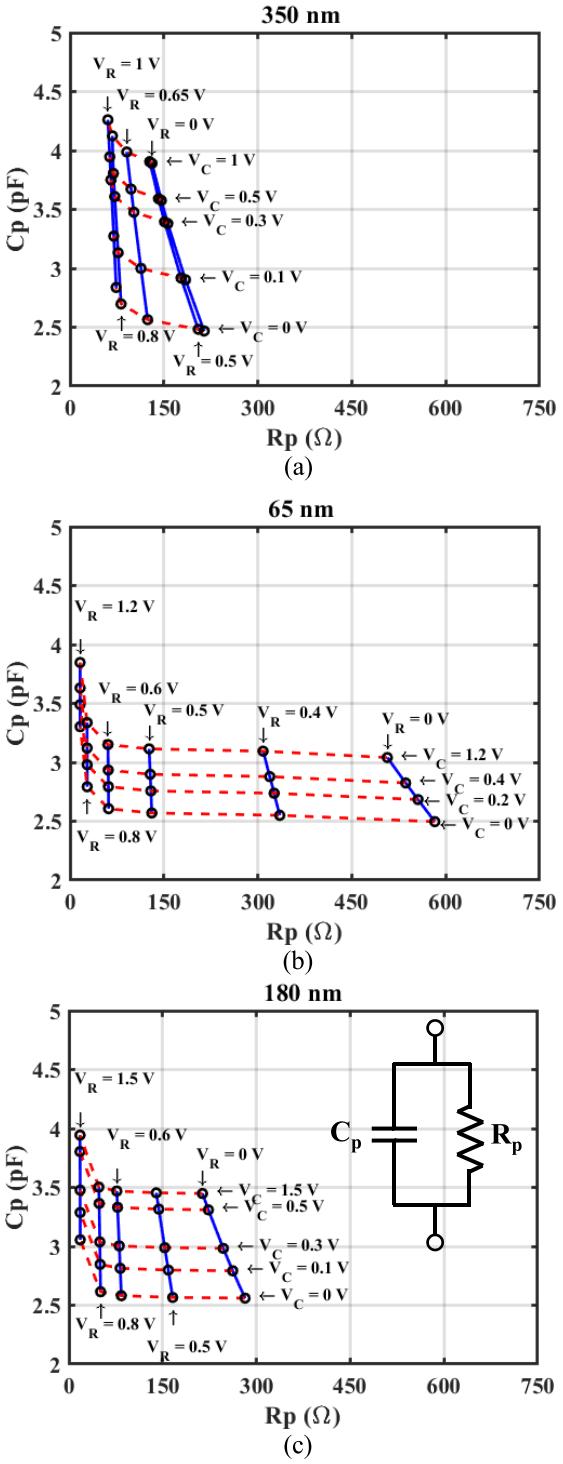

FIGURE 7. Equivalent parallel resistance and capacitance range for (a) 350 nm, (b) 65 nm and (c) 180 nm technologies.

factor of M_2 due to the larger gate length [37]. The gate width also increases the capacitance range proportionally [37]. It is obvious that there is a compromise to be made when choosing the technology. The 180 nm technology offers a compromise between the achievable capacitance and resistance ranges, and was therefore chosen as a viable technology.

With the achieved RC range show in Fig. 7(c), the metasurface can absorb transverse electric and transverse magnetic polarizations at the planes of incidence shown in Fig. 1 up to oblique angles of 45° for the TE polarization and up to 25° for the TM polarization.

As described in Section II A there are four metasurface LEs in each ASIC, connected as shown in Fig. 3(c) or Fig. 8(a). The ASIC uses 19 pins for the controller and the remaining 5 for the LEs. An alternative solution considered, had two metasurface loading elements as shown in Fig. 8(b), however we chose that shown in (a) in order to increase the equivalent parallel resistance of the circuit. The parallel resistance of Fig. 8(a) is essentially double that of Fig. 8(b). Additionally, two of the pins of Fig. 8(b) would have to be converted to a DC ground, using two additional inductors (RF chokes). Note that on-chip inductors occupy an area comparable to the WLCSP pads, which will make the LEs occupy a larger area on-chip. This increased LE area will increase the ASIC's size as well as its cost. Furthermore, the layout implementation of Fig. 8(b) will suffer from additional parasitics, arising from metal lines running across the entire IC. In order to maintain the rotational symmetry required, to allow the chip to be rotated for communication purposes (see Fig. 9), the center pin was selected as the RF ground. A further alternative considered is shown in Fig. 8(c). Although this option needs one fewer pin, it was also abandoned because it would be impossible to independently control the varactors/varistors

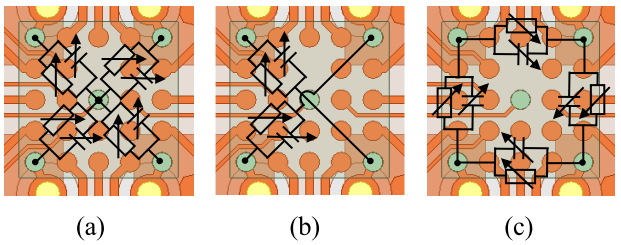

FIGURE 8. (a) Selected metasurface loading element pin location and configuration. (b) and (c) are alternative pin location options.

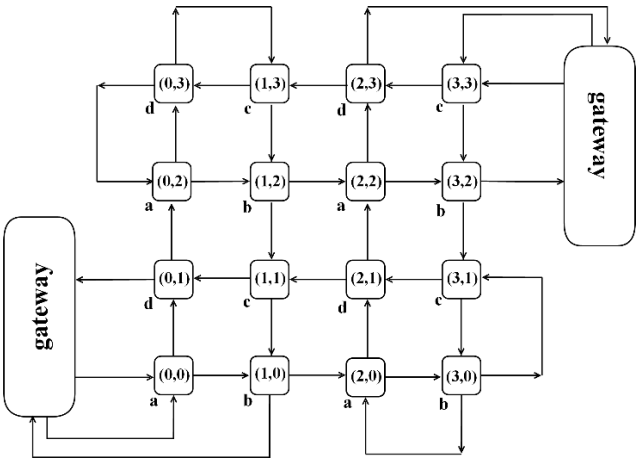

FIGURE 9. A 4 × 4 grid with two gateways and wraparounds forming a network. Letters *a, b, c* and *d* correspond to the orientation of each node.

without additional space-hungry on-chip inductors and DC block capacitors.

B. INTEGRATED METASURFACE LOADING ELEMENT CONTROL CIRCUIT AND DIGITAL-TO-ANALOG CONVERTERS

The integrated metasurface loading element control circuit is presented in this section along with the digital-to-analog converters. The control circuit operation involves the routing of data packages in a grid network where the payload of the package is the eight, single-byte inputs for the eight digital-to-analog converters, which in turn connect to the four analog V_R and four V_C voltages of the four loading elements.

Therefore, the control circuit has two main operations. First to provide the digital input to the digital-to-analog converter and in turn to tune the complex impedance of the unit cell. Second is to send or receive data packets to / from neighboring nodes in order to deliver the payload to the appropriate node of the network.

The ASIC control circuitry takes into account constraints arising both in the application and the manufacturability of the ASIC. Also, asynchronous communication is necessary because using a crystal oscillator and clock signal for synchronization (synchronous communication), can contribute to high power consumption, high EM noise generation and prevent the scalability of the metasurface. Given the large number of dies required to populate the metasurface, a relatively low-cost technology is needed and the die size needs to be as small as possible, to maximize the number of IC's per wafer. Also, the size must be large enough to be handled by automated pick-and-place machinery. A 2 mm $\times$ 2 mm size was selected, and so the maximum available WLCSP solder bumps that can be accommodated in this area is 25. To accommodate these restrictions, the control circuit has two serial input channels and two serial output channels, as shown in Fig. 5. Also, the current implementation is fully asynchronous, and the communication is carried out by handshaking between the transmitter node and the receiver node.

Each control circuit is part of a grid that intelligently moves packets to the destination node and configures the complex impedance values that are used as inputs to the varistors and varactors. In Fig. 9 a 4 $\times$ 4 grid network of metasurface loading ICs is shown. The nodes have four orientations (*a, b, c* and *d*). This way, the network can be formed by designing only one control circuit. The corner nodes are connected using wraparounds to ensure that there is more than just one path to reach every node in the grid. Therefore, even when a node is faulty, the network will not collapse. The gateways are the means to convey packets to the grid and they have full computing capabilities and resources. They are responsible for feeding the packets into the network, receiving the packets, applying fault detection mechanisms or even acting as an intermediate node in the network. The network can adopt intelligent routing algorithms, so that the configuration of all unit cells is done fast and reliably. In [31], the authors present two routing algorithms with fault tolerance mechanisms that can be adopted by the control circuits used in this design.

The data packet, once received by the destination node, is temporarily stored in the node's buffer until verification confirms that the entire packet has been received with no errors. Then, the configuration bits are copied to the memory.

The stored bits directly drive the 8-bit digital-to-analog converter, producing the analog voltages needed to configure the LEs. A two-stage resistor string digital-to-analog converter architecture was adopted for the eight digital-to-analog converters. The digital-to-analog converter's output needs to be monotonic, accurate and it needs to occupy a small area in the IC. The current required by the metasurface loading element is negligible, therefore the digital to analog converter has no need of an output buffer. This requirement and its simplistic design made the two-stage resistor string digital-to-analog converter an attractive solution.

The analog voltages produced by the digital-to-analogue converters are inputs to the metasurface loading elements (V_R and V_C biases). This changes the metasurface loading element impedance, which in turn alters the metasurface surface impedance.

IV. MANUFACTURABILITY OF METASURFACE PCB

This section describes the production processes toward manufacturing the actual metasurface in a large industrial printed circuit board (PCB) format. The metasurface periodic sub-wavelength structure and its anisotropic PCB stack up are demanding, and push the capabilities of the manufacturing process. Asymmetric PCB layer stacks are commonly avoided since the different thermal expansion coefficients of the PCB materials and or the metallization will produce a warped PCB. The asymmetric PCB layer stack pushed for homogenous material layers shown in Fig 10. The PCB stack consists of Megtron 7N materials (Fig. 10), R-5785(N) laminate and prepreg R-5680(N) with thicknesses of T_1:100μm and T_2:750μm. The laminate R-5785(N) and the prepreg R5680(N) have the same electrical properties, dialectic constant of 3.35 (ε_r) and a dissipation factor of 0.002 (tan(δ)). This makes the layering across the thickness H_1 and H_2 act as an electrically homogenous material.

The four-layer PCB presented, consists of four metal layers as shown in Fig. 1. In terms of electrical connectivity, L_3 and L_4 serve for routing, while also a plane is positioned on L_3 that is connected to V_{dd} and on L_4 a metal fill is placed that is connected to the ground (L_2). L_4 includes the chips' footprints with the routing of the tracks for the asynchronous communications and global signals. The remaining area of L_4 is covered with copper fillers that are connected to the ground. In addition, the three global tracks are distributed to the whole tile. The dimensions of the PCB are 302.4 $\times$ 302.4 mm, which translate to approximately 5 $\times$ 5 λ^2, at the design frequency (5 GHz). A top and bottom view of the PCB can be seen in Fig. 11 (a) and (b), respectively.

In Fig. 11 (c) the routing of the chips' pads is shown. An array of 5 $\times$ 5 pads is used as the footprint of the WLCSP

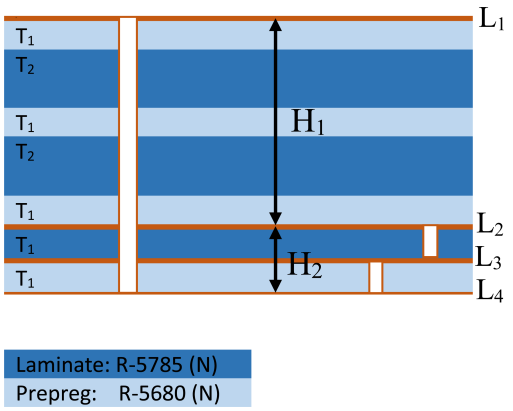

FIGURE 10. The 4-layer PCB stack adopted for the example metasurface design.

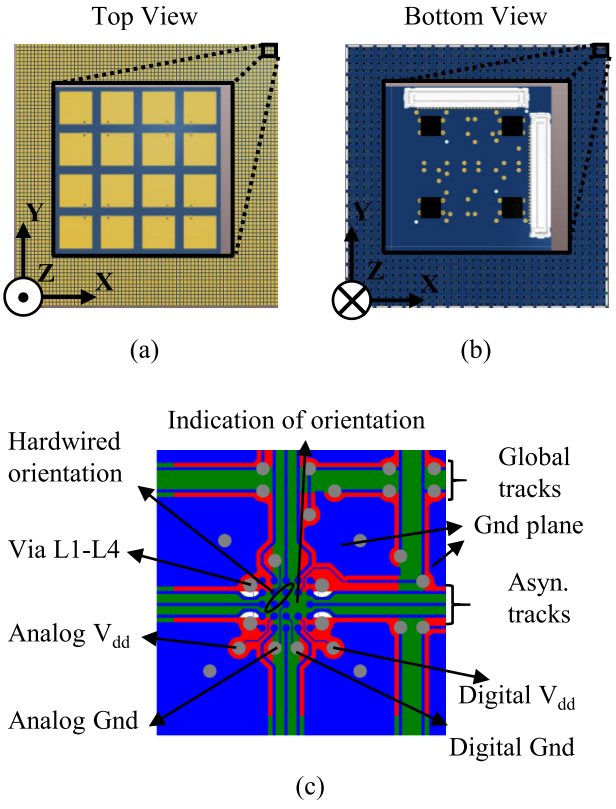

FIGURE 11. Metasurface PCB, (a) top view, (b) bottom view, and (c) routing of chip's pads.

dies. The diameter of the pads is 0.25 mm with a pitch of 0.4 mm (center to center). One of the pads is not used to indicate the correct orientation of the chip. The track width within the chip's footprint is 0.045 mm to enable proper distribution of the tracks. The four corner pads are connected to L_1 through L_1-L_4 vias. Three pads on each side are used for the asynchronous communication with the neighboring chips. Another two pads are dedicated to the global signals. Additional two pads are used for digital V_{dd} and Gnd and two pads for the analog V_{dd} and Gnd. The orientation of each chip is hardwired by two pads to V_{dd} or Gnd. When populating the board, the chips actual orientation can be distinguished by the asymmetry of the pads, where one ball of the 25 is intentionally omitted. Asynchronous tracks are symmetrically routed to match the delays between lines.

Four unit cells are arranged in a scalable design with the appropriate orientation of the chips $\begin{pmatrix} D & C \\ A & B \end{pmatrix}$. Starting from the A position, the chips are rotated 90 degrees clockwise from A to D position. At the edges of the PCB, multiple Low Insertion Force (LIF) connectors are placed to enable the connection to neighboring PCBs. Thus, scalability can be achieved. These connectors can also be used for the connection of the gateway. In addition, pads dedicated to power tracks are distributed all over the edges of the PCB for better distribution of the power.

Even though the metallization layers are not symmetric in the PCB stack, the PCB showed very little warpage, and the warpage was less than 100μm. A post fabrication cross-section of the PCB is shown in Fig. 12. The PCB stack thickness deviated from the nominal PCB thickness. This is mainly attributed to a deviation in the prepreg and lamination thicknesses in the stack compared to the nominal thicknesses, and to slightly larger copper thicknesses after electroplating on the copper layers. The measured H_1 and H_2 thicknesses used in the electromagnetic simulations can be seen in Fig. 12 (a).

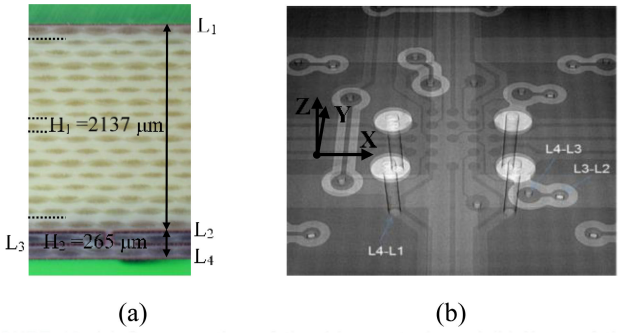

FIGURE 12. (a) Cross-section of the 4-layer stack, and (b) X-ray of the manufactured PCB.

In Fig. 12 (b) an X-ray picture of the Hypersurface PCB was taken to validate that the L_1-L_4, L_2-L_3 and L_3-L_4 vias were successfully electroplated.

V. METASURFACE PERFORMANCE

The functional metasurface performance can be seen in Fig. 13, where the optimal RC values for absorption are overlaid with the 180-nm semiconductor process range to demonstrate the capabilities of this example unit cell. The optimum RC combination for minimizing reflection (maximum absorption) is plotted with blue circular (TE) and red triangular markers. As can be seen, the unit cell can absorb perfectly at the target frequency of 5 GHz both normal and oblique incident waves of TE and TM polarization for angles up to 45 and 25 degrees, respectively [Fig. 13(a)]. The TE angle range is larger, given that this was the target polarization in the design process.

The performance is further examined in Fig. 14, where the reflection coefficient is plotted for various angles of incidence

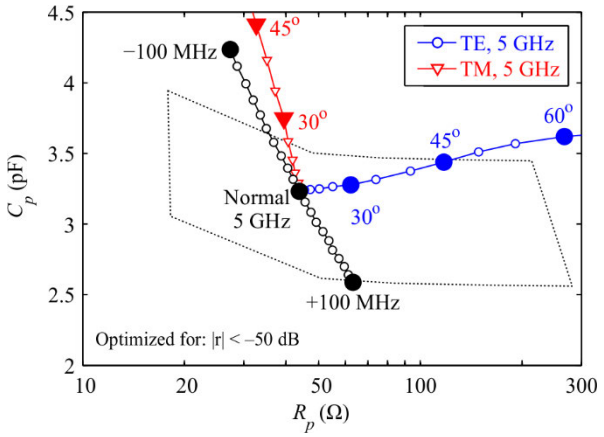

FIGURE 13. Required loading-element *RC* values for perfect absorption of y-polarized oblique incidence for both TE and TM polarizations at 5 GHz.

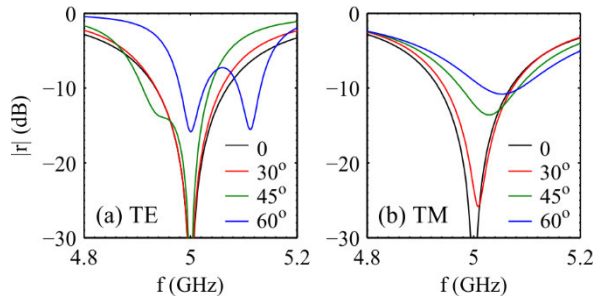

FIGURE 14. Reflection spectra for optimal *RC* values within the range provided by the ASIC, for oblique incidence at the (a) TE and (b) TM polarizations.

as a function of frequency, considering the optimum RC load for each case. At normal incidence the reflection coefficient is less than −50dB. This degrades as the angle of incidence increases, as shown in Fig. 14(a) for TE polarization. However, it remains below −30 dB for incident angles up to 45 degrees, that can be covered with the 180 nm technology, accommodating the majority of RCS reduction applications. Similar behavior is found for the TM polarization, depicted in Fig. 14(b). The reflection coefficient at 5 GHz remains below −20 dB up to 25 degrees, that can be covered with the 180 nm technology.

Finally, the optimal RC values for normal incidence are plotted in Fig. 13 for ±100MHz to illustrate the frequency effect on the RC values. The bandwidth that can be accommodated for normal incidence is approximately 150 MHz around the target frequency of 5 GHz.

For this given metasurface example design, the targeted polarization affects the technology selection. From Fig. 12, it can be seen that TM polarization does not need large resistance tunability, but requires a larger capacitance range. If emphasis were to be placed on the TM polarization, then the 350 nm technology would have been more appropriate. The 350 nm technology can easily be adapted to a TM polarization absorber, and is more affordable. Similarly, for solely TE polarization performance, the 65 nm technology is more appropriate, since TE requires a larger resistance tuning range and a lower capacitance range. As the semiconductor manufacturing costs increase exponentially with decreasing feature sizes, a tradeoff results in the choice of the 180 nm technology. This can satisfy large angles of incidence that would be suitable for the majority of RCS reduction applications.

VI. CONCLUSION

An example programmable metasurface absorber design has been presented and has been used to demonstrate the feasibility of a low-cost, low-power ASIC design for adaptive metasurfaces. The ASIC design has been explored for various technology nodes at 350 nm, 180 nm, and 65 nm, where the performance has been evaluated in view of implementing realizable tunable complex impedance loading elements. After selecting the appropriate 180 nm semiconductor process technology, it has been demonstrated that perfect absorption can be achieved (−50 dB reflection coefficient) at normal incidence as well as at oblique angles up to 45° for TE polarization.

VII. CONTRIBUTIONS

The multidisciplinary work presented in this work had contributors from eight institutions requiring much interaction. Authors affiliated with UCY predominantly contributed to the ASIC design, actual PCB layouts for production, and chip powering/communication/networking aspects. Authors affiliated with FORTH and Aalto predominantly contributed to the metasurface electromagnetic design, related PCB material specifications, the unit cell geometry and absorber performance evaluation. Authors affiliated with IZM provided fabrication guidelines for the design, and handled the PCB manufacturing.

ACKNOWLEDGMENT

The authors like to thank the partners in the VISORSURF consortium, Prof. S. Tretyakov, M. S. Mirmoosa, C. Liaskos, Prof. M. Kafesaki, and Prof A. Pitsilides for useful discussions.

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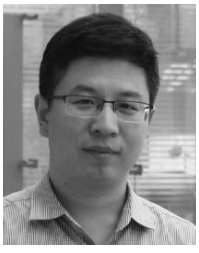

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