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Design of a 20-80 GHz Down-Conversion Mixer for 5G Wireless Communication with 22nm CMOS

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***Abstract*—This paper proposes a 20 - 80 GHz RF double-balanced mixer utilizing a hybrid down-conversion scheme. To achieve the down-conversion over the entire range, two mixers are operating in double-down-conversion for fixed IF of 3 GHz and RF is divided into low-band 20 - 44GHz and high-band 44 - 80GHz. For the low-band, the first mixer is bypassed and the second mixer used for down-conversion. For the high-band, both mixers are used for down-conversion. This results in reducing the LO tuning range by over 50% as compared to a regular sliding IF scheme. The design is evaluated using simulations of the designed mixer in 22nm CMOS technology, achieving a conversion gain of over 5 dB throughout the RF bandwidth, a minimum IIP3 of 4.9 dBm and minimum noise figure of 5.1 dB.**

***Index Terms*—Double-balanced mixer, wideband, sliding IF, CMOS, RF, mmWave, 5G, wireless communication**

I. Introduction

Development of fifth generation (5G) wireless communications requiring high data rates, wide signal bandwidths, good signal-to-noise ratios (SNR) and efficient systems has pushed the telecommunications industry to strive beyond operating frequencies under 6 GHz, as has been the norm in older communications standards. Millimeter-wave (mmW) frequencies, ranging from around 10 GHz up to several hundreds of GHz, contain spectral resources that are still infrequently used, and could provide a platform for the expected growth in wireless communications in the future.

In a conventional superheterodyne receiver, down-conversion of an RF signal to an intermediate frequency is done in a single mixer stage. In this case, the IF frequency is constant and assumed to be low enough for the IF circuitry to be implemented on-chip. However, down-converting RF signals of tens of GHz brings challenges in designing frequency synthesizer circuitry for generating an equally high frequency LO signal.

A way to avoid very high frequency LO signals is to employ a two-stage down-conversion architecture in which two separate frequency conversions take place: first from RF to IF1, and then from IF1 to IF2. The major drawback of this method lies in the fact that two separate oscillators are required to generate the LO signals, thus consuming valuable chip area. The sliding IF receiver provides a straightforward solution to eliminate the need for a second oscillator. Instead, only one oscillator is used by deriving the second LO frequency from the first by using a frequency divider or multiplier [1].

Sliding IF receivers have been presented in previous research, such as in [2] and [3]. In [2], a sliding IF scheme was implemented in which the first conversion uses an LO frequency of $f_{LO1} = 4f_{RF}/5$ to an intermediate frequency of $f_{IF} = f_{RF}/5$. The second conversion is done with an LO frequency of $f_{LO2} = f_{RF}/5$ to baseband. However, the RF frequency range was a fairly narrow band between 25 – 30 GHz. In [3], a receiver architecture was presented with a wider RF bandwidth of 50 – 70 GHz, IF bandwidth of 30 – 50 GHz and baseband bandwidth of 0 – 10 GHz. In this case, however, the LO frequencies were fixed at 20 GHz and 40 GHz for the first and second mixers respectively.

The aim of this work was to provide insight into the design of a mixer with emphasis on achieving wideband functionality and implementation of a suitable down-conversion frequency scheme. The proposed mixer structure features two Gilbert cell mixers to support down-conversion in two stages with an output intermediate frequency of 3 GHz. Transformers are used to achieve wideband operation with an RF bandwidth of 20 – 80 GHz. The down-conversion scheme implements a hybrid solution combining a dual-down-conversion sliding IF receiver and single conversion superheterodyne receiver. This method allows for the reduction of the tuning range in the VCO and PLL circuits, which reduces the complexity and performance requirements of wideband transcievers. A block diagram of the mixer demonstrating its functionality is shown in Figure 1.

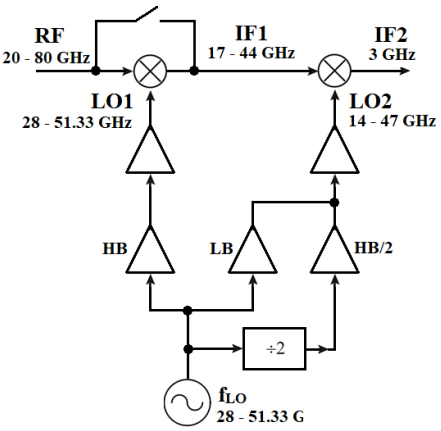

Fig. 1: Proposed sliding IF mixer block diagram.

II. Circuit Design and Analysis

A. Down-conversion scheme

This work features a very wide RF bandwidth of 20 – 80 GHz, which presents a challenge in terms of the LO frequency range and down-conversion scheme design. Using a superheterodyne receiver strategy with only one mixer to convert the RF signal to the 3 GHz IF would cause problems with the generation and propagation of high frequency LO signals, which would need to span 23 – 83 GHz. A two-stage superheterodyne down-conversion for the entire RF frequency range reduces the required LO frequency range to approximately 11 – 51 GHz. This is still a very wide frequency band and would bring major challenges in oscillator design. The challenges associated with designing wideband VCOs have been presented e.g. in [4] and [5].

In order to further reduce the required LO tuning range, this work implemented a division of the RF input frequency range into low and high bands (abbreviated LB and HB). The LB spanned 20 – 44 GHz and the HB 45 – 80 GHz. Consequently, the required LO frequency range was reduced to 23 - 51.33 GHz which is less than 50% of the range required by a superheterodyne single-stage down-conversion. Table 1 displays the RF, IF and LO frequencies for both bands. Figure 2 shows the circuit diagram of the proposed mixer in addition to frequency ranges at key nodes of the circuit.

In the LB, the mixer operates in superheterodyne mode, down-converting the 20 - 44 GHz RF signal directly to the 3 GHz IF2 with an LO of 23 - 47 GHz. This provided the advantage of simplifying the mixing operation as only the second mixer stage was used for down-conversion. The first mixer was operating as a cascode, differential amplifier, in such a way that there was no LO signal fed to the mixing stage transistors and biasing was only applied to the positive branch.

In the HB, the mixer operates in sliding IF mode. The first stage is used for the initial down-conversion from a 45 – 80 GHz RF input using a 28 – 51.33 GHz LO1 signal into the IF1 of 17 – 28.67 GHz. The second down-conversion is done using LO2 which, in accordance to the sliding IF methodology, is a divide-by-two version of LO1 signal. Now, as both mixer stages are operating as mixers, the overall conversion gain is reduced compared to the LB. As a result, a simple differential pair amplifier, with an LC tank tuned to 3 GHz as a load, was added to the output of the second mixer to provide additional gain for the HB.

The LO distribution and buffering scheme for HB and LB is shown in figure 1. According to the sliding IF principle, one oscillator is used to generate the first LO signal and a frequency divider is used to derive the second LO from the first.

In the HB, buffering is done for the original and divided-by-two LO signals in two amplifier stages. In Figure 1, the signal paths marked HB and HB/2 to distribute the 28 - 51.33 GHz LO1 and 14 - 25.67 GHz LO2 to the mixers. In this case the first amplifier in the LB signal path is switched off and the LO distribution is exactly as in a sliding IF mixer.

For the LB, the LO signal follows the LB path shown in Figure 1, in which a 23 - 47 GHz LO is fed to the second mixer. In this case, the entire HB path to the first mixer is switched off, as are the divider and first amplifier of the HB/2 signal path. This distribution scheme allows for the use of the first mixer stage as an amplifier while the second mixer performs the down-conversion.

TABLE I: Mixer frequency plan.

	f_{RF}	f_{LO1}	f_{IF1}	f_{LO2}	f_{IF2}
LB	20 - 44	-	-	23 - 47	3
HB	45 - 80	28 - 51.33	17 - 28.67	14 - 25.67	3

B. Mixer core

The choice of the Gilbert cell as the suitable mixer topology is based on its high rejection of LO noise and high port-to-port isolation, while also achieving a moderate conversion gain and noise figure. As it is a differential mixer topology for both input and output, is directly suited for fully differential receiver architectures [6-9].

Dimensioning of transistors of the mixer was effectively a compromise between gain and power consumption. In this work, the conversion gain of the mixer was prioritized as it

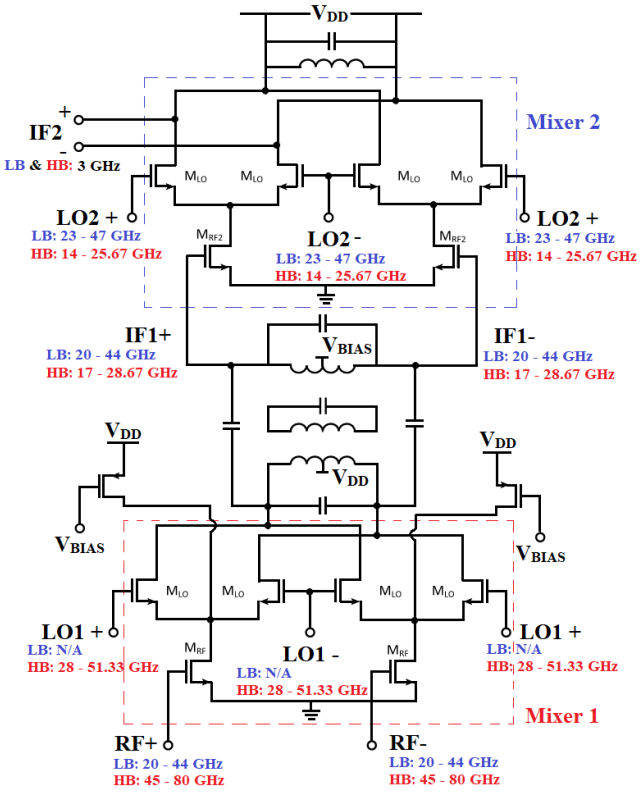

Fig. 2: Proposed mixer circuit diagram.

was designed for mmW-frequencies. Therefore, the transistors were dimensioned for the optimal width to achieve sufficient gain. Gate resistance was minimized by dividing the gate into a large number of fingers with the minimum possible length.

To further improve the conversion gain, current bleeding was added to the basic double-balanced topology. The aim of this technique was to provide more bias current for the transconductance stage with the intention of improving the conversion gain and linearity. In practice, current-bleeding was achieved by adding PMOS-transistors to the mixer, which inject an additional drain current to the transconductance stage transistors, thereby increasing their transconductance [7,9,10].

A key challenge in terms of transistor dimensioning is a result of the low (<1V) supply voltages of modern CMOS technologies. This makes it difficult to achieve correct biasing of transistors in a conventional Gilbert cell. In this work, the issue was circumvented by removing the tail current source, resulting in a pseudo-differential topology. This, when combined with a purely reactive load, provided increased flexibility for biasing.

C. Wideband load

A conventional Gilbert cell loads the mixing stage with resistors. This is a practical solution for mixers operating at sufficiently low frequencies. However, the limitation imposed by low supply voltage and desire to design wideband circuits for mmW-frequencies make resistive loading impractical in these circumstances [8].

In this work, the bandwidth requirement at the first IF between mixer stages spans 17 - 44 GHz. Thus, it was necessary to implement a transformer-based network to load the first mixer. Transformer-based loads have been presented in literature for wideband amplifiers and the same fundamental principle is applied in this work. The coupling factor, k, of the transformer coils can be used to adjust the bandwidth so that a greater coupling factor results in a wider passband response [11-13].

Based on the bandwidth requirements, a wideband transimpedance network was designed based on a transformer featuring three coils. This is presented in Figure 4. The network provides a method of realizing three separate resonance

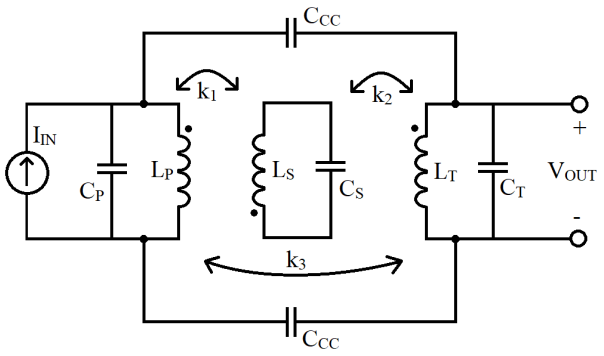

Fig. 3: Transformer-based wideband load network.

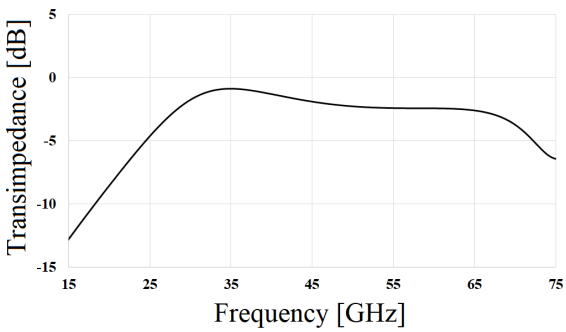

Fig. 4: Load network transimpedance vs frequency.

peaks, when combining parallel capacitors for each coil. For a three-coil transformer, there are three separate coupling factors between each of the primary, secondary and tertiary coils as demonstrated in Figure 3. This allows a wider passband to be achieved than by using a conventional two-coil transformer.

The network also employs a technique presented in [3], namely gain equalization using cross-coupling capacitors, C_{CC}. The function of these capacitors is to balance the passband response, which typically has uneven resonance peaks with the low-frequency peak having the largest amplitude. Gain equalization comes at the cost of a slight reduction in peak gain of the lowest resonance peak but simultaneously raising the gain of the highest frequency resonance peak. The transimpedance of the designed load network as a funtion of frequency is presented in Figure 4.

III. Simulation Results

In this work, all circuit design has been done using circuit models of 22nm FDSOI technology by Global Foundries. For simulations, the layouts of both stages of the mixer were run through parasitics extraction. In addition, all passive components were simulated and extracted with the ADS Momentum EM simulator.

The conversion gain of the mixer was simulated for both low and high bands and is shown in figure 5. Peak gain is achieved at an RF frequency of 30 GHz, while the gain stays above 5 dB throughout a 20 - 80 GHz range.

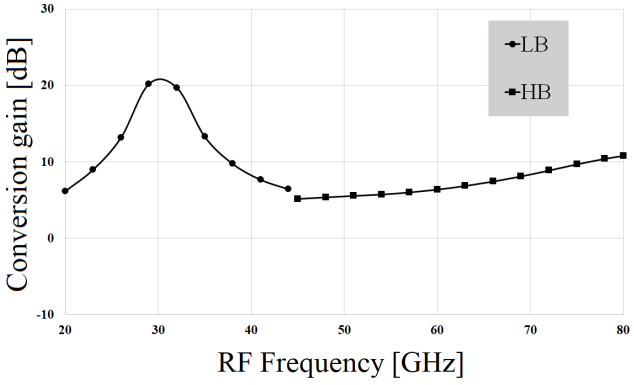

Fig. 5: Simulated conversion gain vs RF frequency.

Figure 6 displays the noise figure of the mixer as a function of the RF frequency with the peak value at around 30 GHz being 5.1 dB.

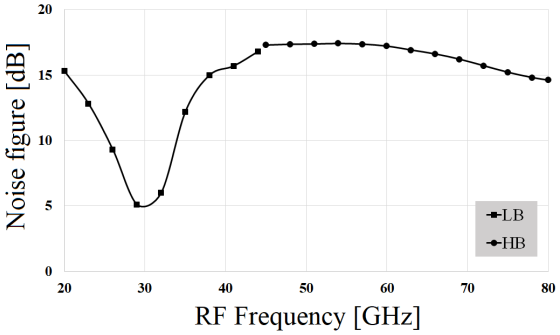

Fig. 6: Mixer noise figure vs RF frequency.

The linearity of the mixer is demonstrated in figure 7 which shows the 3rd order intercept point as a function of the RF frequency. The peak value was 4.9 dBm at 45 GHz.

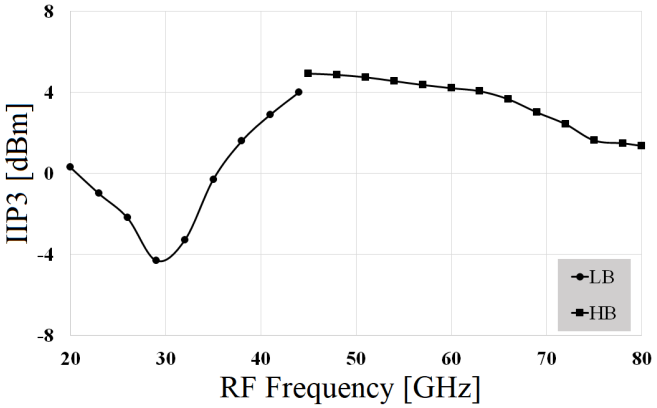

Fig. 7: IIP3 of the mixer.

Figures 8 and 9 demonstrate port-to-port isolations of the first and second mixer stages respectively. In both cases the isolations between the LO and RF ports as well as the LO and IF ports are shown.

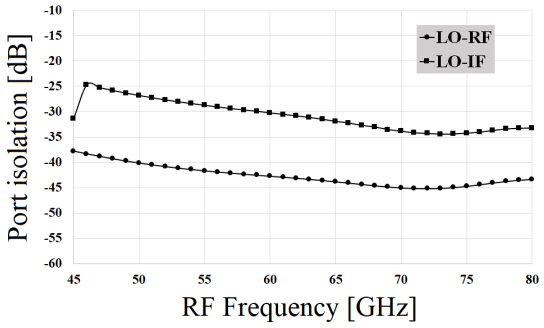

Fig. 8: Port-to-port isolations of mixer stage 1.

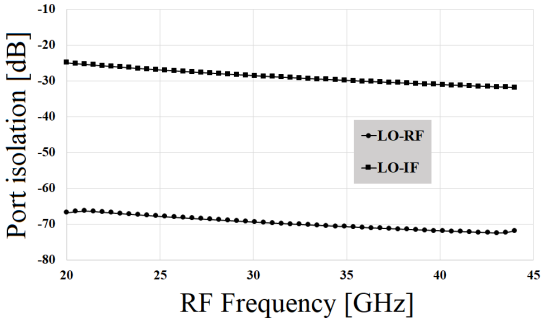

Fig. 9: Port-to-port isolations of mixer stage 2.

IV. Conclusion

In this work, a wideband, double-balanced mixer was presented. The mixer utilized a hybrid down-conversion scheme combining a superheterodyne single down-conversion with a sliding IF dual conversion. The challenges associated with wide LO frequency ranges and their generation were highlighted. The design methodologies of the mixer core were related to transistor dimensioning, limited voltage headroom and current bleeding. Wideband operation was achieved with a transformer-based load network. Operation of the mixer was verified with simulations which demonstrate a wideband conversion gain with reasonable linearity, noise performance and isolation.

TABLE II: Comparison with prior work.

Ref.	This work	[2]	[3]	[9]	[14]
Technology	22nm FDSOI	65nm CMOS	40nm CMOS	65nm CMOS	45nm CMOS
Mixing scheme	Sliding IF & superheterodyne	Sliding IF	Sliding IF	Superheterodyne	Direct conversion
RF bandwidth [GHz]	20 - 80	25 - 30	51 - 71	27.6 - 57.8	45 - 66
LO tuning range [GHz]	28 - 51.33	20 - 24	20 & 40 (fixed LO)	N/A	45 - 66
Conversion gain [dB]	>5	34 (full receiver)	20 (full receiver)	7.3	13.8

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