Haapala, Tuomas; Rantataro, Tuomas; Halonen, Kari

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A Fully Integrated Programmable 6.0–8.5-GHz UWB IR Transmitter Front-End for Energy-Harvesting Devices

Tuomas Haapala, *Student Member, IEEE*, Tuomas Rantataro, and Kari A. I. Halonen, *Member, IEEE*

***Abstract*— Ultra-wideband impulse radio transceivers are becoming a key building block for establishing ultralow power wireless sensor networks. However, impulse radio transmitters commonly suffer from a low spectral quality and a coarse frequency tuning resolution, which limits their global applicability. In this article, we present a fully integrated ultralow power impulse radio transmitter front-end (TFE) whose pulse shaping capabilities and integrated output matching network make it globally applicable up to a 4-MHz pulse repetition rate. We demonstrate a digital carrier frequency-tuning method that achieves a 28-MHz resolution over the frequency band of 6.0–8.5 GHz. In addition, we show that the temperature dependence of the TFE's carrier frequency can be compensated digitally over the industrial temperature range from −40°C to 85 °C. The proposed TFE supports energy-harvesting applications particularly well due to its low leakage power level of 380 nW and a high tolerance to power supply transients during pulse generation. It is demonstrated to operate robustly with low-drive regulators powered by low-quality sources. The TFE is fabricated in a 65-nm CMOS process. It generates 1.8-pJ pulses at a 7.5-GHz carrier frequency while consuming 63 pJ per pulse, corresponding to 2.3% efficiency.**

***Index Terms*— Energy harvesting, impulse radio, transmitter front-end, ultralow power, ultra-wideband (UWB).**

I. Introduction

THE number of smart devices connected to the internet is predicted to grow exponentially in the near future [1] to support a variety of new services in, for instance, health care, smart homes, and industry automation. Many services require the applied smart devices to operate wirelessly. Today, a mobile energy supply is commonly provided by means of batteries despite their environmental hazard. While ambient energy harvesters provide an alternative to batteries, they can suffer from a large equivalent series resistance and entail a demanding power budget.

Ultra-wideband impulse radios (UWB IRs) have been proposed as a potential candidate for allowing energy-harvesting sensor nodes to deliver data wirelessly [2], [3]. The average power consumption level P_{avg} of an UWB IR transmitter at a certain pulse repetition rate (PRR) can be acquired from

$$P_{\text{avg}} = P_s + E_{\text{pp}} \cdot \text{PRR} = P_s + \frac{E_p}{\eta} \cdot \text{PRR} \quad (1)$$

where P_s is the transmitter's static power consumption level, E_{pp} is the amount of energy consumed per generated pulse, E_p is the pulse energy, and η is the energy efficiency. Both P_s and η have to be optimized to make an UWB IR transceiver energy efficient over a wide range of PRRs.

The vast majority of recently published low-power UWB IRs target the U.S. UWB mask between 3.1 and 4.8 GHz, regulated by the Federal Communications Commission (FCC). This allows power savings due to a low carrier frequency and relaxed spectral requirements compared to Asia and Europe [4]. However, UWB IRs designed for the FCC mask rarely comply with the regulations of other regions due to the relaxed requirements, which limits the global applicability of these designs. In addition, most regions only allow usage of the 3.1–4.8 GHz frequency range presuming the appliance of mitigation techniques [5]. The frequency range is also surrounded by strong narrow-band industrial, scientific and medical (ISM) band and wireless local area network (WLAN) interferers, which makes receiver design challenging.

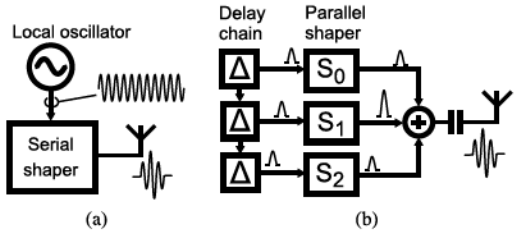

Fig. 1. UWB IR transmitter architectures. (a) LO-based. (b) Edge-combiner.

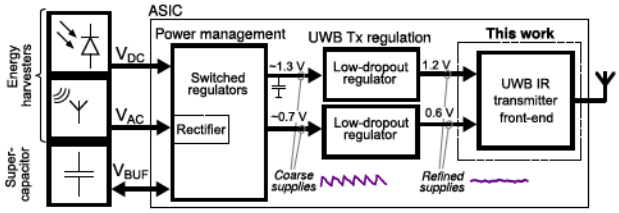

Fig. 2. Energy-autonomous device with hierarchical power management.

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The authors are with the Department of Electronics and Nanoengineering, Aalto University, 02150 Espoo, Finland (e-mail: tuomas.haapala@aalto.fi).

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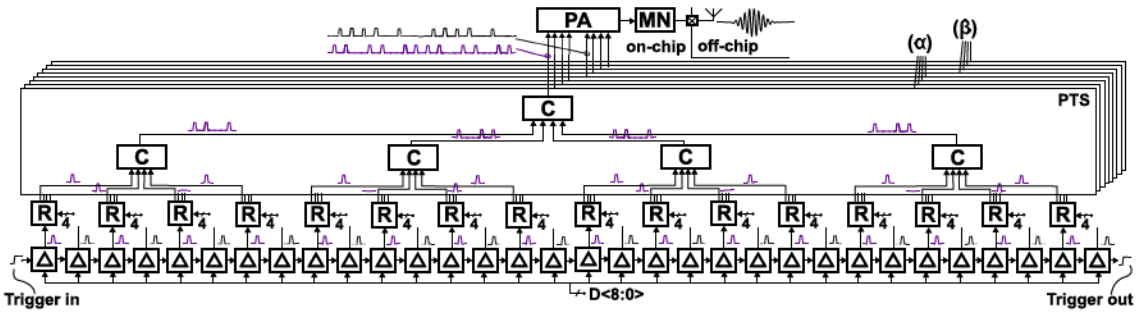

Fig. 3. Proposed edge-combining TFE comprised delay units (Δ), routers (R), combiners (C), a power amplifier (PA), and a matching network (MN). Modified from [13].

UWB IR transmitters based on a local oscillator (LO), as depicted in Fig. 1(a), benefit from straightforward frequency tuning. The serial LO signal can be shaped to a suitable pulse waveform by means of, for instance, a digital-to-analog converter [3], a digital mask generator [6], or an analog pulse shaper [7]. However, achieving a well-controlled programmable pulse shape remains a challenge for LO-based UWB IR transmitters. LO-based transmitters can also suffer from a slow startup, which prevents the circuit from being duty-cycled efficiently at low data rates.

UWB IR transmitters based on a delay chain, as depicted in Fig. 1(b), benefit from the parallelism of the generated oscillation signal. The pulse can be shaped digitally by simple logic ports that can be programed in advance by low-speed logic. This kind of UWB IR transmitters have demonstrated adequate pulse shaping capabilities for potential compliance with more strict UWB masks [8]. These designs also gain from their triggerable character: their startup time can be zero. However, UWB IR designs relying on a delay chain often suffer from coarse digital frequency tuning resolution [8]–[10] or they utilize analog frequency tuning [11]. Delay chains also suffer from a high power supply sensitivity.

This article presents a fully integrated edge-combining UWB IR transmitter front-end (TFE) that complies with the European UWB mask, regulated by the European Commission (EC) [12], up to a 4-MHz PRR. The high end of the targeted frequency band of 6.0–8.5 GHz has a wide unrestricted global availability [5]. The compliance is achieved by means of 4-bit pulse-shaping and an integrated matching network (MN). In addition, we propose a method for tuning the TFE's carrier frequency based on capacitive voltage dividers. The proposed frequency tuning method shows a good linearity over a wide tuning range, a fine tuning resolution, and a high tolerance to power supply transients during pulse generation. The TFE has a good energy efficiency and a very low static power consumption level, which allows for low-power operation over a wide range of PRRs. The TFE's low power consumption level and high tolerance to supply transients improve its support for energy-harvesting applications. The TFE's pulse energy level suffices for a line-of-sight communication range of more than 10 m with a sensitive UWB IR receiver [3].

We have published a brief description of the TFE previously in [13] along with some simulation results. In this article, we provide a comprehensive description of the TFE with a focus on the proposed delay chain design and the TFE's operation with low-drive voltage regulators. We also present the measurement results of the TFE.

The TFE has been designed for an energy-autonomous, energy-harvesting device, as depicted in Fig. 2. The device utilizes hierarchical power management [14] where the first power conversion is performed by switched regulators (SRs) that benefit from high efficiency but suffer from a significant output ripple. Refined secondary supplies are generated by low-dropout regulators (LDOs) that provide an output level with an accuracy down to several millivolts and attenuate the voltage ripple at their input. The LDOs also provide a high power efficiency assuming a small dropout voltage.

This article is organized as follows. The TFE design is detailed in Section II. The measurement results of the TFE are presented in Section III. Section IV compares the TFE with the state of the art.

II. Implementation

A block-level description of the proposed edge-combining TFE is presented in Fig. 3. The carrier frequency f_c signal of an output pulse is generated by a delay chain that is composed of 32 delay units (Δ). The propagation delay of a delay unit t_Δ is translated into the equivalent carrier frequency based on

$$f_c = \frac{1}{t_\Delta}. \tag{2}$$

t_Δ is controlled with a 9-bit frequency tuning word D. Each delay unit delivers an impulse to a router (R). The router propagates an input impulse to up to four parallel outputs based on a 4-bit tuning word. Each router is independently programmable and defines the 4-bit amplitude setting of a single sub-pulse of the output waveform. The impulses propagated by the routers are serialized by parallel-to-series (PTS) converters α and β that consist of impulse combiners (C). The delay chain delivers alternate impulses to PTS converters α and the rest to β. Finally, the serialized impulse trains trigger the PA, each train having a binary-weighted effect on the output pulse envelope. The PA is followed by an integrated MN.

The serialization is performed to keep the power amplifier's leakage current and parasitic output capacitance levels low. In effect, a fully parallel implementation would require 32 sub-PAs. Each PTS converter delivers 16 parallel input impulses to a single output, decreasing the number of required

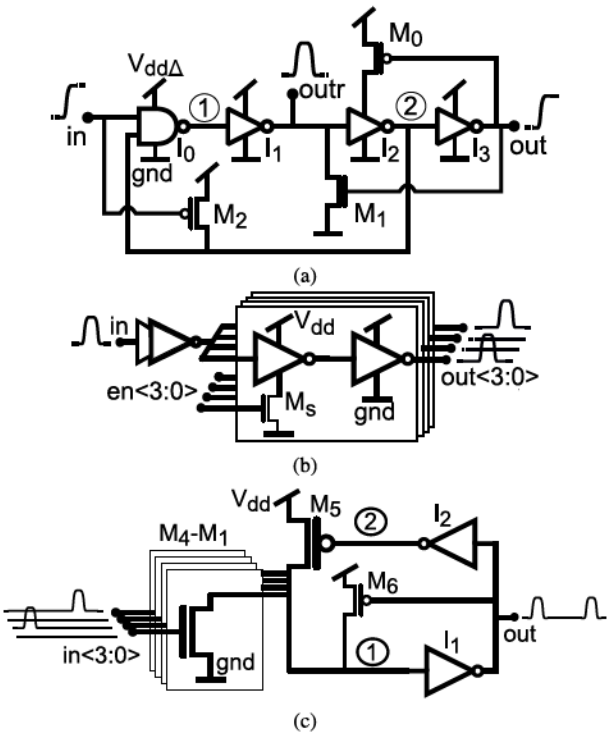

Fig. 4. Impulse propagation blocks. (a) Delay unit. (b) Router. (c) Combiner. Subfigures (b) and (c) modified from [13].

sub-PAs to 2. However, the serialization causes a penalty in the TFE's power consumption since each triggering of a combiner consumes energy. A combiner with four inputs was found to provide a good trade-off between speed and total energy consumption. The interleaving of alternate delay chain impulses to PTS converters α and β relaxes the speed requirement of the combiners. A similar serialization has previously been implemented in [9] with two-input combiners and no routing.

A. Delay Unit, Router, and Combiner

To achieve a high maximum carrier frequency, the propagation delay of the delay chain has to be minimized. In addition, to achieve a high maximum PRR, the reset process has to be fast as well. These are counteracting requirements.

The employed delay unit is shown in Fig. 4(a). The design is similar to the implementation in [10], where its operation is detailed. The propagation speed of the unit has been increased by removing the programmable driver transistors of inverter I_3 and a pull-down transistor from node 2. After the unit has been triggered, the low state of node 2 is held by parasitic capacitance instead of the pull-down transistor until the unit is reset. The delay unit has two outputs, one of which (outr) is connected to a router and the other (out) to the following delay unit. The output to a router requires an impulse-like signal while a delay unit is triggered by a rising edge and reset by a falling edge.

The employed delay unit design has several benefits. Firstly, the propagation time is defined by stages I_0–I_3 but the reset time is defined by transistor M_2 and stage I_3. Since the signal routes for propagation and reset are mainly separate, the delay unit can be designed to both propagate and reset quickly. Secondly, output node outr is pulled by large transistors with no other transistors in cascade, making the driving of the node efficient. This node suffers from a large load capacitance caused by the input of a router.

Fig. 4(b) shows the implementation of the routers. A router propagates an impulse coming from a delay unit to up to four parallel outputs. The routers are based on four pairs of cascaded inverters. The transparency of the cascaded inverters is defined by switch transistors M_s controlled by a 4-bit tuning word. The output of a disabled pair of inverters remains low despite an input impulse.

Fig. 4(c) shows the implementation of the combiners. A combiner propagates an impulse at one of its inputs to its output. Transistor M6 keeps node 1 pulled high at the initial state. An impulse at the gate of one of the input transistors M1–M4 pulls node 1 low, which results in the output node being pulled high by inverter I1. The feedback path, composed of inverter I2 and transistor M5, pulls node 1 back high. Finally, the output node is pulled low. The proposed combiner propagates quickly since it does not include any cascoded transistors.

B. Isolated Delay Unit Supplies

In ultralow power energy-harvesting applications, the TFE may be regulated by low-drive LDOs powered by a poor power source, such as a small photovoltaic array under office illumination or by an energy-storing supercapacitor with a high equivalent series resistance. Since the TFE generates a large current peak during pulse generation, the on-chip supply voltage may experience strong transients despite significant buffering.

The propagation delay of the delay units is sensitive to power supply transients. A change in the propagation delay translates into a proportional change in the pulse carrier frequency, as depicted in Fig. 5(a). The power supply rejection of the delay chain can be improved by isolating the chain from the supply during pulse generation, as shown in Fig. 5(b). However, the delay chain would require a large amount of buffering to prevent the isolated supply voltage level ($V_{\mathrm{dd}\Delta}$) from dropping gradually as the delay units are being triggered. Therefore, we propose giving each delay unit an isolated supply, as shown in Fig. 5(c). This arrangement ensures that the propagation delay remains constant over the delay chain despite isolation.

The power supply sensitivity of the three supply configurations is simulated in Fig. 5(d). Due to its peak current drain of about 5 mA from V_{dd}, the TFE causes an approximately 50-mV voltage drop over a 10-Ω resistor that models the equivalent series resistance of an energy-storing supercapacitor [15]. In the simulation, V_{dd} is decoupled with a 1.4-nF on-chip capacitor and each delay unit is equipped with an additional decoupling capacitor of 4 pF. The delay units and the rest of the TFE are simulated in post-layout (PL) mode but the switches in the figure and the additional 4-pF decoupling capacitors are in schematic level for convenience.

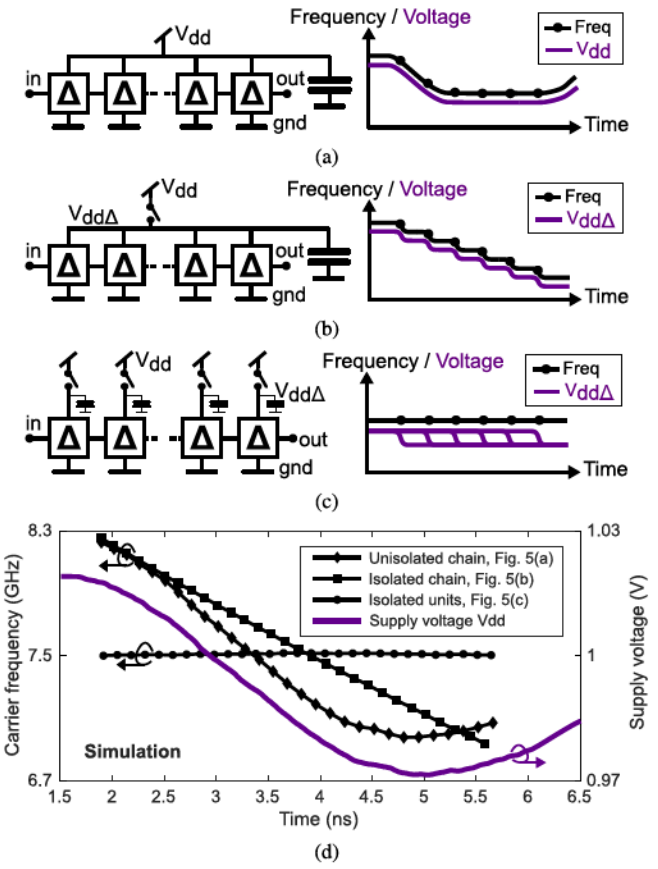

Fig. 5. Delay chain supply configurations. (a) Unisolated delay chain. (b) Isolated delay chain. (c) Isolated delay units. (d) Power supply rejection performance of the configurations.

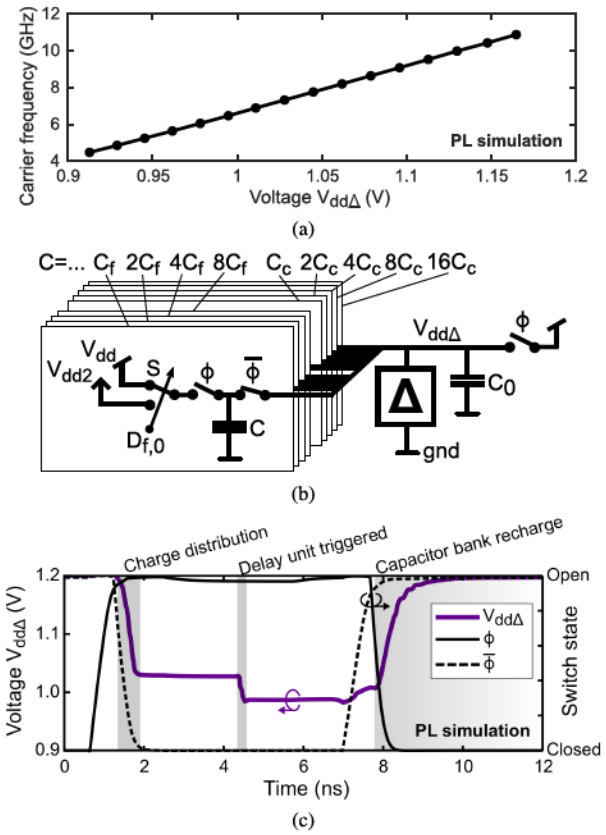

Fig. 6. Operation principle of the capacitive voltage divider of a delay unit. (a) Relation between the isolated supply voltage level $V_{dd\Delta}$ of a delay unit and the corresponding carrier frequency f_c. (b) Configuration of the divider. (c) Transient behavior of the isolated supply voltage level of a delay cell during pulse generation. Subfigures (b) and (c) modified from [13].

Additionally, the supply V_{dd} is brought to the delay chain with a −180-mV offset to set the carrier frequency to approximately 7.5 GHz. The propagation delay of a delay unit is translated into the corresponding carrier frequency according to (2). The transient of V_{dd} is practically the same for all the three supply configurations. The simulation shows that the propagation delay of the unisolated delay chain is modulated linearly by the power supply transient. The isolated delay chain rejects the supply transient but is instead modulated by a gradual drop in $V_{dd\Delta}$. The isolation of all delay units comes with a slight penalty in the maximum carrier frequency level but allows a stable propagation delay over the full delay chain and a significantly improved tolerance to supply transients.

C. Delay Chain Tuning

Recently, published edge-combining UWB IR transmitters employ various methods for delay chain tuning. Programmable driver transistors are used in [8] and [10] and a method based on capacitive delay unit loading is demonstrated in [9]. These methods result in non-linear frequency tuning steps and the achieved tuning resolution is coarse. The supply voltage level of the delay chain in [11] is controlled with an external source. We propose a delay chain tuning method based on integrated capacitive supply voltage dividers that allows tuning the TFE carrier frequency digitally. The voltage division defines the isolated supply voltage level of the delay units. As shown in the PL simulation of Fig. 6(a), there is a very linear relation between the isolated supply voltage level of the delay units and the resulting pulse carrier frequency. In addition to high linearity, some advantages of the proposed method include fine resolution and a wide tuning range.

The capacitive voltage divider is depicted in Fig. 6(b). The divider includes a binary-weighted 4-bit fine tuning capacitor bank and a 5-bit coarse tuning capacitor bank. The unit capacitor is fabricated from poly–p-well capacitors and their sizes are 2.1 fF (C_f) and 33 fF (C_c) for the fine and coarse banks, respectively. The unit capacitors are charged to V_{dd} or V_{dd2} through switches S that are controlled by frequency tuning words D_f and D_c. Capacitor C_0 provides a low-resistance buffering path for the delay unit. The operation of the divider is split in a recharge phase and an isolation phase that are controlled by switches ϕ and $\overline{\phi}$.

In the recharge phase, the bank capacitors are charged through switches ϕ. The isolation phase starts just before the delay chain is triggered. In the isolation phase, switches ϕ are opened and switches $\overline{\phi}$ closed in a non-overlapping manner, connecting all the capacitors of the divider in parallel. The consequent charge distribution between the capacitors sets the target $V_{dd\Delta}$ level according to

$$V_{dd\Delta} = \frac{Q_{\text{bank}}}{C_{\text{bank}}} \tag{3}$$

where Q_{bank} is the total charge in the isolated divider and C_{bank} is the total parallel capacitance in the isolated divider.

The total charge is given by

$$Q_{\text{bank}} = Q_0 + Q_c \sum_{i=0}^{M-1} 2^i D_{c,i} + Q_f \sum_{j=0}^{N-1} 2^j D_{f,j} \tag{4}$$

where Q_0, Q_c, and Q_f are constants ($Q_c > Q_f$), M is the number of coarse tuning bits, N is the number of fine tuning bits, and $D_{c,i}, D_{f,j} \in \{0, 1\}$ are the single tuning bits of frequency tuning words D_c and D_f. Detailed expressions for C_{bank}, Q_0, Q_c, and Q_f are derived in Appendix A.

Since C_{bank} is a constant and there is a linear relation between $V_{\text{dd}\Delta}$ and f_c, Eqs. (3) and (4) show that the proposed digital delay chain tuning method provides a linear means for controlling f_c. Since the delay units are isolated during pulse generation, the proposed method also makes the delay chain tolerant to supply transients, as discussed in Section II-B. However, the dc levels of supplies V_{dd} and V_{dd2} have to remain stable since they control the amount of charges Q_c and Q_f in (4).

A PL simulation of the behavior of the TFE's voltage divider during pulse generation is shown in Fig. 6(c). Initially, node $V_{\text{dd}\Delta}$ is charged to V_{dd}. The isolation phase starts at around 1.5 ns, initiating the charge distribution that lowers the $V_{\text{dd}\Delta}$ level to its target value. $V_{\text{dd}\Delta}$ has settled at about 2 ns. The delay unit is triggered at around 4.5 ns, resulting in a consequent drop in $V_{\text{dd}\Delta}$. The capacitor bank is recharged immediately after pulse generation. The triggering of the TFE, the non-overlapping control of switches ϕ and $\overline{\phi}$, and the immediate recharge is handled by a simple integrated trigger logic circuit.

D. Delay Chain Temperature Compensation

The propagation delay of the delay chain is strongly dependent on temperature and, consequently, it has to be calibrated to a relatively stable frequency reference. Due to its 32 delay elements, the delay chain requires a reference in the range of 125–313 MHz to cover a carrier frequency range of 4–10 GHz. This reference can be generated by a phase-locked loop (PLL) from a low-power crystal [16], microelectromechanical systems (MEMS) [17], or relaxation oscillator [18]. Calibration can then be performed by using a delay-locked loop (DLL) and a successive approximation (SAR) logic, as reported in [19]. The calibration logic should use a low-frequency clock to allow the TFE for a sufficient recharge time and, therefore, the power consumption of the calibration loop is dominated by the PLL. A low-power integer-N PLL with a power consumption of 440 μW at a 400-MHz output is reported in [20].

Due to the high power consumption of the PLL-based calibration process, we propose an alternative open-loop compensation method for the TFE's delay chain that removes the need for the calibration loop in regular use. The PLL-based calibration loop would still be required for acquiring the compensation constants of the proposed method in the field. Alternatively, the constants can be acquired in production. While the open-loop compensation method requires a temperature sensor, the sensor can be sampled at a very low rate in the order of 1 Hz to track the slow changes of ambient temperature. Due to their microwatt-level power consumption, ultralow power energy-autonomous devices have a small self-heating rate and magnitude. A nanowatt temperature sensor that supports 1-point temperature-based calibration is reported in [21] and a microwatt temperature sensor that supports voltage-based calibration is reported in [22].

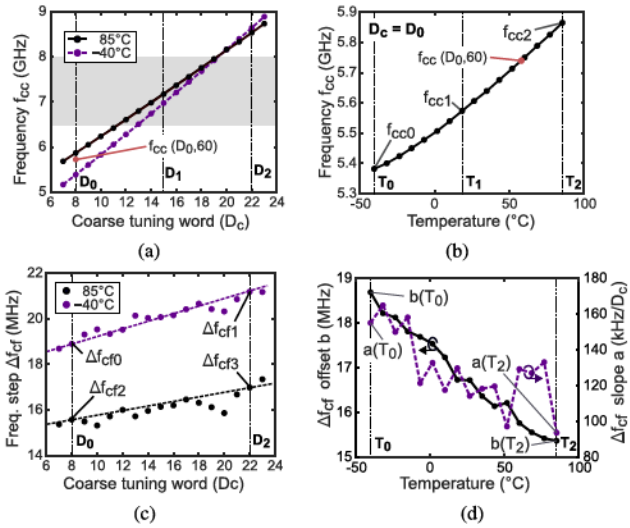

Fig. 7. Temperature behavior of the delay chain. (a) Coarse frequency tuning. (b) Temperature dependence f_{cc} at D_0. (c) Fine frequency tuning. (d) Temperature dependence of a and b.

The TFE's carrier frequency f_c is a factor of temperature T, and frequency tuning words D_c and D_f according to

$$f_c(D_c, D_f, T) = f_{cc}(D_c, T) + \Delta f_{cf}(D_c, T) \cdot D_f \tag{5}$$

where f_{cc} is the coarse carrier frequency component and Δf_{cf} is the size of a fine carrier frequency tuning step. The value of f_{cc} is shown around the target frequency band at the edges of the target temperature range in Fig. 7(a). The measured temperature dependence of f_{cc} at $D_c = D_0$ is shown in Fig. 7(b), including the effect of the LDOs and the temperature sensor used in Section III. To model this dependence, we employ a quadratic interpolator based on Newton's Divided Difference Polynomial Method [23]

$$f_{cc}(T)|_{D_c} = f_{cc0} + \frac{f_{cc1} - f_{cc0}}{T_1 - T_0}(T - T_0) + \frac{\frac{f_{cc2} - f_{cc1}}{T_2 - T_1} - \frac{f_{cc1} - f_{cc0}}{T_1 - T_0}}{T_2 - T_0}(T - T_0)(T - T_1) \tag{6}$$

where f_{cc0}, f_{cc1}, and f_{cc2} are measured at T_0, T_1, and T_2, at a given D_c, as shown in Fig. 7(b).

The size of fine frequency tuning step Δf_{cf} is a factor of both D_c and T, as shown in Fig. 7(c). These dependencies can be modeled with

$$\Delta f_{cf}(D_c, T) = a(T)(D_c - D_0) + b(T) \tag{7}$$

where the slope $a(T)$ and offset $b(T)$ depend on temperature as shown in Fig. 7(d). While the estimation of the slope is rather susceptible to noise, the compensation accuracy is not very sensitive to small errors in $a(T)$.

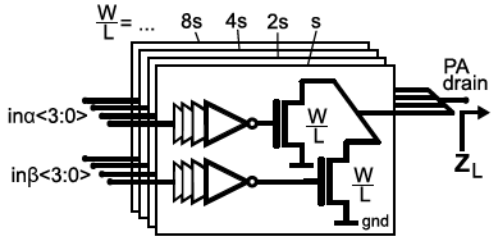

Fig. 8. Power amplifier. Modified from [13].

The complete algorithm requires 19 compensation constants: T_0–T_2, D_0–D_2, $a(T_0)$, $a(T_2)$, $b(T_0)$, $b(T_2)$, and f_{cc0}–f_{cc2} at D_0–D_2. T_0, and T_2 are selected at the edges of the target temperature range and T_1 is selected at room temperature. D_0 and D_2 are selected near the edges of the target frequency band. The quadrature interpolator is used to compute f_{cc} at D_0–D_2 at a given temperature, giving $f_{cc}(D_0, T)$–$f_{cc}(D_2, T)$, as shown in Fig. 7(a), (b) for $f_{cc}(D_0, 60)$. Based on these three points, the quadrature interpolator is then reused to acquire an estimation of D_c for a given f_{cc}. Both the slope $a(T)$ and offset $b(T)$ can be computed from the four fine step points Δf_{cf0}–Δf_{cf4} that are shown in Fig. 7(c). We then employ only the linear part of the quadrature interpolator in (6) to obtain an estimation of $a(T)$ and offset $b(T)$ at a given temperature. The estimation of D_c is floored, after which the redundant frequency offset is removed with an adequate number of fine tuning steps.

The proposed temperature compensation method was synthesized as a 24-bit floating-point arithmetic core controlled by a finite-state machine. The logic has an additional error of less than ± 1 MHz compared to the double-precision implementation used in the evaluation of the proposed method in Section III. The synthesized logic core measures 210 μm $\times$ 210 μm. It was simulated to consume 100 nW of leakage power and 370 nW of active power from a 1.2-V supply at a 32.8-kHz clock frequency. At this clock frequency, the compensation logic can be refreshed at a 250-Hz rate.

E. Power Amplifier and Matching Network

The design of the power amplifier is shown in Fig. 8. The PA has four inputs, each divided to two sub-inputs for the impulse trains coming from PTS converters α and β. The four inputs have a binary-weighted effect on the output waveform. The input impulse trains are combined at the drain of the PA.

The MN provides a dc bias for the PA drain, acts as a filter, and transforms the load impedance seen by the PA drain (Z_L) from 50 Ω to approximately 30 Ω. Based on preliminary simulations, 30 Ω gives a reasonable trade-off between the maximum pulse energy and pulse shaping linearity. The bottom schematic in Fig. 9 shows the design of the MN. The MN consists of a simple bandpass section and an elliptic low-pass section (enclosed by the dashed rectangle). Capacitor C_2 acts as a dc block. Capacitor C_1 includes the output capacitance of the PA drain and capacitor C_5 includes the parasitic capacitance of the output pad. The PA drain is biased with V_{dd2}.

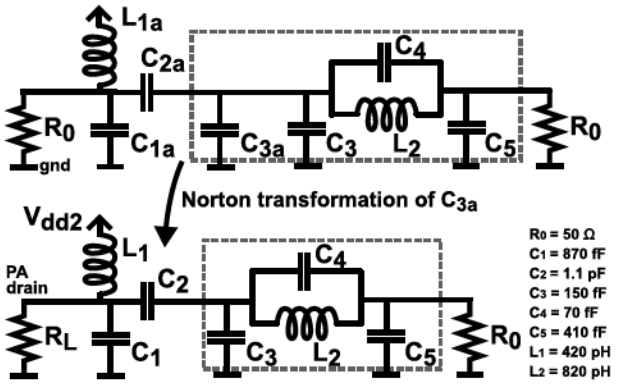

Fig. 9. Matching network and its design process. Modified from [13].

The MN was first designed for 50 Ω in Keysight ADS. The initial input capacitor of the designed elliptic low-pass section consists of a parallel combination of capacitors C_3 and C_{3a} (top schematic of Fig. 9). The load impedance seen by the PA drain was then converted by a capacitive Norton transformation of capacitor C_{3a} that down-converts the impedance on its left (bottom schematic of Fig. 9). A similar design approach has been previously adopted in [24]. In the transformation, capacitor C_{3a} is moved from the right side to the left side of capacitor C_{2a}. The consequent transformation ratio is [25]

$$n = \frac{C_{3a} + C_{2a}}{C_{2a}} \tag{8}$$

and the component values on the left side of C_{3a} after transformation are given by

$$R_L = \frac{R_0}{n^2} \tag{9}$$

$$C_2 = nC_{2a} \tag{10}$$

$$L_1 = \frac{L_{1a}}{n^2} \tag{11}$$

$$C_1 = n^2 C_{1a} + nC_{3a} \tag{12}$$

where C_1 is composed of the parallel combination of the capacitors C_{1a} and C_{3a} after transformation. The transformation carries the benefit that it decreases the size of power inductor L_{1a}, lowering the value of its equivalent series resistance.

The MN design was simulated in the electromagnetic (EM) simulator Keysight Momentum and fine-tuned accordingly. The results of the elecromagnetic simulation are presented in Fig. 10. The results are normalized to 50 Ω. The -1 dB passband of the MN ranges from 5.7 to 9.1 GHz. In that range, the real part of Z_L is matched to approximately 30 Ω while the imaginary part remains small. The minimum insertion loss in the passband is 2.2 dB. Between 6.5 and 8.0 GHz, the maximum group delay variation over any 500-MHz band is less than 10 ps.

III. Measurement Results

The TFE was fabricated in a commercial 65-nm CMOS process. A die photograph of the TFE is shown in Fig. 11.

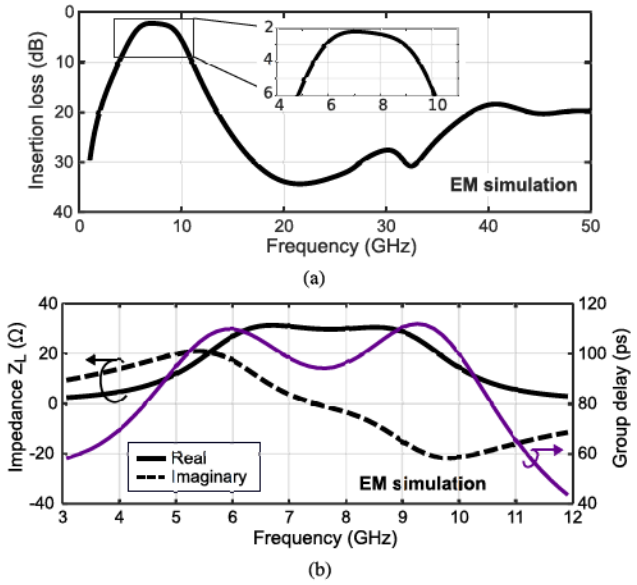

Fig. 10. Performance of the MN. (a) Insertion loss. (b) Load impedance Z_L and group delay. Modified from [13].

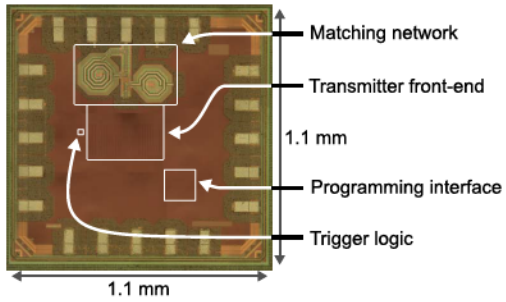

Fig. 11. Die photograph.

The TFE measures 240 μm × 340 μm including the delay chain supply capacitor banks but excluding the PA and MN. The PA and MN measure 280 μm × 470 μm and the trigger logic measures 20 μm × 20 μm. The total area occupied by the TFE and its supportive circuitry is 0.22 mm^2. The chip also has on-chip supply decoupling capacitors for V_{dd} and V_{dd2}, both of which are sized approximately 1.4 nF and 0.20 mm^2. The values of V_{dd} and V_{dd2} are 1.2 and 0.6 V, respectively.

To allow measurements in a temperature chamber, four dies were flip-chip bonded to their measurement printed circuit boards (PCBs) with their RF outputs connected to SubMiniature version A (SMA) connectors. These assemblies were also used to characterize the TFE's delay chain design and one of them was used to measure the supply transients at the end of this section. Otherwise, the TFE was characterized with the setup shown in Fig. 12, where the TFE's RF output was measured through a 40-GHz ground-signal-ground probe. Supplies and triggers were provided from external sources. The measurements described in the following paragraphs were performed in room temperature and with supplies V_{dd} and V_{dd2} decoupled with 100-nF broadband capacitors on the PCBs unless specified otherwise.

Using a spectrum analyzer to measure the TFE carrier frequency gives imprecise results due to the ultra-wide signal

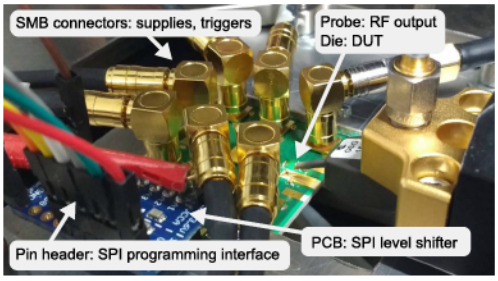

Fig. 12. Measurement setup.

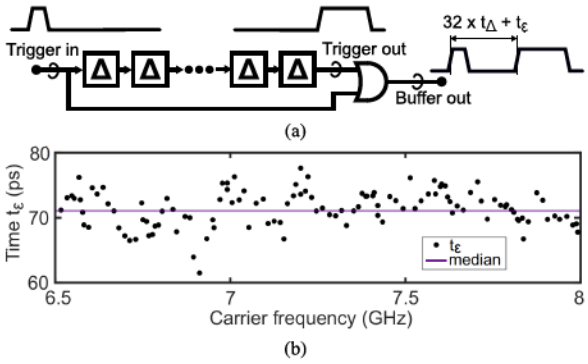

Fig. 13. Measurement of carrier frequency. (a) Measurement setup. (b) Estimation of t_ϵ.

bandwidth, low average signal strength, and the spectral shaping effect of the on-chip MN at stopband carrier frequencies. Consequently, the carrier frequency was measured with the setup depicted in Fig. 13(a). The input and output triggers of the delay chain are delivered to an on-chip OR gate buffer whose output is monitored with a 100-Gsps oscilloscope. The time delay between a rising edge at the input and output of the 32-unit delay chain as measured by the oscilloscope is given by

$$t_d = 32 \cdot t_\Delta + t_\epsilon \tag{13}$$

where t_ϵ is a delay error caused by, for instance, the propagation delay imbalance of the OR gate buffer and the different parasitic loading of the input and output nodes of the delay chain. t_ϵ can be estimated by combining (2) and (13), resulting in

$$t_\epsilon = t_d - 32 \cdot \frac{1}{f_c} \tag{14}$$

where t_d is measured with the oscilloscope and f_c with a spectrum analyzer. The estimation of t_ϵ is performed in the passband of the MN for a minimal spectral shaping and maximal spectrum analyzer signal strength. The final estimate for t_ϵ is taken as the median of multiple measurements over the passband. Such an estimation is shown in Fig. 13(b). With t_ϵ known and t_d measured with the oscilloscope, the carrier frequency can be computed from (14). The root-mean-squared and peak-to-peak jitters of t_d are only 2.5 and 19 ps, respectively, at a 7.5-GHz carrier frequency measured over 10k samples. This root-mean-squared jitter level corresponds to a frequency jitter of ±5 MHz.

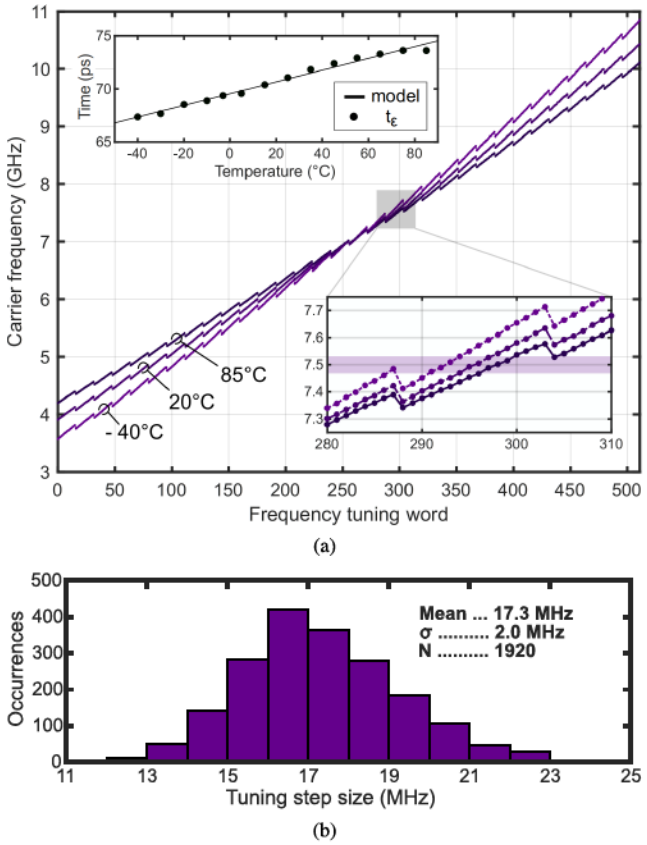

Fig. 14. Frequency tunability of the TFE. (a) Full frequency tuning range. (b) Fine frequency tuning step size measured for four dies.

The full tuning range of the delay chain is shown in Fig. 14(a). There is a temperature-independent carrier frequency point which is located at a $V_{\mathrm{dd}\Delta}$ level where the temperature effects of the threshold voltage and charge carrier mobility of an MOS transistor cancel each other out [26]. The target carrier frequency band between 6.5 and 8.0 GHz is fully covered over the industrial temperature range from −40 ° to 85 °C. Based on the simulations in [13], the target carrier frequency band is covered also at all process corners. The value of t_ϵ was estimated over temperature according to the linear model shown in the upper left corner of Fig. 14(a).

The fine frequency tuning resolution of the delay chain is presented in Fig. 14(b). The data consists of all the fine tuning steps of a full frequency sweep at room temperature. The TFE has an average fine frequency tuning resolution of 17.4 MHz with a 2.5-MHz standard deviation. Since fine tuning steps are slightly larger at the high end of the tuning range, as shown in Fig. 7(c), the distribution is slightly skewed. The maximum measured fine step size was smaller than 28 MHz.

The pulse shaping capability of the TFE is evaluated in Fig. 15(a). The output amplitude was estimated by measuring the average power of a rectangular pulse over a 3-ns window. The shown amplitude values are compensated with a measured cable loss. The TFE is programed with a Gaussian envelope and an approximately 500-MHz signal bandwidth at a 7.0-GHz carrier frequency in Fig. 15(b). The shown transient data are not compensated.

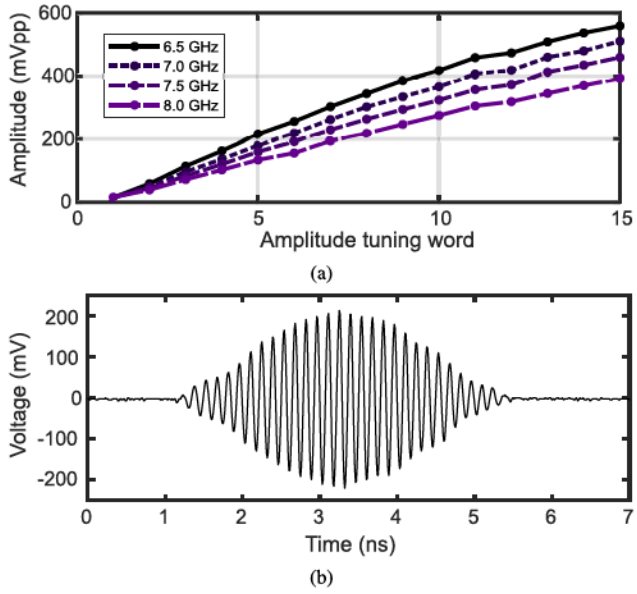

Fig. 15. Pulse shaping capability of the TFE. (a) Amplitude setting sweep. (b) 7.0-GHz Gaussian-envelope pulse.

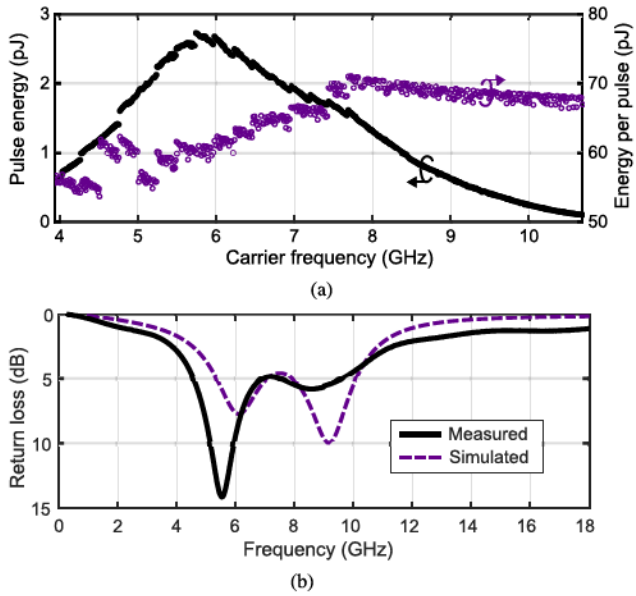

Fig. 16. Matching network performance. (a) Maximum pulse energy and consumed energy per pulse over the full frequency tuning range. (b) RF output return loss.

The TFE's maximum Gaussian pulse energy was measured over the full carrier frequency range as shown in Fig. 16(a). The pulselength was kept constant up to approximately 8 GHz, after which the maximum possible length was used (at least one impulse was propagated from all routers). The shown pulse energies are compensated with a measured cable loss. The TFE consumes more energy at high carrier frequencies since more sub-pulses are required to construct the output waveform. At a 7.5-GHz carrier frequency, the TFE generates 1.8-pJ pulses while consuming 63 pJ per pulse, corresponding to 2.3% efficiency. The TFE's static power consumption level is 380 nW.

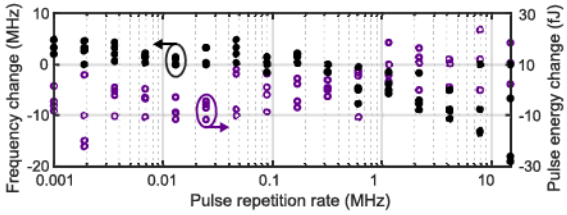

Fig. 17. Pulse energy and carrier frequency change as a function of PRR.

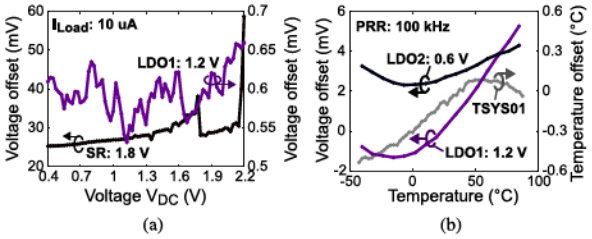

Fig. 18. Characterization of the discrete power management prototype. (a) Sensitivity of the 1.2-V LDO's output voltage to the input voltage V_{dc} of the SR. (b) The output voltage of the LDOs and the temperature offset of the temperature sensor from −40 ° to 85 °C.

Fig. 16(a) shows that the passband of the MN has a strongly skewed shape compared to the simulated expectation in Fig. 10(a). In addition, the center frequency of the passband has shifted down by about 500 MHz. These observations are confirmed by the measured return loss of the TFE output in Fig. 16(b). Based on our analysis, this could be largely explained by a decrease in the parallel resonant frequency of inductor L_1 and capacitor C_1. The undesirable effects of the changed characteristics include extra attenuation at the high end of the passband.

The stability of the output pulse waveform is evaluated in Fig. 17. The TFE was set to the four target carrier frequencies and its PRR was swept from 1 kHz to 15 MHz. The pulse energy levels remain virtually constant over the given PRR range. The TFE's carrier frequency levels drop slightly, by about 20 MHz, toward the maximum PRR.

As predicted by (19) in Appendix A, the TFE has a high power supply sensitivity, with measured values of approximately 17 and 5 MHz/mV for V_{dd} and V_{dd2}, respectively. Consequently, the TFE was tested with a discrete power manager prototype similar to the setup in Fig. 2. We use a MAX17220 from Maxim Integrated Products as a preliminary SR and two LT3009 from Linear Technology as LDOs. Nanowatt LDOs and switched converters have been presented in [27], [28], and [29], [30], respectively, and nanowatt subbandgap voltage references with mV-level stability over temperature have been reported in [31] and [32]. The regulators were equipped with their minimum recommended decoupling capacitors and the output of the SR was set to its minimum value of 1.8 V. The output voltage changes of the SR and 1.2-V LDO are shown in Fig. 18(a), referenced to their nominal values, when the input of the SR, V_{dc}, is swept from 0.4 to 2.2 V. Due to the double regulation, the LDO's output voltage level changes by less than ±0.1 mV, corresponding to a negligible effect on the TFE's carrier frequency. The 1.2-V LDO was loaded with a 10-μA constant current drain, and the

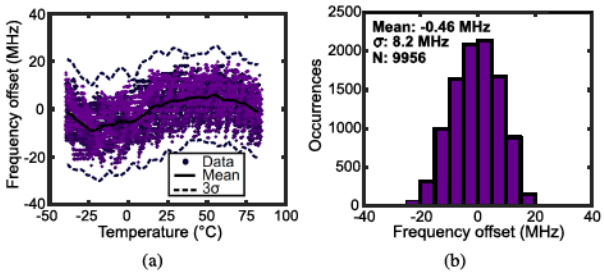

Fig. 19. Compensated TFE carrier frequency offset over the industrial temperature range measured for four dies. (a) All data points. The shown mean and standard deviation are taken over a moving 512-sample window. (b) Histogram of all data points.

SR was powered by a desktop power source using a battery emulation mode [33].

The temperature compensation procedure of Section II-D was applied to the TFE that was supplied by the power management prototype. A TSYS01 from TE Connectivity was used as a temperature sensor. The power management prototype was powered by the battery emulator at 1.2 V. The temperature sensitivity of the LDOs and the temperature offset of the temperature sensor are plotted in Fig. 18(b). The temperature offset of the sensor is referenced to the integrated sensor of the temperature chamber. The nonlinearities of the LDOs and TSYS01 are included in the compensation data and, consequently, taken into account by the compensation process. The TFE was set to a 100-kHz PRR and to switch constantly between four target carrier frequencies of 6.5, 7.0, 7.5, and 8.0 GHz. The temperature compensation was implemented in MATLAB from Mathworks for convenience. The TFE's carrier frequency was measured over the industrial temperature range at a temperature ramp rate of 0.4 °C/min. The measurement result is shown in Fig. 19. The proposed compensation method achieves an accuracy of about ±30 MHz (3σ).

The spectral quality of the TFE is shown in Fig. 20. The TFE was programed with a constant 1.3-pJ pulse energy level to achieve the same peak power density at the four target carrier frequencies. The measurement was performed according to ETSI TS 201 883 v1.1.1 [34] with a 1-MHz resolution bandwidth, 1-MHz video bandwidth, power average detector mode, maximum hold display mode, and 0.5 ms averaging time per point. The shown spectra are compensated with a measured cable loss. The mask is violated at a 100-kHz PRR by a low-frequency spectral peak at around 150 MHz that is caused by the on-chip power supply transients. The peak could be attenuated by 10 dB with a 0.6-pF off-chip dc decoupling capacitor at the TFE output, whose insertion loss at the passband of the MN was 0.3 dB. Additionally, the peak could be shifted down in frequency and attenuated further by removing the TFE's supply decoupling capacitors from the measurement PCB. This effect is probably due to the high-frequency supply ripple being attenuated by the low quality factor of the on-chip decoupling capacitors. With the 150-MHz peak attenuated, the TFE complies with the EC UWB mask for generic UWB usage [12] up to a 1-MHz PRR, after which the mask is violated by the second harmonics of the 8.0-GHz pulse train. The maximum PRR can be increased

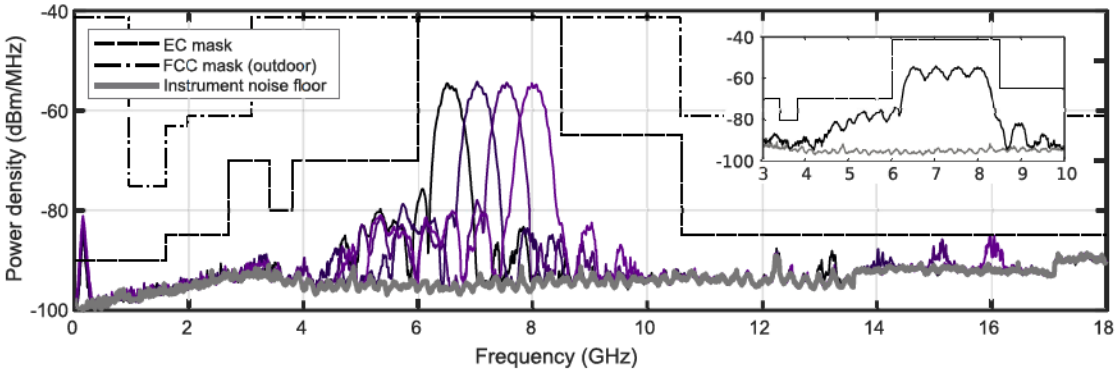

Fig. 20. Spectra of pulse trains centered at 6.5, 7.0, 7.5, and 8.0 GHz at a 1-MHz PRR. The frequency-hopping spectrum on the upper right corner is measured at a 4-MHz PRR. The EC mask is regulated in [12] and the FCC mask in [35].

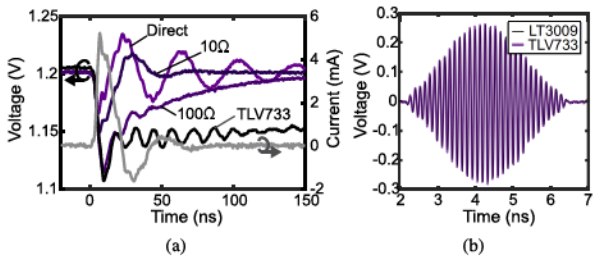

Fig. 21. Performance of the TFE with low-quality voltage sources. (a) Transient of V_{dd} when regulated by different LDOs. The output of LT3009 is connected to V_{dd} directly or with an additional 10-Ω or 100-Ω current-limiting resistor in series. The shown current peak is measured over the 10-Ω resistor. (b) Pulse waveform of the TFE when regulated by the two LDO models.

to up to about 4 MHz by applying frequency hopping between the four target carrier frequencies. The TFE suffers from an elevated level of harmonics compared to the simulations in [13]. This is probably caused by the additional losses of the MN at its passband, which decreases the relative attenuation of the second harmonics. Moreover, unlike in the simulations, the TFE is evaluated at its maximum pulse level, which increases its non-linearity, as shown in Fig. 15(a).

The TFE's tolerance to low-quality power sources and regulation is measured in Fig. 21. The TFE's 100-nF supply decoupling capacitors were removed from the measurement PCB, resulting in an approximately 0.4-dB decrease in its pulse energy, 30-MHz drop in its frequency level, and the previously discussed attenuation of the low-frequency spectral peak. The TFE was set to a 7.5-GHz carrier frequency and a 100-kHz PRR. The SR of the power management prototype was bypassed and the LDOs were powered by a 6.5-mm^2 monocrystalline photovoltaic with an output voltage and current level of 1.45 V and 15 μA. As shown in Fig. 21(a), the 1-μF output capacitor of the 1.2-V LDO prevents V_{dd} from dropping strongly during pulse generation but causes supply ripple. When 10-Ω surface-mounted resistors are placed in series with the LDOs, the magnitude of the voltage drop is similar to the simulated result in Fig. 5(d). Deploying a TLV733 from Texas Instruments in place of the 1.2-V LDO with no input or output decoupling capacitance resulted in an even stronger voltage drop. In addition, the TLV733 suffered from a high posterior ripple with a long settling time of 10 μs, which limits the maximum PRR of the TFE. Due to the higher current consumption of the TLV733, the current level of the photovoltaic was increased to 37 μA by changing ambient illumination and the TFE's frequency setting was lowered slightly to compensate for the TLV733's higher output voltage offset. The 0.6-V LDO was powered by the battery emulator to isolate its 100-nF input decoupling capacitor from the photovoltaic. The pulse energy and frequency was also measured with the TFE connected directly to a desktop power source with identical voltage offsets to the 1.2- and 0.6-V LDO. The pulse energy and frequency remained unchanged in all the above test cases. As an example, the virtually identical pulse waveforms of the TFE regulated by the TLV733 and the 1.2-V LDO are shown in Fig. 21(b). The above measurements show that the TFE can be used with low-drive regulators powered by low-quality power sources with a minor effect on its performance. However, the settling time of the applied regulator defines the maximum practical PRR.

IV. Comparison With Other Works

The performance of the TFE is compared with the current state of the art in Table I. The references have been selected with an emphasis on works whose performance has been evaluated by measurements and that combine a high pulse energy level with a low or moderate PRR. The TFE is compared at a 7.5-GHz carrier frequency where it is applicable globally.

The proposed TFE is the only one that targets the EC UWB mask. Since the EC mask is very strict, the TFE is also compliant in, for instance, the U.S., China, and Japan [4], [38]. The achieved compensated carrier frequency accuracy is better than the tuning resolution of the other edge-combiners and similar to that of the LO-based transmitters. While the TFE's pulse shaping capabilities and high integration level come with a significant power penalty, it achieves an energy-efficiency level comparable with most other works. The works that employ the FCC mask or a low carrier frequency level may gain in power efficiency but they can only be employed globally at a significantly lowered PRR or by applying mitigation techniques [5].

The proposed TFE retains a very low power consumption level over a wide range of PRRs due to its low static current consumption, as shown in Fig. 22. This feature is particularly practical in energy-harvesting applications where

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART LOW-POWER UWB IR TFEs

	This work	Vauche* TCAS-I 2017 [11]	Miranda CICC 2010 [8]	Na TCAS-II 2015 [9]	Soldà* JSSC 2011 [36]	Huang* JSSC 2013 [37]	de Streel JSSC 2017 [3]	Dokania* TCAS-II 2010 [7]
CMOS tech. (nm)	65	130	65	65	130	180 BiCMOS	28 FDSOI	90
Core area (mm^2)	0.22	0.11	-	0.18	0.25◁	0.10◁	0.10‡	0.42
Architecture	Edge -combiner	Edge -combiner	Edge -combiner	Edge -combiner	LO -based	LO -based	LO -based	LO -based
Spectral compliance	**Global**	FCC	FCC	FCC	FCC	FCC	FCC	FCC
Integration level	Full/High▷	Full	Ext. matching	Ext. BP filter	Full	Full	Full	Full
f_c range (GHz)	6.5–8.0	3–5	3.6–7.5	3.1–4.8	6.6–9.0	7.5–12.2	3.5–4.5	3.5–4.5
f_c resolution (MHz)	**28**	Analog tuning	1000×	110^	80	–	–	Analog tuning
Pulse shaping (bits)	**4**	Analog	3	0	0	1	5	1
Static power (μW)	**0.38**	100	13	–	–	170 pW	–	5
PRR (MHz) | f_c (GHz)	1 | 7.5	1 | 4	12 | 3.6	200 | 3.3	5 | 7.5	0.03 | 9.8	6.81 | 4.5	0.1 | 3.5
Pulse energy★ (pJ)	1.8	0.64	2.4×	0.7†	13.2	1.5†	0.64	1.0†
Energy per pulse★ (pJ)	63	250	9.6×	30	186	747	30‡	80
Efficiency★ (%)	**2.3**	0.26	25×	2.3†	7	0.2†	2.1‡	1.3†

* Paper also includes a receiver.
★ At the conditions defined by row PRR (MHz) | f_c (GHz).
‡ Includes digital baseband.
† Estimated from the reported pulse waveform.
× f_c resolution estimated from [8, Fig. 4]. Pulse energy estimated from [8, Fig. 5] at 0.75-V antenna driver voltage.
^ Estimated from [9, Fig. 2(b)].
◁ Estimated from the reported die photograph.
▷ An external DC decouling capacitor required for global spectral compliance at PRRs from 0.5 to 4 MHz

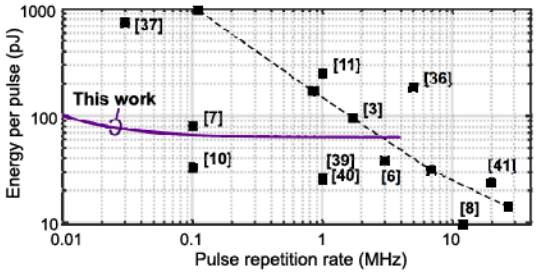

Fig. 22. Comparison with other recent UWB IR transmitter designs of similar characteristics.

the scavenged power level may vary from microwatts to milliwatts depending on ambient conditions and harvester size. In contrast, a transmitter with a high static power consumption level or limited duty-cycling capabilities loses its power efficiency already at moderate PRRs, such as in [3] and [11]. All the compared designs in Fig. 22 target either the FCC mask or no maks in particular. While the transmitters in [8], [10], [39], [40], and [6] feature a lower power consumption level than the proposed TFE, they nevertheless suffer from coarse carrier frequency tuning and/or pulse shaping capabilities. In addition, they all operate at a low FCC frequency band.

V. CONCLUSION

We demonstrated a fully integrated UWB IR TFE based on the edge-combining architecture, integrated in a 65-nm CMOS process. The TFE's delay chain is equipped with a propagation delay tuning method based on isolated supply capacitor banks. The proposed tuning method features a high tolerance to supply transients and achieves a carrier frequency tuning resolution of 28 MHz, comparable to LO-based architectures. We showed that the temperature dependence of the delay chain can be compensated over the industrial temperature range by employing precharacterized calibration constants and a quadrature interpolator.

The TFE is compliant with the EC UWB mask up to a 4-MHz PRR due to its pulse shaping features and an integrated power amplifier MN. Unlike designs targeting the FCC UWB mask, this design has a wide global applicability. The TFE delivers 1.8-pJ pulses at a 7.5-GHz carrier frequency with 2.3% total efficiency. The static power consumption level is 380 nW, allowing a high efficiency level even at low data rates.

The TFE was demonstrated to operate robustly with low-drive regulators without off-chip supply decoupling. This feature is particularly practical in energy-harvesting applications. In comparison to the state of the art, the TFE features a high spectral quality, a high carrier frequency tuning resolution, a low static power consumption level, and a comparable energy efficiency.

APPENDIX A

The capacitor bank of a delay unit is depicted in Fig. 6(b). The total parallel capacitance in the bank is given by the sum

of the fine unit capacitors C_f, coarse unit capacitors C_c, and capacitor C_0, according to

$$C_{\text{bank}} = C_0 + (2^M - 1)C_c + (2^N - 1)C_f \tag{15}$$

where M is the number of coarse tuning bits and N is the number of fine tuning bits. Capacitors C_f, C_c, and C_0 are based on poly–p-well capacitors biased in the linear region, and their sizes are 2.1 and 33 fF for the fine and coarse banks, respectively. In addition to these nominal values, the unit capacitors include parasitic routing capacitances, whose extracted values from layout are 0.48 and 1.6 fF for C_f and C_c, respectively. In both cases, approximately two thirds of the parasitic routing capacitance connect to ground. Routing has a more significant relative effect on the fine unit capacitor size. The bottom-plate parasitics have a negligible effect on the bank since the capacitors' body terminals and wells are connected to the ground potential along with the substrate. While the bottom plates are resistive, the charges have enough time to distribute evenly before the triggering of the delay chain, as shown in Fig. 6(c). The total charge in the voltage divider is given by

$$Q_{\text{bank}} = C_0 V_{\text{dd}} + C_c \sum_{i=0}^{M-1} 2^i V_{c,i} + C_f \sum_{j=0}^{N-1} 2^j V_{f,j} \tag{16}$$

where $V_{c,i}$ and $V_{f,j}$ obtain the value of V_{dd} or V_{dd2} depending on the position of switches S. We can formulate

$$V_{c,i} = (V_{\text{dd}} - V_{\text{dd2}})D_{c,i} + V_{\text{dd2}} \tag{17}$$

$$V_{f,i} = (V_{\text{dd}} - V_{\text{dd2}})D_{f,i} + V_{\text{dd2}} \tag{18}$$

where $D_{c,i}, D_{f,j} \in \{0, 1\}$ are the single tuning bits of frequency tuning words D_c and D_f. Substituting the above formulations in (16) gives

$$\begin{aligned} Q_{\text{bank}} &= \overbrace{C_0 V_{\text{dd}} + C_c V_{\text{dd2}} \sum_{i=0}^{M-1} 2^i + C_f V_{\text{dd2}} \sum_{j=0}^{N-1} 2^j}^{Q_0} \\ &\quad + \overbrace{C_c(V_{\text{dd}} - V_{\text{dd2}})}^{Q_c} \sum_{i=0}^{M-1} 2^i D_{c,i} \\ &\quad + \overbrace{C_f(V_{\text{dd}} - V_{\text{dd2}})}^{Q_f} \sum_{j=0}^{N-1} 2^j D_{f,j} \\ &= Q_0 + Q_c \sum_{i=0}^{M-1} 2^i D_{c,i} + Q_f \sum_{j=0}^{N-1} 2^j D_{f,j}. \end{aligned} \tag{19}$$

Since $C_c > C_f$, it follows that $Q_c > Q_f$.

ACKNOWLEDGMENT

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Tuomas Haapala (Student Member, IEEE) received the M.Sc. degree in biotronics from Aalto University, Espoo, Finland, in 2015, where he is currently pursuing the Ph.D. degree under the supervision of Prof. Kari Halonen. He joined the Department of Electronics and Nanoengineering, Aalto University, in 2011. In 2018, he was a visiting Ph.D. student at the University of Toronto, Toronto, ON, Canada, under the supervision of Prof. Antonio Liscidini. His research interests include low-power analog, digital and RF circuits for the massive IoT.

Tuomas Rantataro received the B.Sc. degree in bioinformation technology from Aalto University, Espoo, Finland, in 2015. He is currently pursuing the M.Sc. degree in biosensing and bioelectronics. From 2015 to 2017, he worked as a Research Assistant with the Department of Electronics and Nanoengineering, Aalto University, in the research group of Prof. Kari Halonen. His research interests lie with digital electronics.

Kari A. I. Halonen (Member, IEEE) received the M.Sc. degree in electrical engineering from Aalto University (formerly the Helsinki University of Technology), Espoo, Finland, in 1982 and the Ph.D. degree in electrical engineering from Katholieke Universiteit Leuven, Leuven, Belgium, in 1987.

He became the Head of the Electronic Circuit Design Laboratory in 1998 and was appointed as the Head of the Department of Micro- and Nanosciences, Aalto University, from 2007 to 2013. Since 1988, he has been with Electronic Circuit Design Laboratory, Helsinki University of Technology (since 2011 Aalto University), Espoo, Finland. Since 1993, he has been an Associate Professor with the Faculty of Electrical Engineering and Telecommunications, where he has also been a Full Professor since 1997. He specializes in CMOS and BiCMOS analog and RF integrated circuits, particularly for telecommunication and sensor applications. He has authored or coauthored over 450 international and national conference and journal publications on analog and RF integrated circuits.

Dr. Halonen was a TPC member of ESSCIRC and ISSCC. He was a recipient of the Beatrice Winner Award of the ISSCC Conference 2002. He has been an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I: REGULAR PAPERS, a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, and the Technical Program Committee Chairman of the European Solid-State Circuits Conference in 2000 and 2011.