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A 0.6–4.0 GHz RF-Resampling Beamforming Receiver with Frequency-Scaling True-Time-Delays up to Three Carrier Cycles

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***Abstract*—True-time-delays enable wideband analog and hybrid beamforming by mitigating the beam squint problem. This paper reports a true-time-delay beamforming receiver supporting delays up to three carrier-frequency cycles. The implementation is the first published work in which the delays scale with the carrier frequency. The scaling enables true-time-delays for large arrays at low-GHz frequencies where long delays are required due to $\lambda_c/2$ antenna spacing. The delays are implemented through delayed resampling of a passive mixer's discrete-time output. Driving the mixers with pulse-skipped local oscillator (LO) signals allows the delay range to exceed one carrier cycle. A polyphase receiver structure prevents aliasing of noise and unwanted tones caused by LO pulse-skipping. Our prototype implementation demonstrates squint-free beamforming for an 800 MHz instantaneous RF bandwidth. The proposed true-time-delay is efficient for large arrays since the power consumption per antenna is only 5–13 mW across the 0.6–4.0 GHz frequency range. The prototype was implemented in 28-nm FD-SOI CMOS, and the die area including bonding pads is only 1.2 mm^2.**

***Index Terms*—Analog beamforming, beam squint, CMOS, hybrid beamforming, phased array, radio receiver, resampling, RF sampling, spatial filtering, true-time-delay.**

I. Introduction

Hybrid beamformers [1] combine analog and digital beamforming to improve signal-to-noise ratio and in-band interference tolerance of a receiver through spatial diversity. Digital beamforming provides flexibility and accuracy of numerical computation to enable spatial multiplexing of multiple users simultaneously. On the other hand, analog beamforming helps relax the linearity and dynamic range requirements of the receiver chain and A/D conversion [2]. Analog beamforming is typically implemented by equalizing the propagation delays from the antenna array with phase shifters. However, a phase shift equals delay only on a single frequency. Hence, approximating delay with phase shifters for signals with a wide relative bandwidth results in frequency-dependent beam squint [3]. Squinting causes error in the directivity of the array and hence power loss for signals from the target direction.

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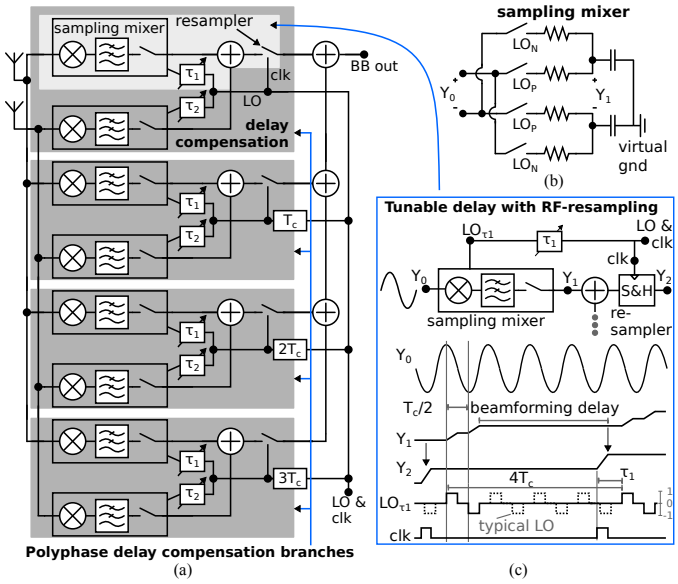

Fig. 1. Proposed beamforming receiver: (a) signal flow graph with four polyphase branches (Q mixers not shown), (b) passive mixer configuration for sampling, and (c) illustration of beamforming delay with RF-resampling and the waveforms of the first delay path of the receiver.

This paper continues our work in [4] by presenting an implementation of a true-time-delay (TTD) analog beamformer with a relative delay range of three cycles (T_c) of a carrier frequency (f_c) over 0.6–4.0 GHz frequency range. TTD beamforming prevents beam-squinting, and therefore enables wideband spatial multiplexing before A/D conversion [3]. The beamforming delays of $3T_c$ are implemented with a combination of RF-resampling and pulse-skipped LO signals. A passive mixer creates a discrete-time output, which is resampled at the LO frequency. The delay between the mixer's LO and the resampler clock appears as a delay for the received signal. The pulse-skipped LO signals enable the extension of the delay range beyond T_c.

Our implementation offers several improvements over published true-time-delay beamforming solutions [5]–[9]. The proposed RF-resampling TTD method is the only one published, which scales the delays with f_c. The scaling enables long absolute delays for supporting large arrays at low frequencies, where antenna spacing set by $\lambda_c/2$ is large. In addition to viable operation at low f_c, our implementation has the highest published TTD operating frequency of 4 GHz among area-efficient inductorless designs. The RF-resampling can take

advantage of technology scaling, as its operation benefits from increasing speed and time resolution of the semiconductor processes. The implementation achieves state-of-the-art power consumption per antenna by sharing all amplifiers between antenna paths.

Section II describes the proposed architecture and the implemented IC prototype. Measurement results are presented in Section III, followed by conclusions in Section IV.

II. True-Time-Delay Beamforming Receiver

A. True-Time-Delay with RF-Resampling

Fig. 1 shows the block diagram describing the signal processing steps of the proposed true-time-delay beamforming receiver with RF-resampling. Each delay compensation block combines individually delayed signals from each antenna. The delays are implemented with a sampling mixer, which has a purely capacitive output as shown in Fig. 1 (b), followed by a resampler as shown in Fig. 1 (c). The received signal Y_0 is first down-converted and filtered by the RC frequency response of the sampling mixer, producing a discrete-time baseband (BB) signal Y_1. Then the baseband signals are resampled during the mixer's hold period, which produces a delayed version of Y_1 at Y_2. Delay tuning for each antenna is implemented with individually programmable timing offset between the LO signals of separate antennas and the resampler clock. The resampler is shared between antenna inputs by placing it after the beamforming summation. The addition of the resampling function extends LO phase-shifting to a true-time-delay for beamforming.

The maximum beamforming delay is set by the mixer's hold period length. Pulse-skipped LO signals, shown in Fig. 1 (c) as $\mathrm{LO}_{\tau 1}$, increase the delay tuning range beyond one carrier cycle and hence enable true-time-delay beamforming for larger antenna arrays. The pulse-skipped LOs consist of a positive and negative pulse with $T_c/2$ separation repeated with sample period $4T_c$. Compared to a typical LO signal, the pulses shown with a dashed line have been skipped. The selected LO sample period allows a delay range from 0 to $3T_c$, the range being limited by not allowing the LO signal and resampler clock to overlap. The true-time-delays scale from 5000 ps to 750 ps over our prototype's frequency range of 0.6–4.0 GHz. The sample period can be increased by further pulse-skipping to enable an even larger beamforming delay range.

A single delay compensation block driven with a pulse-skipped LO can implement true-time-delays of $3T_c$. However, down-conversion with the pulse-skipped LO which has a lowered sample rate would result in aliasing of blockers present at the antennas as well as thermal noise from multiples of $f_c/4$ on top of the desired baseband signal. To avoid the aliasing, we propose a polyphase aliasing cancellation consisting of four identical delay compensation branches. The branches are time-offset from each other by T_c through delaying the LOs and resampler clocks. Summation of the branch outputs allows the receiver to operate with an effective sample rate of f_c. The delay range of the receiver can be increased by lowering the LO sample rate by skipping more pulses of the continuous The noise performance of the polyphase structure equals one

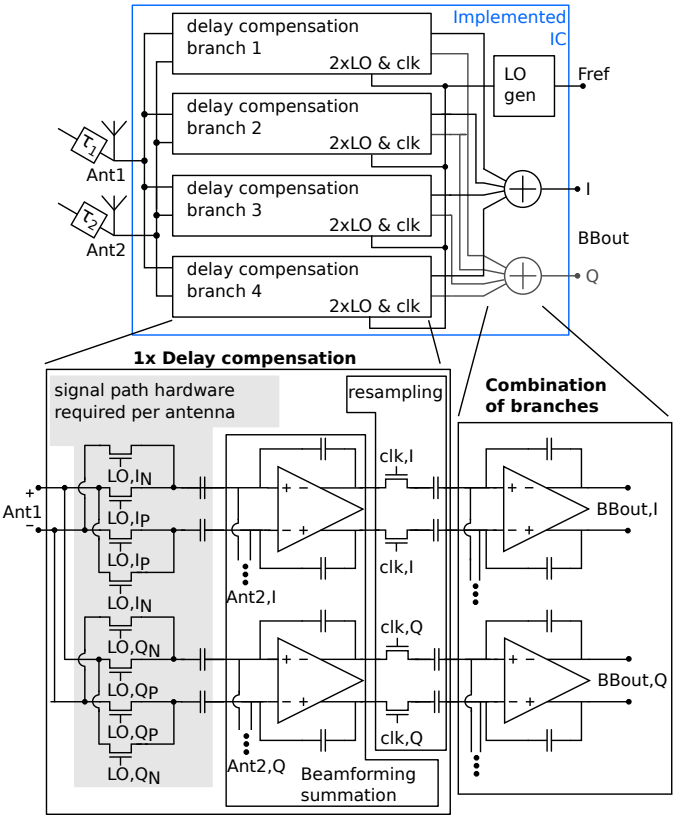

Fig. 2. Receiver front-end block diagram and circuitry for one receive path

branch sampling at f_c, and thus true-time-delay beamforming delays up to $3T_c$ are enabled without an increase in noise.

B. Receiver Prototype

The proof-of-concept prototype receiver front-end with 2 antenna inputs is shown in Fig. 2. Mixer-first architecture was chosen to demonstrate the wide frequency range of the proposed RF-resampling true-time-delay beamforming, but it is possible to include LNAs. The chip includes the four polyphase delay compensation branches, each producing beamformed I and Q baseband outputs. The branch outputs are combined to achieve the polyphase aliasing cancellation. The on-chip LO generator produces the required pulse-skipped LOs with delay from 0 to $3T_c$.

Typically individual delay elements are implemented for each antenna causing the power consumption of beamforming to increase linearly with the number of antennas. In contrast, the proposed receiver requires only polyphase passive mixers and related LO generation for each added antenna, as highlighted with grey in Fig. 2. The mixers and LO generator have low power consumption as they rely on switching and CMOS logic. On the other hand, the power-hungry baseband amplifiers are shared between antennas. The low power overhead per antenna makes the proposed true-time-delays feasible for large arrays.

The LO generator shown in Fig. 3 (a) creates the required control signals for the polyphase delay compensation branches. Fig. 3 (b) depicts two separately delayed quadrature pulse-skipped LOs and the resampler clock required for beamforming in one polyphase branch. In the example of Fig. 3 (b), the

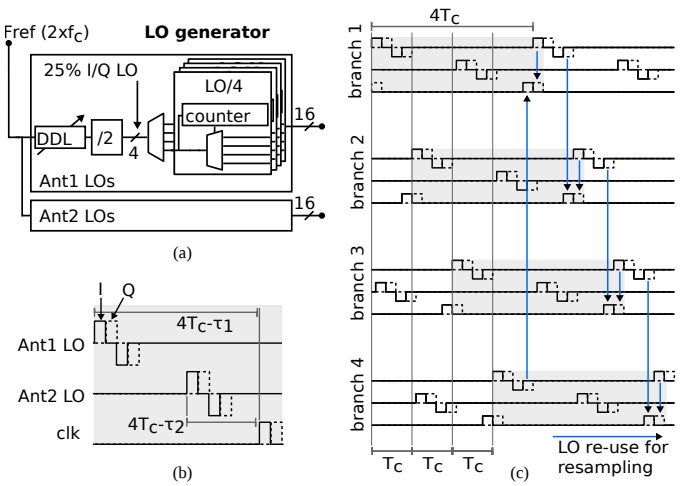

Fig. 3. (a) LO generator, (b) LOs and resampler waveforms for delay compensation block of one branch, and (c) control signals for the full receiver.

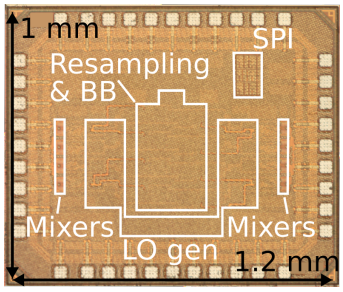

Fig. 4. Chip micrograph.

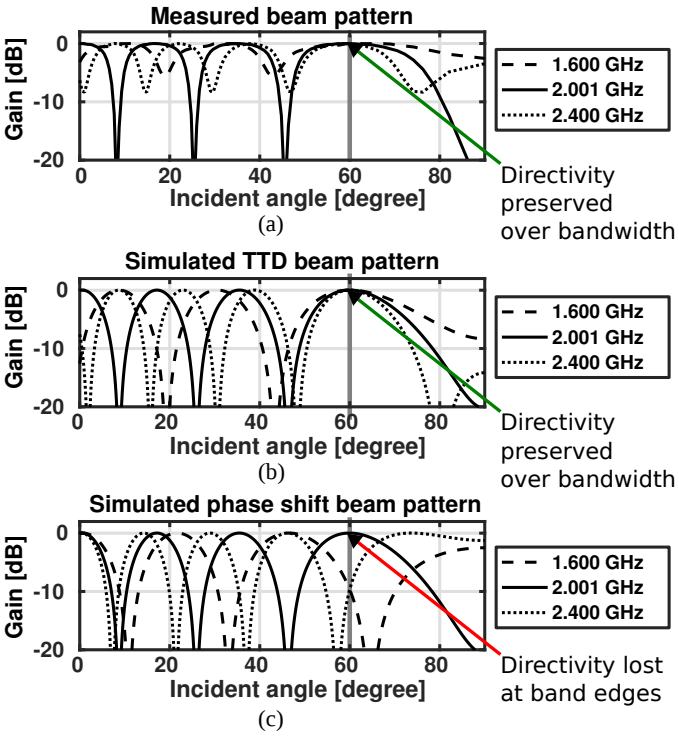

Fig. 5. Beamforming over 800 MHz RF bandwidth: (a) measured result with main beam direction remaining constant across the bandwidth, (b) simulated true-time-delay beamforming with matching beam directions compared to measurement, and (c) simulated phase-shift beamforming demonstrating squint which is prevented with true-time-delays.

LO delay difference between the two antennas is over $2T_c$, showing how the pulse-skipped LO's delay tuning can exceed one carrier cycle. The other polyphase branches are driven with the same set of signals, with delays of T_c between each branch as shown in Fig. 3 (c). A divide-by-two circuit creates four-quadrant I/Q LO signals at f_c from a reference signal at $2f_c$. Each quadrature LO is then fed to separate divide-by-four blocks that multiplex consecutive pulses to different polyphase branches. This multiplexing realizes both pulse-skipping for the individual LOs and the required T_c delays between the polyphase branches. Coarse beamforming-delay tuning steps of $T_c/4$ are selected with digital control in the first multiplexer. Further steps of size T_c are selected by setting the counter to different states, changing the order of the polyphase signals compared to the other antenna. Delay fine-tuning with a resolution of 35 ps is implemented by tapping different nodes of an inverter chain delay line before the quadrature LO generation. Certain LO signals of antenna 1, which is chosen as a reference, are re-used as the resampling clocks as shown in Fig. 3 (c). The presented circuit was implemented in 28-nm FD-SOI CMOS, and the chip micrograph is presented in Fig. 4. The total die area including the pad ring is 1.2 mm^2.

III. Measurement Results

Fig. 5 presents the measured wideband true-time-delay beamforming with the prototype. In this particular implementation, the mixers and baseband amplifiers were designed for a 70-MHz baseband bandwidth, while the proposed technique of true-time-delay with RF-resampling is inherently bandlimited only by the Nyquist criterion, thus operating up to $f_c/2$ offsets from the carrier. Hence, in Fig. 5 (a) we are able to show squint-free directivity towards 60 degrees over an 800-MHz RF bandwidth around f_c of 2 GHz. The measured directivity at 1.600 GHz, 2.001 GHz and 2.400 GHz match the simulated TTD beamforming shown in Fig. 5 (b), verifying squint-free TTD operation for a 40 % relative bandwidth. The beamforming zero depth is limited due to operating outside the bandwidth of the summation amplifier. The two inputs of the chip were chosen to represent the two outermost antennas of an array with 8 antennas with $\lambda_c/2$ spacing. The resulting 3.5 λ_c input spacing with the target angle of 60 degrees requires delays of $3T_c$, and the result verifies the delay range increase offered by the pulse-skipped LO.

The benefit of the true-time-delay beamforming is illustrated with a comparison to simulated phase-shift beamforming, which suffers from squint. As shown in Fig. 5 (c), phase-shift beamforming for the same test setup leads to the directivity towards 60 degrees being practically lost, causing more than 9 dB loss from the target direction. The grating lobes visible in the measured and simulated beam patterns of Fig. 5 are an expected side-effect of the test setup with the large antenna spacing. The grating lobes are not related to the proposed beamforming implementation.

Fig. 6 (a) shows beamforming within the receiver's baseband bandwidth. The measurement done at $\pm$ 70 MHz from f_c of 3 GHz demonstrates spatial selectivity of more than 15 dB. The achieved selectivity doesn't require gain calibration between antenna paths in this implementation as signals from

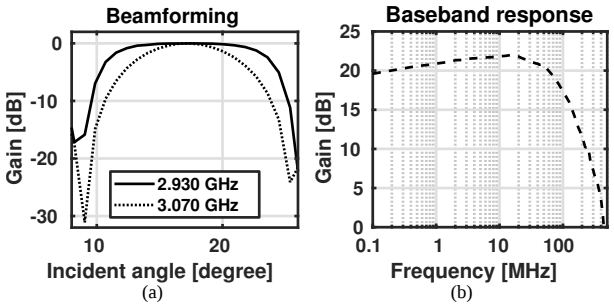

Fig. 6. (a) Measured main lobe of the beam pattern at the edges of a 140 MHz instantaneous RF bandwidth, and (b) measured baseband frequency response from 2 GHz carrier frequency.

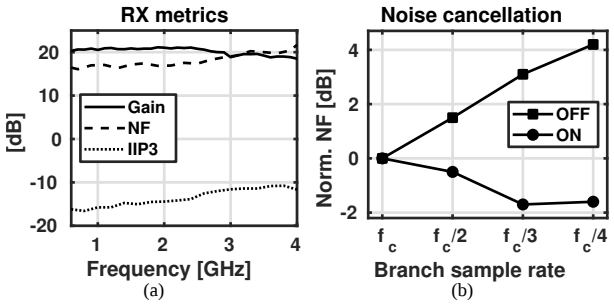

Fig. 7. (a) Measured RX performance showing the dependency of gain, noise figure and IIP3 on input frequency, and (b) polyphase noise cancellation.

both antennas are amplified with the same amplifier. The baseband bandwidth of 70 MHz is shown in Fig. 6 (b) as down-conversion gain to baseband from a frequency band of 500 MHz above a 2 GHz carrier. Further RX characteristics of the prototype are presented in Fig. 7 (a). The measured gain is 19–21 dB over the input frequency range 0.6–4.0 GHz. The noise figure, integrated from 1 to 70 MHz, is 16–20 dB, and is mainly limited by the noise contribution of the beamforming amplifier. In-band IIP3 is -11– -16.5 dB with test tones at 30 and 48 MHz offsets from the carrier.

Fig. 7 (b) demonstrates how the polyphase structure prevents noise aliasing, when pulse-skipped LO is used to decrease the LO sample rate and increase delay range. The NF plots are normalized to the case when the LO sample rate is f_c, thus not requiring parallel aliasing compensation branches. With the polyphase branches ON, lower sample rates do not increase NF. The decrease in NF which saturates at a sample rate of $f_c/3$ is due to increased gain from a single antenna to the output. When only one branch is active (compensation OFF), decreasing sample rate leads to an expected increase in NF due to aliasing. The result shows that the polyphase structure allows the pulse-skipped LOs without an increase in NF.

Table I summarizes the measured performance of the prototype, and compares it to the state-of-the-art [5]–[8]. The proposed true-time-delay front-end provides the widest reported frequency range of 0.6–4.0 GHz, which is realized without area-consuming inductors. The front-end has the smallest power consumption overhead per antenna path of 5–13 mW.

IV. Conclusion

This paper presents a true-time-delay beamforming receiver front-end based on RF-resampling. The front-end has the largest inductorless TTD frequency range of 0.6–4.0 GHz. The delay range of $3T_c$ scales with f_c, supporting a fixed antenna array size regardless of $\lambda_c/2$. Squint-free beamforming is demonstrated for an 800 MHz instantaneous bandwidth. The TTD with RF-resampling is power efficient for large arrays, since additional antenna paths require only 5–13 mW each across the frequency range.

TABLE I
Comparison to state-of-the-art TTD beamforming solutions

	[5]	[6]	[7]	[8]	[9]	**This Work**
Delay method	LC	Gm-C	Gm-C	BB-resampling	VTC combining	**RF-resampling**
Frequency range [GHz]	2 – 20	1 – 2.5	0.1 – 2	N/A[1]	N/A[1]	**0.6 – 4**
Beamforming BW [Ghz]	18	1.5	1.9	0.1	0.5	**0.8**
Delay tuning range [ps]	508	550	1450	15000	1000	**750 – 5000[2]**
Delay resolution [ps]	4	13	10	5	N/A	**35**
Power [mW]	285[3]	90[3]	112 – 364[3]	47[4]	40[4]	**70[5]**
Power required for additional antennas [mW]	285	90	112 – 364	N/A	N/A	**5 – 13[2]**
Techonology [nm]	130 (SiGe)	140	130	65	65	**28**
Active area [mm^2]	5.54[6]	0.07	0.29	0.57[4]	0.31	**0.13[5]**
Single channel RX performance						
BW [GHz]	2 – 20	1 – 2.5	0.1 – 2	0.1	0.5	**0.07**
Gain [dB]	-7.2 – 0	12 – 15	0.6	N/A	N/A	**19 – 21**
Noise figure [dB]	N/A	8 – 10[7]	17.5 – 23	N/A	N/A[8]	**16 – 20**
IIP3 [dBm]	N/A	-13 – -20	-4.6 – 4.9	N/A	7.9[1]	**-11 – -16.5**
P1dB [dBm]	N/A	-21 – -28	N/A	N/A	-0.5[1]	**-23 – -27.5**

[1]Baseband implementation. [2]Scales with f_c. [3]1 RF delay path. [4]4 input baseband beamformer. [5]Front-end shared power consumption + 1 input. [6]Chip area. [7]Average between best and worst case delay settings. [8]32.6 dB SNDR

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