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Published in:
IEEE Access

DOI:
10.1109/ACCESS.2020.3020865

Published: 01/01/2020

Document Version
Publisher's PDF, also known as Version of record

IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Date of publication xxxx 00, 0000, date of current version xxxx 00, 0000.

Digital Object Identifier 10.1109/ACCESS.2017.Doi Number

Modular Design and Thermal Modeling Techniques for the Power Distribution Module (PDM) of a Micro Satellite

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ABSTRACT The power distribution module (PDM) is one of the vital modules onboard small satellites and its design governs the performance of all the subsystems including communication, attitude determination & control, navigation, payload, etc. The paper presents the design of the PDM developed for the Pakistan National Student Satellite-1 (PNSS-1). The main focus of the design is modularity, redundancy, design reuse and miniaturization using commercial off the shelf (COTS) components. PDM is the sub-module of electric power system (EPS) which converts the power distribution bus (PDB) voltage level (unregulated 28V) into the secondary voltage levels and to distribute these voltages to loads according to their requirements. In order to improve reliability and to overcome various failures, redundancy is provided at all levels. No single component failure in PDM disables or degrades its intended functions that may lead to mission failure. Latch-up protection circuit is designed for the CMOS processor and at the end a thermal model is presented for the PDM unit.

INDEX TERMS Power distribution, redundancy, radiation effects, thermal resistance

I. INTRODUCTION

Small satellite is one of the most rapidly developing sector in space industry due to low cost, small size and less development time as compared to their counterpart (conventional satellites). Recent technological advancements such as subsystems modularity, redundancy, diversity, miniaturization and integrated circuits (ICs) development have further enhanced small satellites capabilities in terms of their longer lifespan, less development time and cost, large data handling capability and accommodating more subsystems on-board [1]. Typically, subsystems on-board of a small satellite includes attitude sensors and control systems, telemetry and telecommand transceiver system, on-board data handling system, communication antennas, and the electrical power system (EPS) [2].

Many universities and organizations are working on small satellites projects around the globe. According to studies, currently 377 known future small satellites are in the Satellite Launch Demand Database (LDDB) [3]. The global space economy in 2018 was valued at over $383.5 Billion in commercial revenue and government budgets, and is expected to double by 2030 [4]. According to a report by the Bank for International Settlements (BIS) research, the global market of small satellites is expected to reach $566.2 million by 2022, growing at a compound annual growth rate (CAGR) of 33.4% during the period, 2016 – 2022 [5]. This extensive interest worldwide in the small satellites development area is due to several advantages offered by small satellites over their larger counterparts. The main objective of small satellite development is to have fast and low-cost projects; however, the high probability of failure (about 40% for university-led missions) and poor life expectancy are known drawbacks related to these projects [6]. The electrical power system (EPS) is one of the leading causes for it. Therfore, improving the reliability of the EPS for a nanosatellite significantly reduce the failure rate and improve success ratio [7]. As commercial microelectronic devices can be used for rapid and cost-effective design of EPS for a

nanosatellite but there many limitations associated with it. Such limitations include the lack of expertise for efficient correlation between reference schematic designs of the EPS functional unit and spacecraft subsystems or the ability to troubleshoot EPS as required during a mission [8]. EPS consist of four primary functions i.e. power source, energy storage, power regulation & control and power distribution.

At the time of writing this paper, more than 1000 CubeSats have been launched since they began in early this century [9]. Unfortunately, the underdeveloped countries are far behind in the race for university satellites development in comparison with technology advanced nations like USA, as reflected in Figure 1 [10]. Therefore it seems an appropriate time to focus on the indigenous small spacecraft technology that may open new avenues of innovation and take the space capabilities a step further.

In this regard, Pakistan, Space and Upper Atmosphere Research Commission (SUPARCO) also launched a program of satellite series in collaboration with Pakistani universities and local industry. This program is called Pakistan National Student Satellite (PNSS) program. Pakistan National Student Satellite-1 (PNSS-1) is the first satellite of this series. PNSS-1 has a weight of 50 ± 5kg, average power requirement of 50W and dimensions of 450×450×450 mm^3. It is a modular satellite basically comprised of 14 modules [11] accommodating nine subsystems including payload as shown in Figure 2.

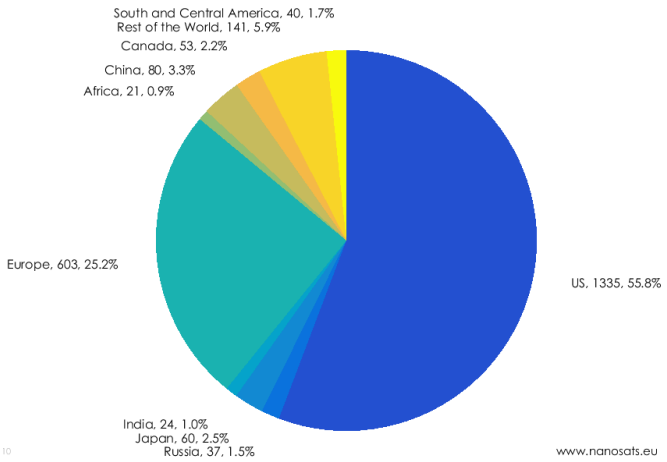

FIGURE 1. **Nation-wise contribution for Nanosatellite (launched, planned and cancelled) missions [10]**

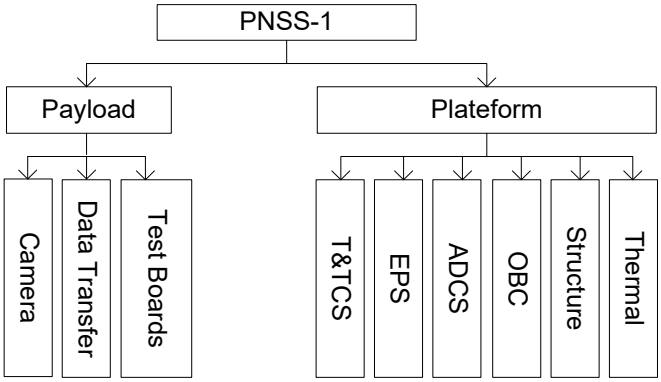

FIGURE 2. **PNSS-1 subsystems**

A number of universities and industrial entities across Pakistan are involved in the design and development of the PNSS-1 satellite. Our group worked on the design and development of Electric Power Supply (EPS) and Attitude Determination & Control System (ADCS). The PNSS-1 EPS block diagram as in Figure 3, constitutes of three modules where Power Distribution Module (PDM) [12] is one of them.

The EPS is responsible for efficient and reliable power generation, its conversion to different power and voltage levels, power storage and proper distribution to various subsystems on-board the satellite according to their requirements [11, 13]. EPS being the vital part has a high probability of failure (about 40% for university-led missions) and poor life expectancy [14]. Thus, improving the reliability of the EPS for a nanosatellite shall greatly reduce failure rate and improve success ratio [15]. EPS of PNSS-1 has four solar panels which are located on its external periphery (four sides). The exterior dimension of the single solar panel is 450×450 mm^2 which absorbs 276W at AM0 and with 28% of solar panel efficiency, generates 77W useful electrical power. The solar panels output power is unstable and has different voltage and current levels that varies with sun irradiance and other environmental aspects. The Power Conditioning Module (PCM) have Maximum Power Point Tracking (MPPT) buck converter with current and voltage sensors that converts the unstable power from solar panels into stable power level which feeds the power distribution bus (PDB) and regulates the battery charge and discharge [14]. The PDM module is connected on the PDB and provides secondary voltage levels to satellite loads as per their requirements.

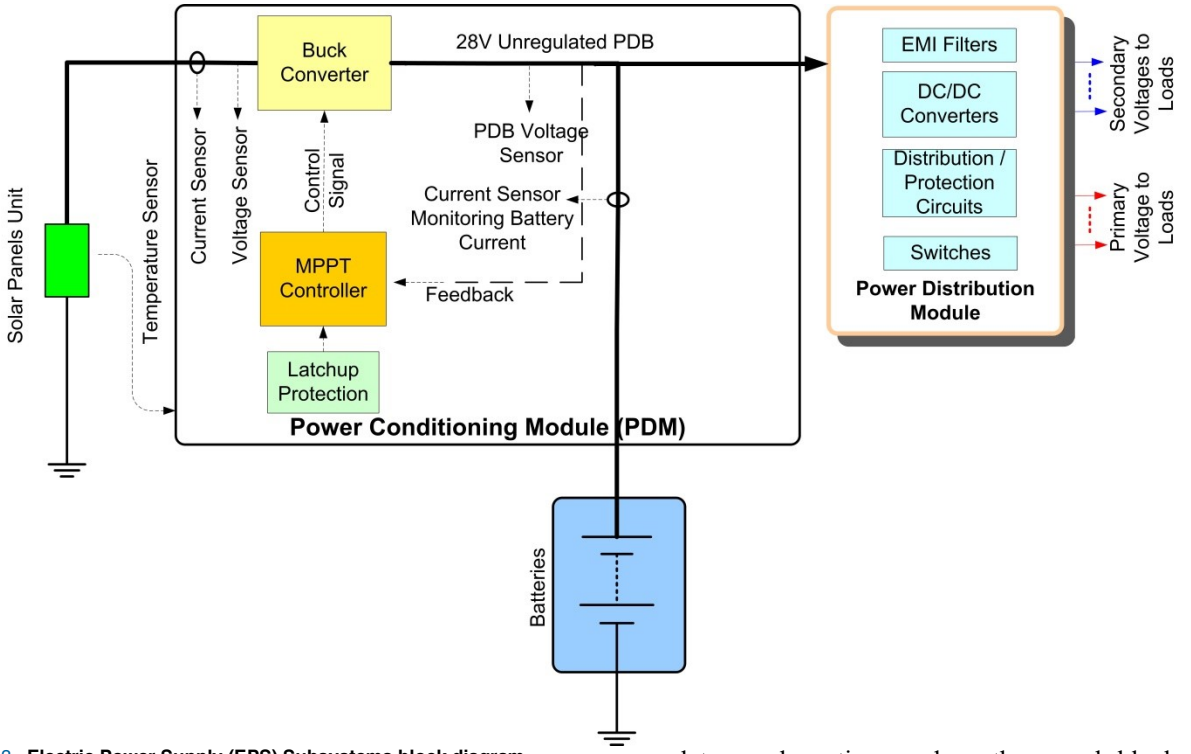

FIGURE 3. **Electric Power Supply (EPS) Subsystems block diagram**

II. MODULAR DESIGN APPROACH

The overall modular architecture design approach has been adopted for the PDM design which has made it more reusable, reconfigurable, and easily upgradable to more advanced forms [15]. The PDM unit has two fold modularity, first at unit level having uniform dimensions, mounting holes, and input/output ports (IO ports) where standardized D-type connectors are used for power and data signals. If the PDM needs to be replaced with an upgraded version, the dimension, mounting holes, the IO ports, and connectors will remain the same. Therefore, the modification/replacement will not affect rest of the satellite modules. The PDM unit printed circuit board (PCB) and its dimensions are shown in Figure 4, which reflects the PDM modularity at unit level. Second, on the schematic level, the main schematic as shown in Figure 5, is subdivided into several small blocks and sub-blocks. This technique helps in a way that several instances of the same schematic can be used multiple times. An easy schematic level upgrade is possible for the complete system by replacing only schematic sub-block with newer modified versions. It also enables schematic level fault tracing and makes hardware debugging more convenient. In a nutshell, it assists in developing a library with numerous schematic blocks and sub-blocks that could be reused for other space missions.

For understanding purposes, the schematic of the PDM controller block is shown Figure 6. Figure 5 shows that an instant of this block is used in main schematic. It can be replaced by a more updated PDU block as per need or mission requirement without modifying/ disturbing complete schematic and other sub-blocks and corresponding signals. Another advantage of this technique is that same schematic block can be reused (even multiple times) for other projects or units as well. Comparing modular schematic design technique in Figure 5 with conventional design of the same unit as shown in Figure 19, reveals that advantages of using the prior in terms of complexity, trouble tracing, hardware debugging/ troubleshooting and reusability.

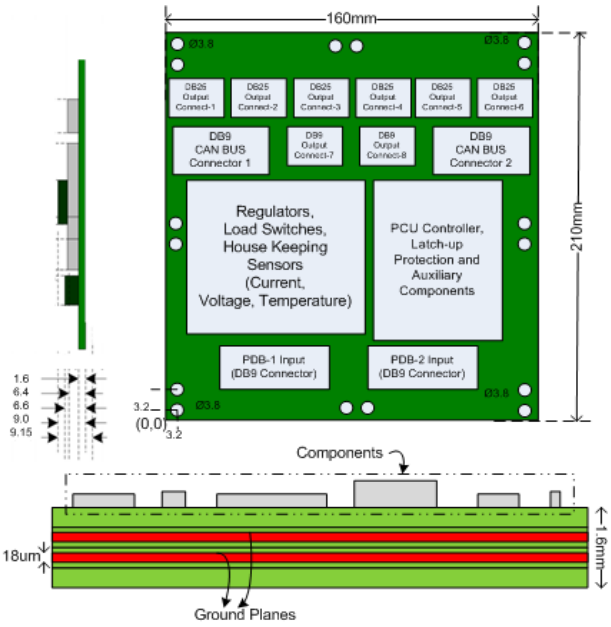

FIGURE 4. **PDM modularity at unit level.**

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2020.3020865, IEEE Access

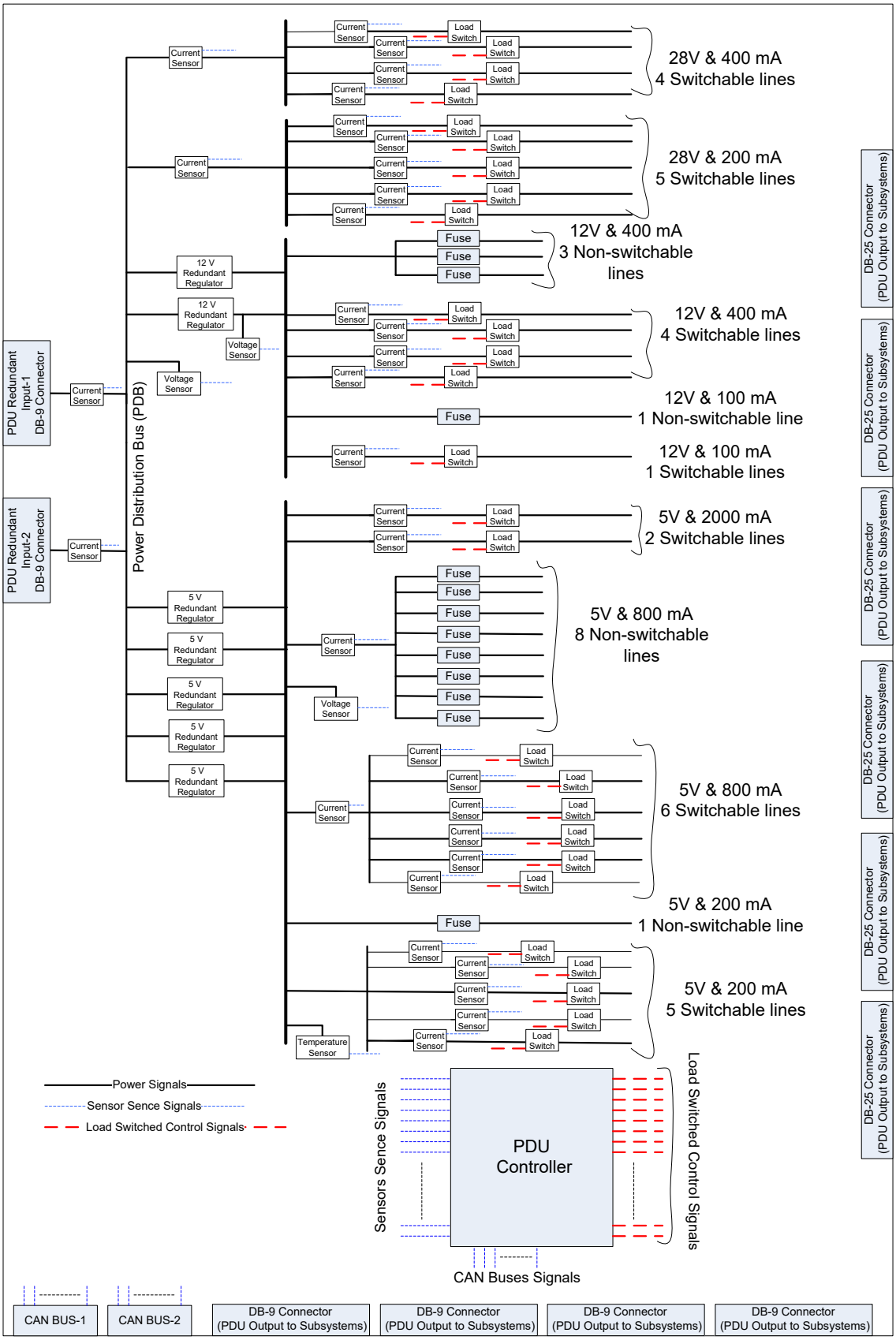

Figure 5. **PDM block diagram**

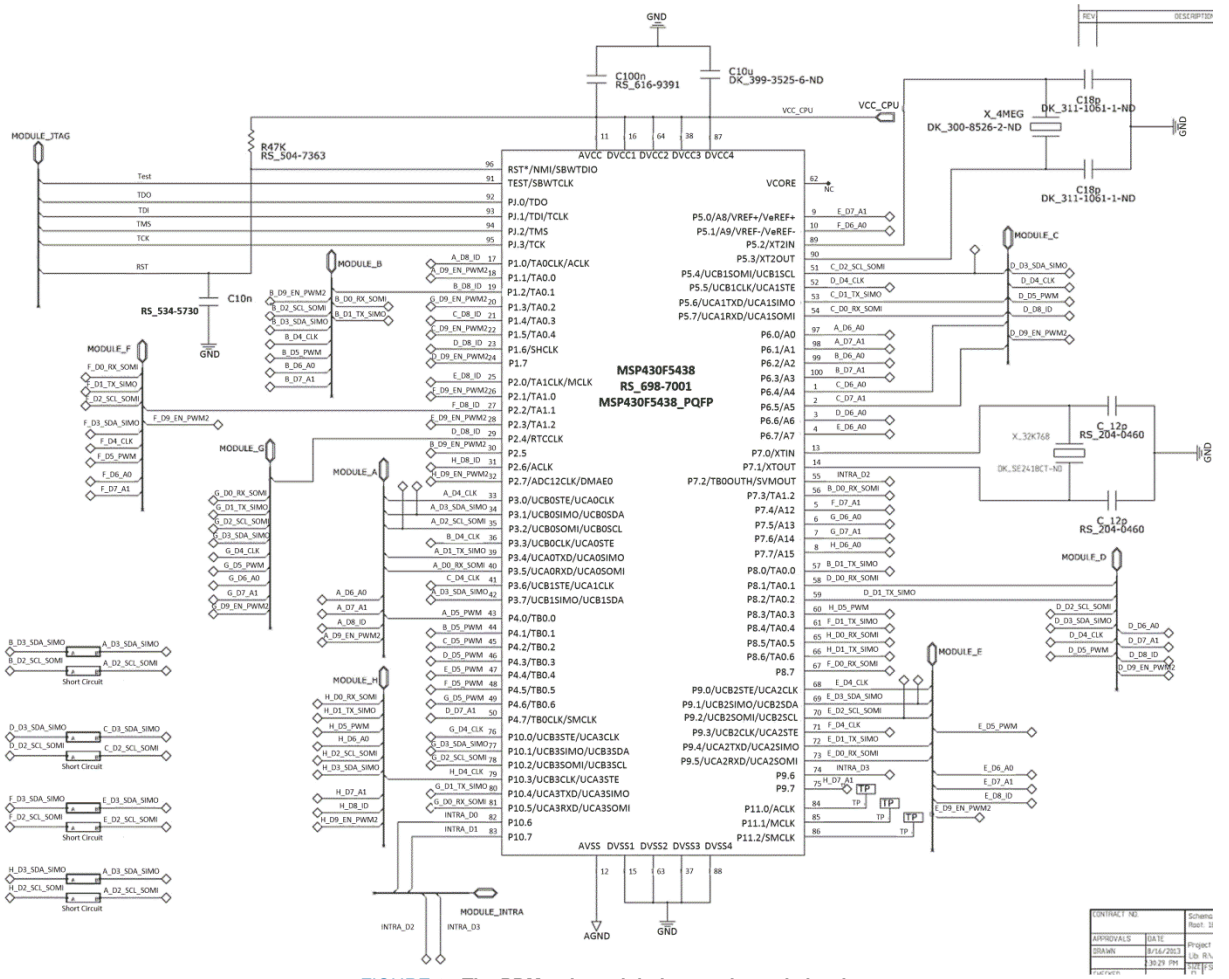

FIGURE 6. **The PDM unit modularity at schematic level**

III. PDM DESIGN

PDM is the sub-module of EPS which converts the PDB voltage level into the secondary voltage levels and distributes them to loads as per their requirements. PDM has various housekeeping sensors i.e. temperature sensor, Current and voltage sensors to observe and monitor its proper operation. PDM controller connects with the PNSS-1 OBC through redundant CAN buses. PDM gets input power from PCU at bus voltage 28V±6V (unregulated) and provides regulated output voltage levels at +12V and +5V. The PDM output power distribution lines have short circuit and over-current protection. Figure 5 shows block diagram of the PDM unit where each block can be treated as a specific instant and can be replaced in the diagram with an updated one.

A. PDM INTERFACES

All the electrical interfaces i.e. power inputs and outputs, telemetries (TM), telecommands (TC) and two redundant CAN buses of the PDM are summarized in pictorial form as shown in Figure 7.

1) INPUT POWER INTERFACES

PDM is receiving two redundant power inputs from the PCM's PDB. The PDB has 28±6V unregulated voltage level, which is converted into various regulated voltage levels by the PDM. On the redundant input lines from PCM, there are two current sensors (one on each line) and one voltage sensor for monitoring the current drawn by the PDM unit and the voltage level of the PDB, respectively. One of the 28V redundant power input line schematic is shown in Figure 7.

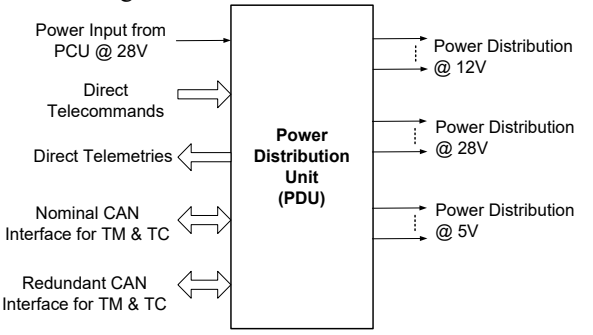

Figure 7. **Block diagram of PDM interfaces**

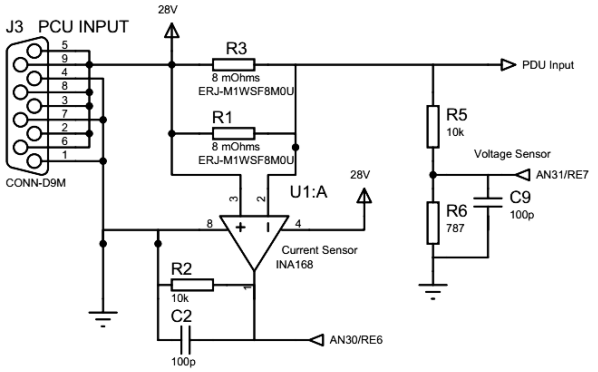

Figure 8. **28V power input to PDM from PCM**

INA168 [16] is used as a current sensor as shown in Figure 8. It has wide-range input voltage (2.7V ~ 60V), draw minute quiescent current and very small packaging (i.e. SOT23) which is perfect for space applications. Alternative choices can be CR5200 [17] series current sensors based on Hall Effect technology and can sense DC current upto 150A. These sensors have large size, heavy weight and are very expensive which make them incompatible with PDM module.

The differential input voltage across the redundant sense resistors (R1 and R3) on the input pins (PIN3 and PIN2) is converted to a current output. Here the redundancy in the shape of double input power lines and two parallel sense resistors has great significance, because the current for all of the PNSS-1 subsystems passes through these resistors and their failure can result in the loss of power to all subsystems. Therefore two input power lines with double redundant resistors reduce the failure chances four times. The INA168 current output is converted back to voltage through an external load resistor (*R2*). The current sensor conversion of the current signal into output voltage signal is can be understood by (1);

$$\text{Where;} \quad I_o = g_m(V_{3+} - V_{2-}) \qquad g_m = 200\mu A/V \qquad V_{OUT} = (I_s)(R_{sense})(g_m)(R_{Laod}) \tag{1}$$

Here I_o is the output current, g_m is the trans-conductance of the amplifier (INA168), R_{sense} is the sense resistor (*R1/R3*), I_S is the sense current flowing through R_{sense}, V_{3+} and V_{2-} are the sense resistor input and output voltages, R_{Load} is the load resistor (*R2*) and V_{OUT} is the output voltage (across capacitor *C2*). The INA168 current sensor, actually converts the sense current into corresponding output voltage range, fed to the PDM controller. The load resistor is a voltage divider which value is calculated such that it converts the sense voltage into the PDM controller input voltage range i.e. 0V ~ 2.5V (maximum input voltage limit is 3.9V, where a fraction voltage above the limit will permanently damage the controller).

The voltage sensor shown in Figure 8, is a simple voltage divider that consists of resistors *R5* and *R6* which senses PDB voltage and converts it to PDM controller input voltage range. The maximum voltage on PDB is 34V (28±6V). To be on the safe side, the maximum input voltage to PDM controller should not be greater than 2.5V, therefore the resistors values of *R5* and *R6* are chosen accordingly.

By observing current and voltage sensors schematics from the output side, there behavior is similar to a low pass filters. In case of current sensor, the sampling frequency (f_{samp}) is set by the values of *C2* and *R2*, while in case of voltage sensor f_{samp} is dependent on *C9* and *R6* values. In order to avoid aliasing, the criteria given in (2) should be satisfied;

$$f_{samp} \geq 2\frac{1}{2\pi \times C58 \times R184} \tag{2}$$

2) OUTPUT POWER INTERFACES

PDM is providing various voltage levels (28V, 12V and 5V) to the PNSS-1 subsystems. There are nine power lines which feed 28V directly to the satellite subsystems. Out of these nine 28V lines, four switchable lines have 400mA current rating while five switchable lines have 200mA current rating. The PDM primary and secondary output power (switchable and non-switchable lines) along with their required voltage and current specifications are shown in table 1.

TABLE 1
PDM SWITCHABLE AND NON-SWITCHABLE OUTPUT POWER LINES

S. No	Voltage Level	Power lines and their current rating	Switchable/ Non-Switchable
1	28V	4 Lines @ 400mA each	Switchable
2	28V	5 Lines @ 200mA each	Switchable
3	12V	3 Lines @ 400mA each	Non-Switchable
4	12V	4 Lines @ 400mA each	Switchable*
5	12V	1 Line @ 100mA each	Switchable
6	12V	1 Line @ 100mA each	Non-Switchable
7	5V	2 Lines @ 2000mA each	Switchable
6	5V	8 Lines @ 800mA each	Non-Switchable
7	5V	6 Lines @ 800mA each	Switchable
8	5V	5 Line @ 200mA each	Switchable
8	5V	1 Line @ 200mA each	Non-Switchable

Standard D-type connectors are employed for all input and output interfaces. Each power line (primary as well as secondary) of the PDM have a separate wired return line. Positive power lines and their returns have a gap of at least one unused pin in all interface connectors to mitigate cross talk and interference. In the PDM design, a total of six DB25 and three DB9 connectors are used to interface the PDM switchable and non-switchable outputs (28V, 12V and 5V) to the satellite subsystems.

To avoid accidental wrong connections, all the output connectors of the PDM are female type while the input connectors are male type. The primary power input leads is kept isolated from the unit housing by a DC resistance of 1MΩ. Similarly the signal and secondary power circuits are kept isolated from the primary power leads by a minimum DC resistance of 1MΩ.

3) INDIRECT TELE-METRIES &TELE-COMMAND (TMTC) INTERFACE

PDM has a dual redundant CAN interface with OBC for all telemetries (TM) and telecommands (TC) signals. Some of these TMTC signals are forwarded to OBC through PDM controller and is called indirect TMTC interface. PDM provides sufficient telemetries (through CAN interface) to OBC in order to monitor ON/OFF status for its switchable distribution lines as well as health of primary and secondary buses during all mission phases. The PDM receives telecommands (through CAN interface) in order to govern the ON/OFF operation of its switchable power lines (or satellite loads) throughout the mission. Telemetries of PDM include the following:

i. Two Current Sensors on the redundant PDB input lines
ii. 4 current sensors on 4 Lines @ 400mA
iii. 5 current sensors on 5 Lines @ 200mA
iv. 3 current sensors on 3 Lines @ 400mA
v. 4 current sensors on 4 Lines @ 400mA
vi. 1 current sensors on 1 Line @ 100mA
vii. 1 current sensors on 1 Line @ 100mA
viii. 2 current sensors on 2 Lines @ 2000mA
ix. 8 current sensors on 8 Lines @ 800mA
x. 6 current sensors on 6 Lines @ 800mA
xi. 1 current sensors on 1 Line @ 200mA
xii. 5 current sensors on 5 Lines @ 200mA
xiii. 1 voltage sensor on 12V voltage line
xiv. 1 voltage sensor on 5V voltage line
xv. 1 current sensor to measure total current at 12V line
xvi. 1 current sensor to measure total current at 5V line
xvii. ON/OFF status of all switches

All the above telemetries are communicated with the OBC through the PDM controller.

4) DIRECT TMTC INTERFACE

PDM also has a direct/dedicated telecommand interface with OBC for switching ON/OFF all its switchable distribution lines called direct TMTC interface for redundancy purposes. The direct telemetries of PDM include both bi-level and analog as defined below.

For Bi-Level Telemetry: Low (0) Voltage : 0V
High (1) Voltage : 5V

In case of Analog Telemetry Range: 0 to 5V

The direct telecommand interface specifications are as follows:

Low (0) Level : 0 to 0.2V
High (1) Level : 11V ± 1V

In case of direct telemetries and telecommands, multiple telemetries and telecommands share a common return/ground interface for TM and TC signals. However, in that case, the return wire is 2:1 redundant in order to avoid single point failure.

5) CAN BUS INTERFACE

PDM communicate with OBC through Controller Area Network (CAN) buses. Parallel access architecture with two separate CAN controllers for each CAN bus is used [18, 19]. It means that the CAN controller/processor have two CAN channels for separate dual redundant CAN operations. Figure 9 shows the block diagram of the CAN redundant buses. Here, the PDM microcontroller is connected to two redundant CAN bus controllers through SPI interface. The two redundant CAN bus controllers are connected with CAN bus transceivers. Single channel CAN bus is shown in Figure 10. The bus is composed of two integrated circuits (ICs) MCP2515 [19] and SN65HVD230D [18]. MCP2515 is CAN controller that can transmit and receive both normal and extended data remote frames. The MCP2515 has two acceptance masks along with six acceptance filters used for filtering the unwanted messages. In this way MCP2515 reduces the main PDM controller burden. The SN65HVD230 CAN is capable of data rates up to 1 megabit per second (Mbps), and ensures CAN network robustness by providing many safety features. The SN65HVD230 transceiver is compatible with the Texas Instruments MCP2515 CAN controller [19].

The MCP2515 interfaces with PDM microcontrollers via an industry standard Serial Peripheral Interface (SPI) having signals *SO* (slave out), *CS* (chip select), *SI* (slave in) and *SCK* (serial clock). Data and command signals are received by the MCP2515 on its *SI* pin, with the rising edge of the *SCK* clock pulse while data is sent to the PDM controller by the MCP2515 (on the *SO* line) on the falling edge of *SCK*. The *CS* pin is kept low data transmission. MCP2515 transmit and receive data from the CAN transceiver through *TXCAN* and *RXCAN* respectively. On a reset pulse, the MCP2515 keeps its logic and registers in default state, after every power-up. In Figure 10, a hardware reset is achieved automatically by mounting an RC network of 10kΩ resistor and 200pF capacitor on the *RESET* pin, result in 2µs reset time [19].

The SN65HVD230 can be operated into three different modes: high speed, slope control, and low-power. The high speed mode is achieved when RS pin is directly grounded, which switches ON/OFF the transmitter output transistor very fast with no control on the rise and fall slopes. In order to adjust the rise and fall slopes, a resistor is connected between the RS pin and ground. Connection of a 10 kΩ resistor, result in a signal with rise and fall edge slew rate of ~15 V/µs while a 100 kΩ provides a slew rate of ~2.0 V/µs. In PDM CAN a 10 kΩ resistor is connected on the RS pin with a slew rate of ~15 V/µs. As the resistor value increases, the slew rate decreases and results in reduction of the electromagnetic interference (EMI) produced by the rise and fall times of the driver and resulting harmonics. In order to prevent signal reflections on the CAN bus, a resistor of 120 Ω, equal to the characteristic impedance (Z_O) of the line is connected to terminate both ends of the cable [18].

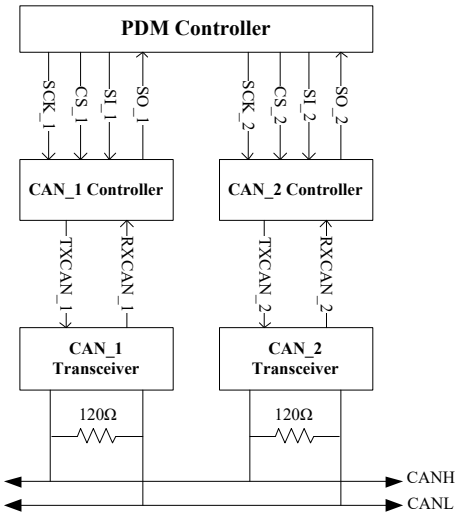

Figure 9. **Block diagram of the CAN redundant buses**

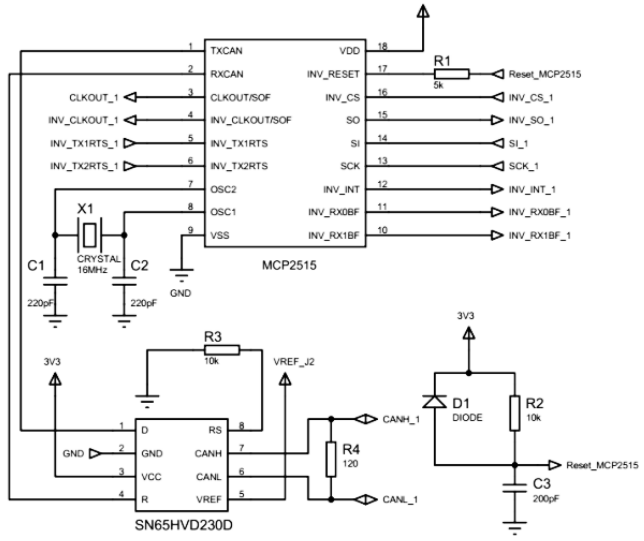

Figure 10. **CAN Bus interface schematic**

B. POWER REGULATORS

PDM receive primary power from PCM with power distribution bus (PDB) voltage level of 28V ± 6V (unregulated) and generates regulated secondary voltage levels at +12V and +5V. In order to convert the PDB voltage level to the required voltage levels, the PDM uses two redundant switchable power regulators to convert the PBD voltage to the required voltage levels.

Texas Instruments 5A adjustable regulator LM2679 [20] is used for providing 5V as well as 12V from PDM to the PNSS-1 subsystems. The LM2679 is capable of driving up to 5A loads with excellent line and load regulation characteristics. The LM2679 converter is a highly efficient step down switching regulator of wide input range (8V ~ 40V) with a switching frequency of 260 kHz and operating temperature from -40 to 125 °C. Efficiency greater than 90% is obtained by using low ON resistance DMOS power switch. The series consists of fixed output voltages (i.e. 3.3 V, 5 V, and 12 V) and adjustable output voltages. Other features include the ability to power on by adding a timing capacitor to gradually turn on the regulator. The LM2679 series has soft-start ability reducing the input surge current, built-in thermal shutdown and resistor programmable current limit to protect the device and load circuitry under fault conditions. There is very insignificant effect on the efficiency (still above 90%) during high load current and/or high input voltage conditions, as shown in Figure 11 and Figure 12 respectively. The device has excellent line regulation and even with input voltage variation from 10V ~ 40V, the output voltage remain almost constant with just 0.1% change as shown in Figure 13.

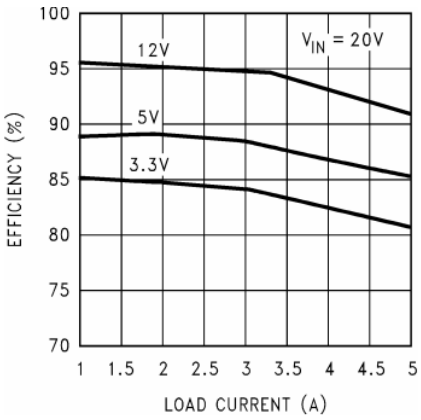

Figure 11. **Load current versus efficiency [20]**

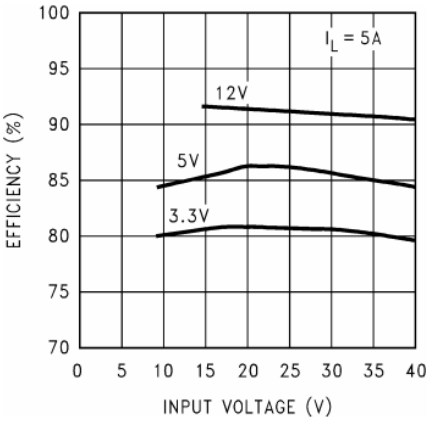

Figure 12. **Input voltage versus efficiency [20]**

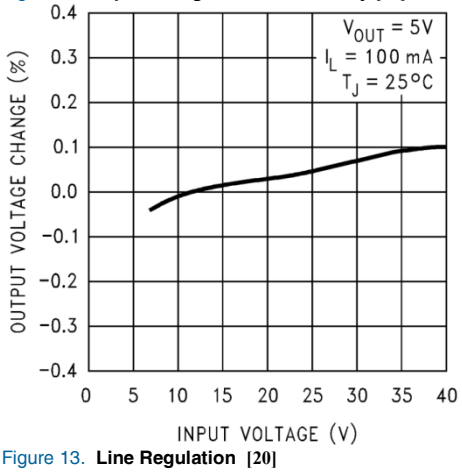

Figure 13. **Line Regulation [20]**

1) 5V REGUALTORS

On the 5V power bus, there are thirteen switchable and nine non-switchable lines with a total maximum current rating of 16400mA. In order to meet the PNSS-1 specification constraint and current requirement on the 5V regulated line, four LM2679S-ADJ [20] 5V redundant regulators are used. In order to make the LM2679S-ADJ compatible with the required specifications of V_{in} = 28V, I_{load} = 3.5A and V_{out} = 5V. The resistors ratio with respect to output and feedback voltages is given by (3);

$$V_{out} = V_{FB}\left(1 + \frac{R_{36}}{R_{41}}\right) \tag{3}$$

Where, V_{FB} represents the feedback voltage with a typical value of 1.21V. Suppose *R41* is 1kΩ, then from (3) *R36* is 3.2kΩ. This results in an output voltage (V_{out}) of 5.08V which is within 0.5% of the target value.

The inductor value from Figure 14, can be found from the calculation of the inductor Volt • microsecond constant (E • T expressed in V • µS) as given in (4);

$$E.T = \left(V_{IN(max)} - V_{out} - V_{sat}\right).$$

$$\frac{V_{out}+V_D}{V_{IN(max)}-V_{sat}+V_D} \cdot \frac{1000}{260}(V.\mu s) \tag{4}$$

Where, V_{SAT} is the voltage drop across the internal power switch which is $R_{ds(ON)}$ times I_{LOAD}. In the 5V regulator case, V_{SAT} is typically 0.12 Ω × 3.5 A or 0.42 V and V_D is the voltage drop across the forward biased Schottky diode, typically 0.5V. By inserting $V_{IN(max)}$ = 28V, V_{out} = 5V and other parameters values in (4), results in E.T = 18V.µs. In Figure 14, the intersection of 18V.µs horizontally and the 3.5A of I_{load} vertical line indicates that *L40*, a 33µH inductor could be used for the reference designator *L1* in Figure 15. Similarly, a Schottky diode with part number MBRD1545CT, 0.01µF *C11* capacitor, 33µF *C6* and *C10* capacitors while a 7.15kΩ *R42* resistor is used according to the 5V regulator requirement, using the datasheet given in [20].

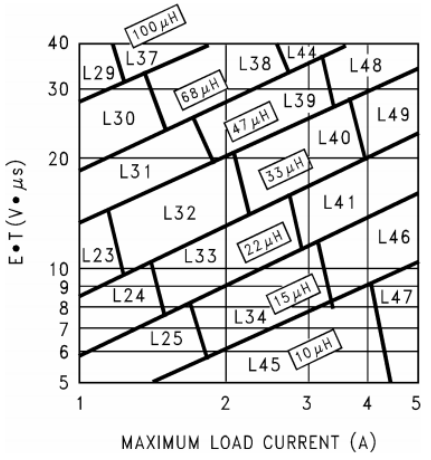

Figure 14. **Adjustable voltage [20]**

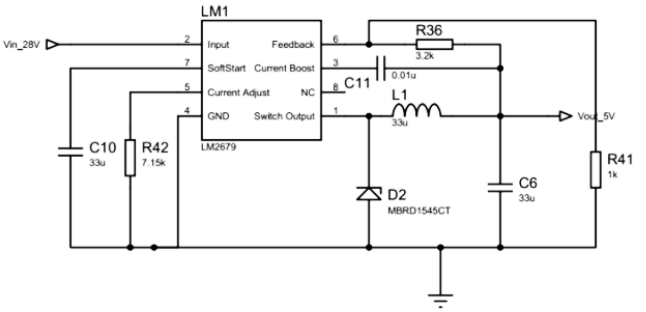

Figure 15. **Converter circuit design diagram**

2) 12V REGUALTORS

The total current requirement on the 12V line of the PDM unit is 3000mA as shown in table 1. The two redundant regulators LM2679S-ADJ [20] connected in parallel can provide upto 7A load current on the 12V line of the PDM unit. The 12V regulator converter circuit design steps are similar to the 5V regulator except the 5V V_{out} is replaced with 12V.

C. PDM CONTROLLER

PDM controller is the heart of PDM unit and is mainly responsible for controlling and managing the system, in particular:

- Processing data and resources of the PDM unit
- Communication of the PDM unit with OBC through redundant CAN buses
- Power management and power scheduling task
- Storing and processing housekeeping data
- Decoding and executing PDM unit commands

A commercial Texas Instruments (TI) MSP430F5438A [21] is used as PDM controller which is an ultra-low power 16-Bit RISC architecture microcontroller. It can support up to 25MHz system clock. The MSP430F5438A has a total of seven low power modes: one active and six software selectable modes. The device is activated from low power modes on an interrupt event, the device deal the request, and return back to low-power mode. MSP430F5438A is an eight ports microcontroller as shown in Figure 16. On each port a subsystem of PDM unit is connected. The controller also has a J-Tag connector for programming and debugging purpose. A single port of the PDM controller has digital I/O, analog and communication signals as shown in table 2.

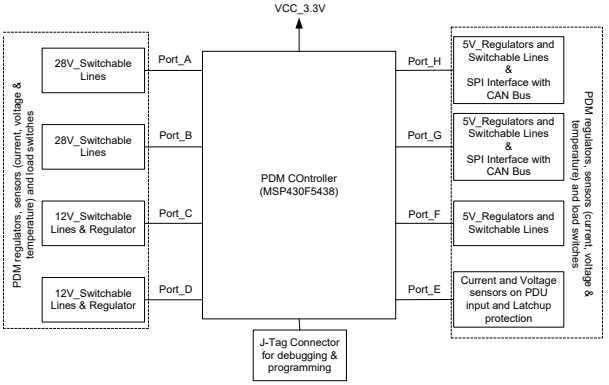

Figure 16. **PDM unit architecture with respect to controller**

TABLE 2
PDM CONTROLLER SINGLE PORT SIGNALS

D0_RX_ SOMI	D1_TX_ SIMO	D2_SCL_ SOMI	D3_SDA_ SIMO	D4_CLK
D5_PWM	D6_A0	D7_A1	D8_ID	D9_EN_ PWM2

D. SWITCHABLE POWER LINES

PDM unit has a total of 27 switchable power outputs on 28V, 12V and 5V power lines. Each switchable power output is the combination of a current sensor and a load switch. A current sensor monitors the current of the respective output and intimates the PDM controller. In case of any anomaly, the PDM controller isolates that power line through a control signal to the respective power switch. A combination of the current sensor and load switch used in all the switchable power outputs is shown in Figure 17.

The current sensor design details are already discussed in section IIIA(1) with title input power interfaces. The load switch function is to supply and cutoff power from the other subsystem by the enable signal from the PDM controller in response to current sensor signal.

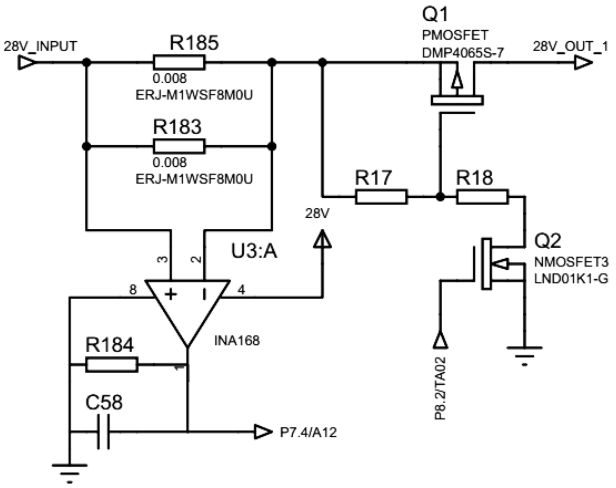

Figure 17. **Basic circuit connections of INA168**

E. LATCH UP PROTECTION

Space is a radioactive environment and has different types of radiation effects on the aerospace systems [22, 23]. PDM controller is CMOS based COTS device which is prone to radiation in space environment [22, 23]. With respect to system design, these effects can be divided into hardware and software effects. The hardware effects are classified into three main classes i.e. displacement damage (DD), total ionization dose (TID), and single event effects (SEE). SEE is further categorized into single event gate rupture (SEGR), single event functional interrupt (SEFI), single event latchup (SEL), and single event burnout (SEB) [24, 25]. TID and DD are delayed effects that damage the system after a specific dose limit and lifespan. Among the single event effects the most frequent and hazardous is the SEL. Latch is a temporary effect in which the device is short-circuited between power supply and ground resulting in high current flow and damages the device. The solution to latch-up is to avoid CMOS and use bipolar devices, that are resistant to latch-up and require high energy to initiate SEL. Totally avoiding CMOS devices is impossible because microcontrollers and microprocessors are CMOS based, used on spacecraft for data processing and control. Alternative solution is to use SEL hardened CMOS microcontrollers [26].

In order to make the PDM controller radiation hardened against SEL, a latch-up protection circuit was designed and simulated as shown in Figure 18 (a). This circuit disconnects the PDM controller supply voltage (V_{CC}) and avoids high current flow through the device. In Figure 18 (a), *V4* is connected to V_{CC} pin through MOSFET *M1* (PMOS) and *M2* (NMOS) switching. One leg of capacitor *C1* is connected to node A while its other leg is connected to microcontroller pin, here represented with voltage supply *V3*. Normally, *M2* is ON through *C1*, which is fully charged from supply *V2* through resistor R4. It further keeps ON *M1*, and voltage supply *V4* is connected with microcontroller V_{CC} pin. The resultant waveform is shown Figure 18 (b). The waveforms at node *A* and node *B* shows the voltages across *C1* and microcontroller V_{CC} respectively.

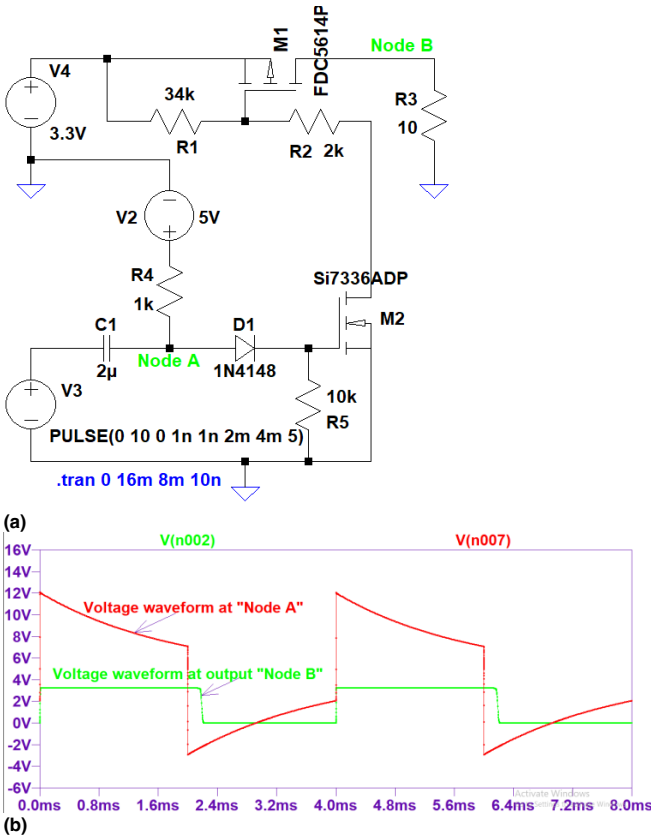

Figure 18. **(a) Basic simulation circuit of Latch up protection (b) waveform**

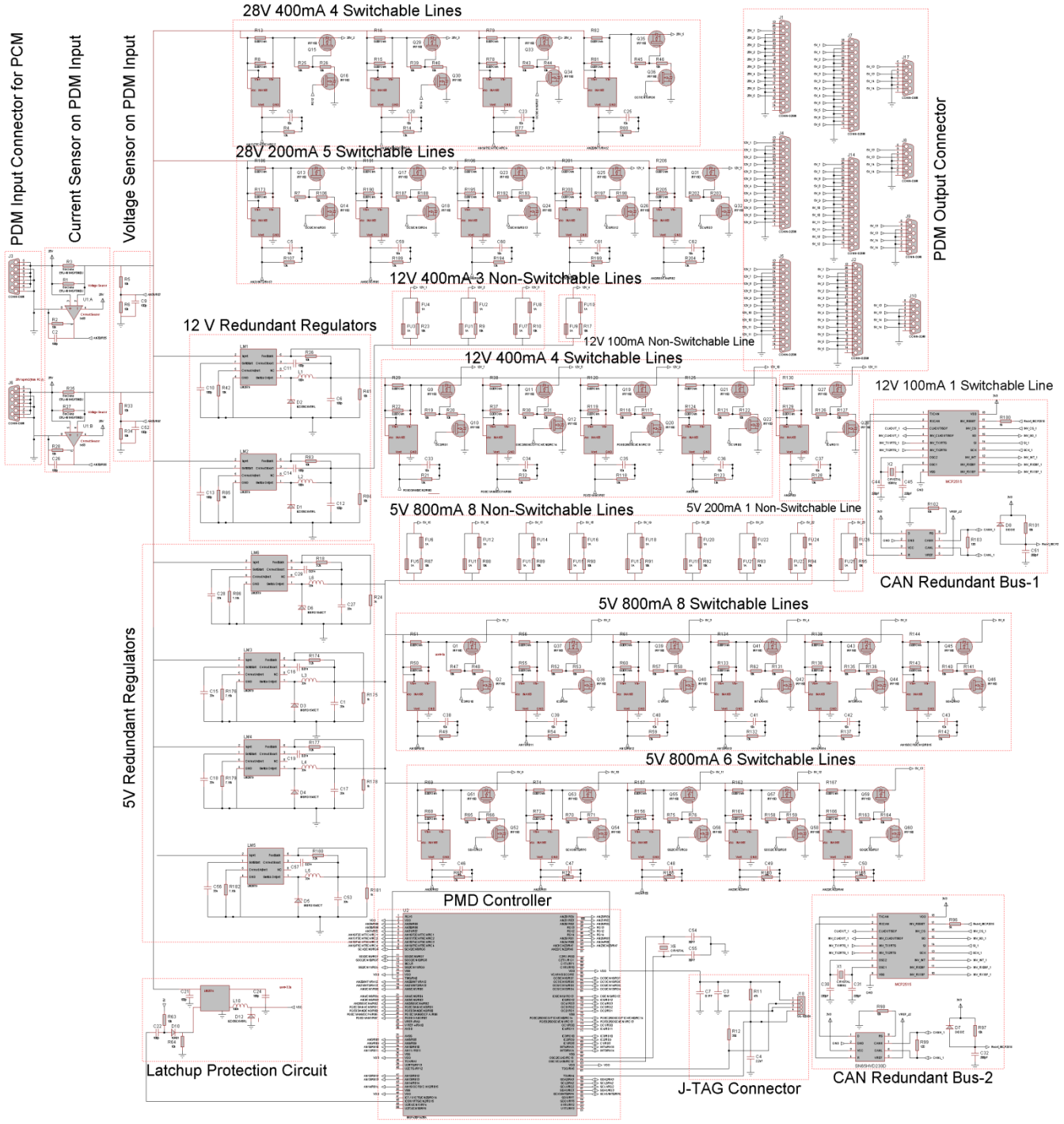

Figure 19. **PDM unit complete schematic**

Normal operating conditions are shown in Figure 18 (b) between time slots 0 ~ 2ms and 4 ~ 6ms. In case of latch-up, the PDM controller pin here represented by *V3*, will connect to ground and the capacitor *C1* will discharge. As a consequence, *M2* and *M1* switches will turn off and cut off voltage supply to PDM controller V_{CC} pin. The PDM controller supply disconnected state is depicted in Figure 18 (b) between time slots 2 ~ 4 ms and 6 ~ 8 ms. Resistor *R1* and capacitor *C4* values decides the off time. Here *RC* time constant chosen is 2ms.

The complete (conventional) schematic of the PDM unit is shown in Figure 19 for comparison purpose with modular schematic approach as discussed earlier. It is far complex, hard to troubleshoot or to trace faults. It is also not that convenient to upgrade the same as modifying any component without careful execution can disturb the complete schematic. Furthermore, reuse/ customization of same for future missions is comparatively less convenient.

IV. PDM THERMAL MODEL

The small satellites onboard electronic components receive almost ten times greater solar power as compared to terrestrial solar exposed electronic systems, because in aerospace there is no season or atmospheric attenuation of sunlight [27]. In space, heat transfers through radiation and conduction, there is no convection [28]. Therefore, the spacecraft body directly exposed to solar radiations has higher temperature as compared to the opposite side in dark (very low temperature). The temperature delta between the opposite spacecraft fronts depend on the satellite structure thermal resistance. Structure material with high thermal resistance block heat flow from hot to cool face which result in heat trapping inside the spacecraft and further increase subsystem temperature. The high temperature worsens the performance and reduces the lifetime of the components. Thermal resistance is dependent upon the material used and their dimensions. In this section, thermal resistance of the PDM module is calculated through electrical and mathematical thermal models and it elaborates the fact that how thermal resistance of a specific module of the satellite varies with dimension and material used for that subsystem.

In thermal domain, Ohm's law [29] is given by (5).

$$\Delta T = P.\theta_{th} \tag{5}$$

Where ΔT is the difference of temperature across a material, P is the heat power absorbed and θ_{th} is the thermal resistance that can be found using the Fourier's Law for heat conduction [30].

Thermal model of a system can be achieved as a combination of thermal capacitors and thermal resistances [31]. Consider an object that consists of N-materials stacked together as shown in Figure 20(a). It can be represented by two thermal models i.e transient thermal model given in Figure 20(b) and steady state thermal models depicted in Figure 20 (c), where the temperature difference between top surface (*material_1*) and bottom side (*material_N*) is ΔT. *T_material_1* is the upper side temperature of *material_1, T_material_N* is the bottom side temperature of *material_N*, *material_1* thermal resistance is represented by θ*_material_1*, *material_2* thermal resistance is represented by θ*_material_2*, *material_3* thermal resistance is represented by θ*_material_3*, *material_N* thermal resistance is represented by θ*_material_N*. Similarly *C_material_1* represents the thermal capacitance of material_1, *C_material_2* depicts the thermal capacitance of *material_2*, *C_material_3* portrays the thermal capacitance of *material_3* while *material_N* thermal capacitance is denoted by *C_material_N*.

Transient thermal model consists of thermal resistances and thermal capacitances related with the body materials of the object as shown in Figure 20(b). In steady state model, when power and temperature achieve stable levels, means that the thermal capacitors are now fully charged (play no role in the model) and can be ignored from the thermal model as shown in Figure 20(c). The PNSS-1 satellite with PDM unit is shown in Figure 21. Let the solar radiations are impinging on face A. A portion of the solar power is reflected back and the remaining power is absorbed by the panel. Some of the absorbed solar power will convert into useful electrical energy through solar cells and the remaining power is absorbed by the satellite subsystems as heat energy.

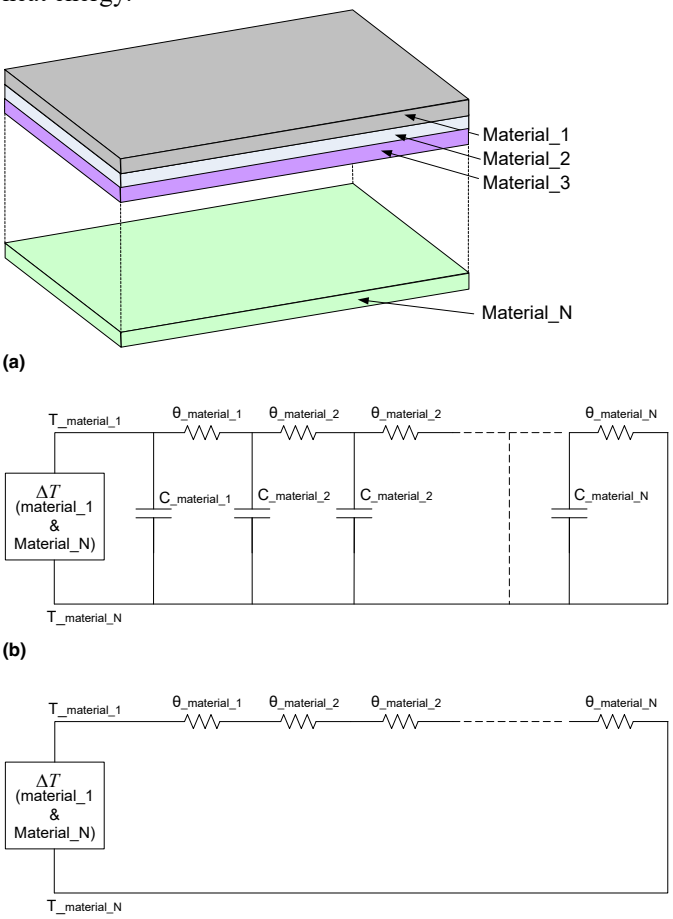

Figure 20: **(a) Object composed of N materials (b) Transient thermal model (c) Steady state thermal model**

If the subsystem modules have high thermal resistance to heat flow from hotter side (face A) toward the cooler side (face B), most of the absorbed heat will be trapped inside the satellite and will result in increased subsystem temperature. As a consequence the temperature may increase above the threshold of certain components and damaged them permanently. In order to avoid this destructive phenomenon a thermal model of the system is needed at design stage in order to ensure thermal reliability of the developed subsystem. Here, the model of Figure 20 is applied on the PDM unit and total thermal resistance of the unit is calculated.

The cross sectional view of the PDM unit and the corresponding thermal model from face A to face B are shown in Figure 22(a) and Figure 22(b) respectively. The PDM unit is basically composed of four layers made of *FR4* material and copper traces. The components are attached on layer 1. The layers 1 & 2 have copper traces

used for components interconnection. These two layers (1 & 2) may have different numbers of copper traces of certain dimensions. Layers 3 & 4 have the ground planes embedded inside FR4 material.

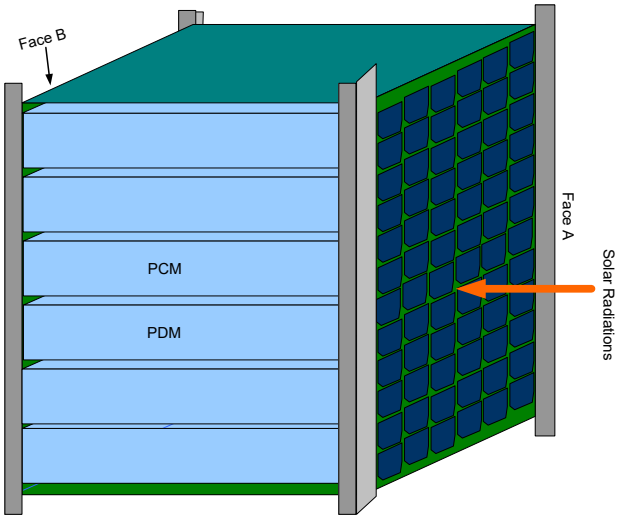

Figure 21. **PNSS-1 with PDM unit**

In order to get the required thermal model, the panel has been divided with respect to the number of layers. Each layer has two type of materials i.e. FR4 and copper having their associated thermal resistances, as depicted in Figure 22(a) and Figure 22(b). In this model θ represents thermal resistance, F represents FR4 material, L with numbers (1, 2, 3, 4) shows the respective layer, c represents centre of the layer, BE depicts bottom edge while TE denotes top edge of the layer. In layers 3 & 4, the FR4 material and copper material ground planes are in parallel therefore there resultant resistances are also in parallel as shown in the thermal model of Figure 22(b). In layers 1 & 2, the resistances associated with the FR4 material on the edges are in series with the parallel combination of the *FR4* and copper traces resistances in the centre.

The equivalent thermal resistance *(θ_{eq})* of the PDM unit thermal model of Figure 22(b) is written in mathematical form as given in (6);

$$\theta_{eq} = \left(\theta_{F\_L1\_BE} + \theta_{F\_L1\_C} // \theta_{Cu\_L1\_C} + \theta_{F\_L1\_TE}\right) // \left(\theta_{F\_L2\_BE} + \theta_{F\_L2\_C} // \theta_{Cu\_L2\_C} + \theta_{F\_L2\_TE}\right) // \left(\theta_{F\_L3\_C} // \theta_{Cu\_L3\_C} // \theta_{F\_L4\_C} // \theta_{Cu\_L4\_C}\right) \quad (6)$$

The value of the thermal resistance depends on the length, width and material type of the portion of the respective layer. After inserting the individual resistors values into (6), the θ_{eq} value of the PDM unit is found which is *2.1K/W*.

PNSS-1 have around six similar modules like PDM connected in parallel from face A to opposite face B. Suppose all the modules have same thermal resistance i.e. *2.1K/W*. The seven resistances connected in parallel will result in the equivalent resistance equal to (*2.1/7=*) *0.3K/W*.

The solar power intensity in LEO orbit is about *1365 W/m*^{2}. In case of PNSS-1, with solar panel dimensions *450* $\times$ *450 mm*^{2} absorbs a total solar power of *276W*. Let solar power is impinging on single solar panel with an efficiency of *28%*. It means that solar panel converts the *28%* power (*77W*) to electrical output and the remaining *72% (199W)* wasted power (*P*) is delivered to the satellite subsystems. The temperature difference (ΔT) between the satellite face exposed to solar radiations and opposite face can be obtained by inserting *P* and θ_{eq} values into (5). The resultant ΔT value is (*199W*$\times$*0.3K/W=*) *59.7K*.

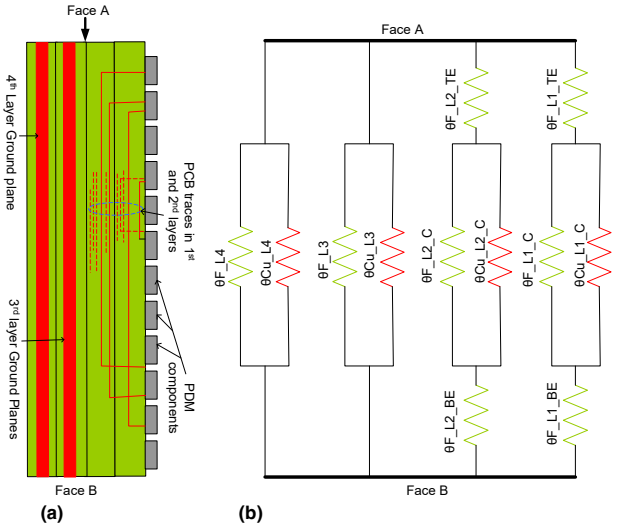

Figure 22. **Thermal model of the PDM**

V. COMPARATIVE ANALYSIS

The main feature of the PDM design discussed in this paper is modularity and redundancy at all levels and to avoid single component failure that may lead to mission failure. In this regard, redundancy and to some extent diversity is ensured at the input power lines, regulators, sensors, switches and output power lines. The Figure 8 and Figure 19 shows, the redundant sense resistors R1 and R3 on the input pins (PIN3 and PIN2) are laid out as double redundant input power lines. Using this layout is advantageous in comparison to single line layout as it reduce the chances of failure by four times. Whereas single line layout, incase of a fault can result in the loss of power to all the subsystems. Two redundant 28V unregulated power buses are provided by PDM to the satellite subsystems. Similarly, two redundant 12V regulators connected in parallel can provide a current of 7A to the satellite subsystems. In order to meet the PNSS-1 specification constraint and current requirement on the 5V regulated line, four 5V redundant regulators are used. Likewise, all the switchable and non-switchable PDM output power lines are redundant to ensure the availability of power to satellite subsystems. As CMOS components are prone to SEL in space environment, therefore to make the PDM controller radiation hardened against SEL, a latch-up protection circuit is designed.

Comparing the PDM discussed in this paper with other PDM designs available in the online literature, it has

several added advantages/ features. They lack the latch-up protection, which is a crucial part of the PDM microprocessor in the space radiation environment [32-36]. Most of the PDM [33-35] have no inlet power line redundancy which is very essential for reliable power delivery to PDM from the power conditioning module. Similarly, in most of the designs [34-36], two separate power regulators are used for 12V and 5V power buses, but instead of providing redundancy, they collectively meet the power requirement of the respective loads.

VI. CONCLUSION

In the paper a comprehensive design of the PDM unit of PNSS-1 satellite is presented. This modular design of the PDM unit is a fundamental step in designing PDM subsystems on a single PCB for micro and nanosatellites. It illustrates an innovative solution to resolve conflicting problems such as cost, weight and physical dimension. To implement such a large number of subsystems on single module is never a trivial job. Best suitable results have been achieved by proper selection of COTS devices with lower dimensions, cost and power consumption. In the first part of the paper, the detail design of the PDM subsystems is presented. PDM interfaces, power regulators, current and voltage sensors, PDM controller and redundant CAN buses are discussed in detail. A latchup protection circuit is designed for enabling use of CMOS COTS components in space. This innovative design not only reduces the overall cost and weight of the PDM unit but also delivers considerably compact design. Thus, provides enough space for more onboard subsystems. In the second part of the paper, a thermal model of the PDM unit has been presented. The thermal resistance of the PDM unit was measured by employing the presented thermal model. The resultant low thermal resistance ensures that the spacecraft can easily dissipate heat from hotter to cooler surface. The presented model and measurement techniques can be applied to various aerospace systems for thermal resistance measurement and ensuring their thermal stability.

The main constraints on small satellite subsystems development are budget, size and power consumption. Therefore, in future the focus will be to further reduce the PDM size and analyse it for its overall power consumption and development cost.

AUTHORS CONTRIBUTIONS

Anwar Ali: Conceptualization, Investigation, Formal analysis, methodology, writing original draft
Haider Ali: Investigation, Formal analysis, methodology, writing original draft
Jijun Tong: methodology, writing original draft
M. Rizwan Mughal: methodology, writing original draft, Writing – review & editing
Saeed Ur Rehman: Investigation, Writing – review & editing

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