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Decreasing Interface Defect Densities via Silicon Oxide Passivation at Temperatures Below 450°C

Zahra Jahanshah Rad,[†] Juha-Pekka Lehtiö,[†] Iris Mack,[§] Kawa Rosta,[§] Kexun Chen,[§] Ville Vähänissi,[§] Marko Punkkinen,[†] Risto Punkkinen,[‡] Hannu-Pekka Hedman,[‡] Andrei Pavlov,[†] Mikhail Kuzmin,[†,‖] Hele Savin,[§] Pekka Laukkanen,[,†] and Kalevi Kokko[†]*

† Department of Physics and Astronomy, University of Turku, FI-20014 Turku, Finland

§ Department of Electronics and Nanoengineering, Aalto University, FI-02150 Espoo, Finland

‡ Department of Future Technologies, University of Turku, FI-20014 Turku, Finland

‖ Ioffe Physical-Technical Institute, Russian Academy of Sciences, St. Petersburg 194021, Russian Federation

* email: pekka.laukkanen@utu.fi

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ABSTRACT

Low-temperature (LT) passivation methods (< 450°C) for decreasing defect densities in the material combination of silica (SiO_x) and silicon (Si) are relevant to develop a diverse technology (e.g. electronics, photonics, medicine), where defects of SiO_x/Si cause losses and malfunctions. Many device structures contain the SiO_x/Si interface(s), of which defect densities cannot be decreased by the traditional, beneficial high temperature treatment (> 700°C). Therefore, the LT passivation of SiO_x/Si has been, since long, a research topic to improve applications performance. Here, we demonstrate that a LT (< 450°C) ultrahigh-

vacuum (UHV) treatment is a potential method that can be combined with current state-of-the-art processes in a scalable way, to decrease the defect densities at the SiO_x/Si interfaces. The studied LT-UHV approach includes a combination of wet chemistry followed by UHV-based heating and pre-oxidation of silicon surfaces. The controlled oxidation during the LT-UHV treatment is found to provide an until now not reported crystalline Si oxide phase. This crystalline SiO_x phase can explain the observed decrease in the defect density by halve. Furthermore, the LT-UHV treatment can be applied in a complementary, post-treatment way to ready components to decrease electrical losses. The LT-UHV treatment has been found to decrease the detector leakage current by factor of two.

INTRODUCTION

The material combination of silicon (Si) and silica (SiO_x) has an exceptionally diverse application area including electronics, photonics and medicine.[1-6] The SiO_x/Si interface is part of, e.g. transistor gate, detector mesa sidewall, optical waveguide, and exposed surfaces of porous Si and Si nanowires. Thus, the function of SiO_x/Si also varies, for example, from guiding electricity and light to acting as a tunneling barrier or a molecule capture site. It is, however, common for these different SiO_x/Si-containing applications that material defects are harmful to the performance of applications. For instance, they can cause operation instabilities or electrical and optical losses. The defects at the SiO_x/Si interface increase material non-uniformity and result in extra electron levels in the crucial band-gap area. This leads to further losses and malfunctions of the applications. Therefore, decreasing the defect-level densities in SiO_x/Si is essential to further improve SiO_x/Si-containing devices. The Si-based electronics has used traditionally high temperature (HT) treatments (above 700°C) in order to produce superior SiO_x/Si and HfO_2/SiO_x/Si device materials[1,2,7-12] which possess defect-level densities (D_{it}) down to $1–5 \cdot 10^{10}$ defects/eVcm^2. However, more and more applications require a passivation

of the SiO_x/Si interfaces at temperatures, as low as possible. For example, when SiO_x/Si is combined with metal, polymer, graphene, or glass, the resulting hybrid materials do typically not tolerate elevated temperatures without material degradation. Examples for these hybrid materials are metal interconnections of Si components, amorphous Si thin film transistors on glass, or wafer-bonded heterostructures. Furthermore, manufacturing procedures of Si-containing applications include in practice several low temperature processing steps, where Si becomes readily oxidized and SiO_x/Si is formed without an optimized HT treatment. On the other hand, the usage of HT treatments increases the risk of contamination (e.g. in-diffusion of impurity atoms). In addition, the usage of LT treatments decreases the energy consumption during the manufacturing processes. Therefore, LT treatments to decrease the defect densities of SiO_x/Si are relevant to advance in the very large silicon-based technology.

In electronics, three-dimensional integration of Si components with different materials is intensively investigated to increase the device functionality per chip area.[13-15] The processing temperature is limited to maximum 450°C, the so-called back-end-of-line limit.[13-15] Many hybrid materials, such as metal-Si interconnects, degrade at high temperatures and lose their properties. Therefore, we have chosen 450°C as the upper limit in this work, although it can be necessary to have an even lower limit depending on the applications. The photovoltaics sector has adopted the LT processing (< 450°C) for SiO_x/Si, and is continuously developing the technology for front and rear passivation for Si solar cells.[16-36] HT treatments can change the doping profile of the cells, as well as it can increase the manufacturing costs, energy consumption, and the risk of bulk contamination in the silicon (e.g. via enhanced metal diffusion). LT passivation methods for SiO_x/Si are essential not only for transistor and photovoltaic applications, but also for developing diverse Si-based technologies including, e.g. biomedicine, photo-electrochemistry, photonics, sensors and thin-film-transistors.[37-45]

The atomic layer deposition (ALD) technique is widely used, nowadays, to manufacture insulator-silicon junctions for many devices. ALD is particularly suitable for the LT and 3-D technologies, as the growth temperature of conformal ALD films is often clearly below 450°C. After cleaning the Si surface (i.e. by removing surface oxides and contaminants), it still gets oxidized to some extent during the ALD-film growth, due to oxygen in ALD process. The oxidation of silicon is an energetically driven process, therefore, insulator-Si interfaces normally contain a thin SiO_x layer. This leads for example to the following stacks: $HfO_2/SiO_x/Si$ or $Al_2O_3/SiO_x/Si$. Interface oxides, formed at LT, are typically amorphous or highly disordered. Therefore, the high-quality $HfO_2/SiO_x/Si$ stacks for transistors are often post-annealed above 700°C.[7-12,46,47] The gained benefit of this HT post-annealing arises most likely from an increased degree of crystallization of SiO_x, because HT treatments have been found to provide a crystalline interface layer for SiO_x/Si systems.[48-57] Interfacial crystallization leads to a natural decrease in the density of point defects, as compared to the corresponding amorphous (or disordered) interface. It is essential to note that high-quality transistor $HfO_2/SiO_x/Si$ interfaces are still subsequently hydrogen passivated, in addition to the HT treatments (i.e. combination of HT annealing and hydrogen exposure).

Thus, an important question is, how should SiO_x/Si interfaces be passivated at low temperatures (< 450°C) before and/or after the ALD growth without the above-described beneficial HT step. In order to decrease the density of defect levels in SiO_x/Si, various LT pre-treatments and post-treatments have been investigated intensively for several decades. Two state-of-the-art LT methods are: (i) chemical oxide growth before ALD (e.g. Refs. 21,22,24,30,35,36,58,59) and (ii) hydrogen passivation by post-ALD-annealing in forming gas at temperatures below 450°C (e.g. Refs. 16,17,22,24,25,27,29). Often these two methods are combined. A clear benefit of the chemical-oxide growth is that the method allows a scalable control of the Si oxidation, which occurs, anyhow in an uncontrolled way, at some stage(s) of

the processing. LT post-annealing after ALD activates another type of the interface passivation: the field-effect passivation. Here the fixed charges of the insulator film cause an internal electric field, which repels electrons or holes from the defect-rich interface region. Both the chemical and the field-effect passivation simultaneously affect electrical measurements, and it is in fact difficult to separate their contributions in experimental data.

Undoubtedly, SiO_x/Si is one of the most investigated material systems in the past 60 years. Therefore, a relevant question is whether it is still possible to develop the LT treatments to further decrease the number of defects in Si applications. In this work, we approach the objective from a different perspective; our general goal is to contribute to the bridging of two traditionally rather separated fields: surface science and electrical engineering. We clarify the issue, whether ultrahigh-vacuum (UHV) technology is useful to further develop the LT (< 450ºC) treatments for a diverse SiO_x/Si-based technology. UHV is particularly used in surface science because it enables the preparation of well-defined surfaces. In the UHV preparation methods, relatively high temperatures have been used, e.g. 1200^{o}C flash heating to clean silicon surfaces. Anyhow, previous studies support that the UHV environment is useful to improve device materials in general.[60-62] In this study, we demonstrate that LT-UHV treatments decrease D_{it} of SiO_x/Si, as compared to the state-of-the-art recipe. In addition, we have found that LT-UHV heating enhances the crystalline order of wet chemically cleaned Si surfaces, which are surprisingly disordered after the chemical treatments. Furthermore, by controlled LT oxidation in UHV, a crystalline SiO_x surface phase can be obtained. In order to evaluate the effects of the LT treatments on the interface defect density (D_{it}) and the total charge (Q_{tot}), reference samples with chemical grown oxide, which is the state-of-the-art for solar cells and photodiodes,[26,37] were prepared. Finally, we investigated whether the LT-UHV treatment can be used in a complementary way – post-treatment of ready SiO_x/Si-containing detector components.

EXPERIMENTAL SECTION

Measurements were in part performed in an ultrahigh-vacuum (UHV) multi-chamber system, which allows preparation and characterization of small wafer pieces, 6 mm x 12 mm, and in-situ ALD growth using a prototype instrument of the University of Turku. Low-energy electron diffraction (LEED), scanning tunneling microscopy/spectroscopy (STM/STS) and non-monochromatized X-ray photoelectron spectroscopy (XPS) equipment are attached to the system, enabling in-situ surface characterization without breaking the vacuum. STM was performed by an Omicron instrument in constant current mode. STS current-voltage (I-V) curves were measured with the grid mode. Before numerical analysis of I-V curves, they were averaged over a chosen surface area. Both n-type Si(100) and p-type Si(111) wafer pieces were used. Two different cleaning procedures were used for the small wafer pieces: (i) flash heating up to 1200ºC by feeding a direct current through the Si piece and (ii) a combination of RCA cleaning with LT-UHV heating. The RCA recipe included: pre-clean with acetone, methanol and isopropanol; contamination removal with (3:1 H_2SO_4:H_2O_2, 15 min at 110ºC) + deionized water rinsing + N_2 drying; an SC-1 step with (5:1:1 H_2O:NH_4OH(29%):H_2O_2(30%), 15 min at 80ºC) + deionized water rinsing + N_2 drying; an SC-2 step with (6:1:1 H_2O:HCl(37%):H_2O_2(30%)), 15 min at 80ºC) + deionized water rinsing + N_2 drying. The RCA recipe was finished either with the SC-2 step or with an extra HF (1-5%) dip. The treated pieces were transferred within two minutes in air to the vacuum system. A different UHV system was used to perform 4-inch wafer treatments after the RCA chemical cleaning with a final HF dip. The wafers were transferred to the vacuum chambers within two minutes after the wet chemical treatments. Reflection high-energy electron diffraction (RHEED) was used to monitor the wafer during LT-UHV treatments.

Defect density measurements were performed for the float zone (100) wafers (FZ, Topsil) with a resistivity of 3.0±2.0 Ohm cm and a thickness of 280±15 micrometer. Al_2O_3 films (20 nm) were grown on top of both the LT-UHV pre-treated and the chemical oxide SiO_x/Si interfaces using TMA and water precursors in a Beneq TFS-500 ALD reactor. Thereafter, the wafers were post-annealed at 400°C in N_2 for 30 min. Defect density levels and fixed negative charges of the Al_2O_3/SiO_x/Si were measured by corona oxide characterization of semiconductor (COCOS) technique.[63,64]

Separate capacitor samples were prepared for small surface-science samples (6 mm x 12 mm) using the interconnected ALD prototype (HfO_2), and were measured by precision LCR Meter (HP4284A). A shadow mask was used to deposit the Au/Cr metal contacts by sputtering on top of HfO_2/p-Si(111). Silver paste was used for the backside contact formation.

The post heating tests were performed on commercial photodiode (detector) chips, which were small enough for the surface-science vacuum instrument. The backside of the photodiodes containing an aluminum film was placed in contact with the metal sample holder, which was then transferred to the vacuum system. The heating was performed indirectly with a heater element beneath the sample holder. Leakage currents of the photodiodes were measure with a semiconductor parameter analyzer (HP4145B) at controlled temperatures in dark.

RESULTS AND DISCUSSION

Figure 1 presents a scheme of the investigated LT-UHV approaches, which can be divided into the two categories: pre-treatment (Fig. 1a) and post-treatment (Fig. 1b) methods. The used temperature range is 200–400ºC. In the pre-treatment approach the Si surfaces were cleaned by an RCA-based procedure. The RCA-based procedure is a wet chemical process to remove native oxides and contaminants, which was used for the experiments, except if

mentioned otherwise. The cleaned Si samples were then transferred to an UHV instrument, consisting of a sample heating element and an oxygen gas (O_2) source in the most simple configuration.

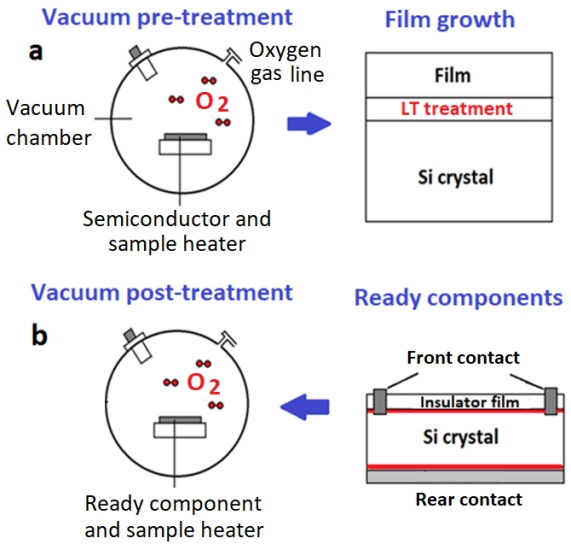

Figure 1. *Schematic of the studied LT-UHV methods. (a) Pre-treatment of Si before a film growth (e.g. by ALD) includes heating and controlled oxidation of the chemically beforehand cleaned Si surface. (b) Post-treatment of Si-based components (e.g. photodiodes, capacitors) containing metal contacts. Red lines highlight the SiO_x/Si-containing parts.*

One goal of the study was to correlate surface properties of Si samples to the different treatments. Therefore, we used a specific surface-science set-up (EXPERIMENTAL SECTION), which enables in-situ measurements without breaking the vacuum in-between. Characterization was started with the surface-science samples: 6 mm x 12 mm pieces of a Si(100) wafer. These small pieces were cleaned with the well-known method of feeding a short direct current through the small piece under UHV conditions. Such flash heating up to 1200°C for several times produces an ultra-clean and crystalline Si surface with a smooth terrace-step structure, containing also the well-known double-domain (2x1)+(1x2) surface reconstruction. Supplementary Fig. S1 exemplifies characteristics of Si(100)(2x1)+(1x2) cleaned by the flash

heating. These Si substrates provide a well-defined platform to study the LT oxidation of Si(100). Figure 2 summarizes the surface measurements after 200 Langmuir (L) oxidation of the Si(100)(2x1)+(1x2) surface at 400ºC in an oxygen containing atmosphere. The O_2 gas was provided via a leak valve. Low-energy electron diffraction (LEED) pattern (inset of Fig. 2a) from this LT-oxidized surface showed only (1x1) pattern, while the double-periodicity (2× and ×2) spots, which are characteristic of the atomically clean Si surface, have disappeared. Therefore, one could consider just the traditionally expected case: a thin amorphous oxide layer was formed on top of the Si(100), in such a way that the native (2x1)+(1x2) reconstruction is destroyed. The visible (1x1) LEED diffraction spots would then come from the (100) bulk-crystal planes beneath the amorphous oxidized surface layer. However, the scanning-tunneling microscopy (STM) revealed something different (Figs. 2a and 2b): very smooth islands, which have not been reported earlier on Si(100) after oxidation. These islands do not exist on the clean Si(100)(2x1)+(1x2) surface. No Si-dimer row structure, which is a characteristic fingerprint of the clean starting surface, was seen on the top of the smooth oxidation-induced islands. This is consistent with the obtained (1x1) LEED pattern. Furthermore, zoomed-in STM images of the island suggest an ordered structure with a row distance close to Si(100) plane lattice constant. In addition, X-ray photoelectron spectroscopy (XPS) confirmed that Si surface was oxidized, as the Si 2p core-level spectrum includes the oxidation-induced shoulder[52] (Figure 2c) and the O 1s intensity increased significantly (Fig. 3a). Moreover, the scanning-tunneling spectroscopy curve from the LT-oxidized surface (Fig. 3b) showed a significant increase in the surface-band gap up to 5 eV, which is consistent with the formation of SiO_x. The surface band-gap of clean Si(100)(2x1)+(1x2) is approximately 0.5 eV (see Fig. S1). The above results indicate the formation of a hitherto not reported crystalline SiO_x layer, which is formed at the surface of clean silicon at the low temperatures. It is interesting to compare our results to the firstly reported epitaxial SiO_x interface layer (tridymite type) discovered by cross-

sectional transmission electron microscope.[48] Ourmazd *et al.* explained that the key for their finding was the preparation of a very smooth and highly crystalline starting Si surface by means of a sophisticated silicon molecular-beam-epitaxy (MBE) technique. The resulting grain size of the SiO_x crystals is determined by the spacing between atomic-scale steps on the clean surface before the oxidation.[48] Although we have not used the MBE method, we prepared a well-defined starting surfaces for the subsequent oxidation studies. The detailed stoichiometry of the obtained SiO_x will be addressed in future studies. The XPS result in Fig. 2c shows that the high binding-energy tail is shifted by less than 3.7 eV of bulk SiO_2. The STS result in Fig. 3b shows that the resulting band gap is smaller than that of bulk SiO_2 (about 9 eV). Therefore, XPS and STS indicate that the stoichiometry of the obtained crystalline SiO_x should be different from SiO_2 (i.e. $x < 2$). However, possible effects of the thin film nature on the core-level shift and the surface band gap need to be still clarified. A contour line-profile curve (see Fig. S2) shows that the height of the islands can be at least 0.8 nm. Furthermore our preliminary tests for oxidation of Si(111) wafer pieces (see Fig. S3) suggest that the crystalline oxidation at LT is not limited to Si(100) surfaces, but might be a more general property at well-defined conditions.

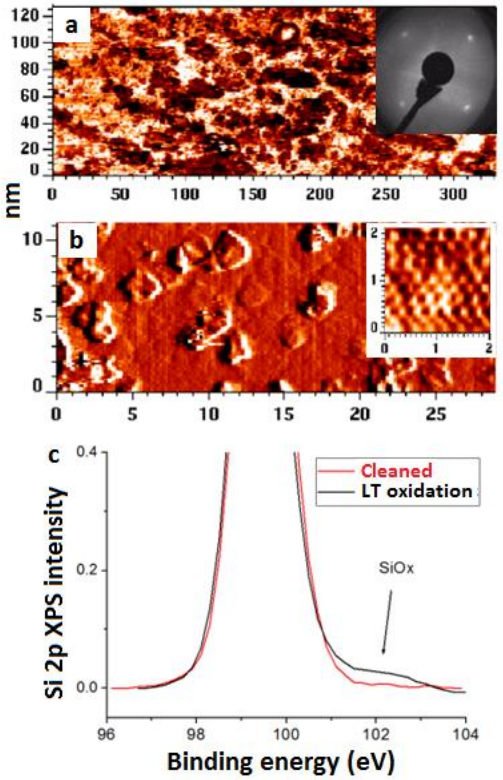

Figure 2. *Surface-science characterization after LT oxidation of Si(100) at 400°C. (a) Large-scale STM of LT-oxidized Si(100), and the inset shows the (1x1) LEED-pattern from the same surface. (b) Smaller-scale STM image from the same surface, and the inset shows atomic scale ordering. (c) Si 2p XPS spectra before and after the LT oxidation.*

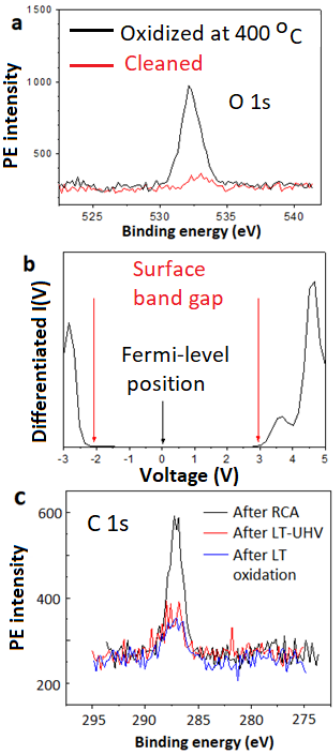

Figure 3. *Surface-science characterization after low-temperature (400°C) oxidation of Si. (a) X-ray photoelectron spectroscopy (XPS) intensity comparison of oxygen O 1s core level shows a clear incorporation of oxygen due to 200-L exposure. (b) Scanning tunneling spectroscopy indicates a surface band gap of 5 eV approximately, which is consistent with SiO_x formation at the Si surface. (c) XPS measurements show that pure LT heating in ultrahigh-vacuum (UHV) condition decreases carbon contamination, which might be related to the wet chemical pre-treatment.*

Next, we investigated the possibility of cleaning Si surfaces utilizing the LT-UHV heating, which would make it possible to perform the whole process, cleaning and oxidation, below 450ºC in UHV condition, instead of cleaning the samples at 1200ºC. Figure 4 exemplifies a cleaned Si(100) surface after the RCA procedure was finished with an HF dip. Figure 4a shows a reflection high-energy electron diffraction (RHEED) pattern from the HF etched Si(100), which includes sharp white (1x1) streaks. This shows how disordered (or amorphous) the topmost surface is still after the widely used RCA treatment. As can be seen from the STM images in Figures 4b and 4c, there is no long-range atomic ordering. Therefore, the sharp (1x1) RHEED pattern arises from the bulk crystal planes beneath the topmost disordered layer. This issue might have been underestimated previously, if the (1x1) diffraction pattern has been taken as prove of crystal quality of Si sample. This disordered surface with many point defects, which is obviously far from the ideal (100) crystal plane, one has to keep in mind when proceeding towards the next device processing steps, like ALD. Thus, our result supports that one should be careful when making conclusions about the surface quality based only on diffraction patterns, which are not sensitive to local defects.

Figures 4d–4f present effects of the LT-UHV heat treatment on the above-described RCA cleaned Si(100) piece, when heating them up to 400ºC. First, (2x1) reconstruction-related streaks appear between the sharper (1x1) streaks in RHEED, which means some ordering at the topmost layer occurs. STM images support the re-ordering, as short (2x1)-type dimer rows can be observed in Figure 4f. It is interesting to note that LEED shows clearly weaker (2x1) features (not shown here) after the same LT-UHV heating, as compared to RHEED. In other words, RHEED is more sensitive to those changes than LEED. Furthermore, XPS shows that the LT-UHV heating also decreases the amount of carbon contamination, which is difficult to avoid when using wet chemical treatments, by a factor of approximately two, as can be also seen in the C 1s intensity comparison given in Fig. 3c. To

recapitulate, the LT-UHV heating increases the degree of crystallization at the Si surfaces, which suggests a natural decrease in the point-defect density.

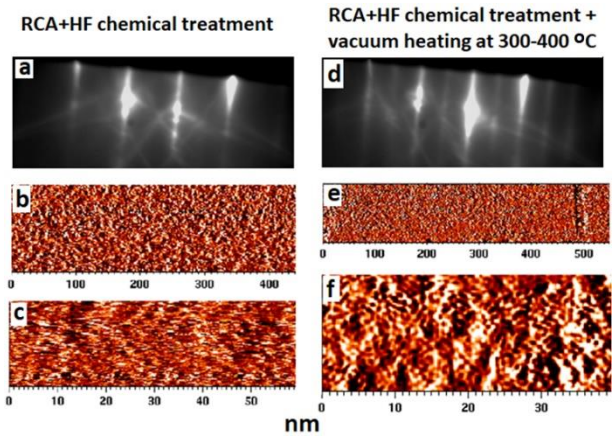

Figure 4. *Effect of LT-UHV heating on structural properties of chemically cleaned Si(100). (a)-(c) Reflection high-energy electron diffraction (RHEED) before heating shows (1x1) diffraction streaks for RCA cleaned Si(100) completed by HF dip. Large-scale and zoomed-in STM images after this chemical treatment. (d)-(f) RHEED reveals that surface ordering improves due to 300-400°C heating in UHV, because surface-related (2x1) diffraction streaks appear. Zoomed-in STM image after the UHV heating shows a local dimer row structure, consistent with the (2x1) RHEED. Local dimer row directions are about 45 degree from horizontal.*

For electrical characterization, 4-inch Si(100) wafers were prepared by standard RCA cleaning. Then the wafers were thermally oxidized to protect them during wafer transfer via air. Before introducing the wafer to the full-wafer-compatible UHV system, the thermal oxide was removed with a 10% HF solution. The wafer surface was monitored with RHEED during the UHV heating and oxidation. The (2x1) reconstruction of clean Si(100) became visible in RHEED at around 350°C, as described above. Then oxidation of the wafer was performed at the same temperature range with 200-L exposure by introducing O_2 gas to the

UHV chamber via a leak valve. After the oxidation, the wafer was left to cool down under vacuum, until it reached room temperature. The characterization of the wafers was performed at a different laboratory. Therefore, the wafer was moved from the vacuum system to an inert atmosphere (argon gas) glove box, to be packed for the transfer. The wafers were placed in wafer boxes and sealed in double clean-room plastic bags to maintain the wafers in inert atmosphere during the transfer of 3–4 hours. For the following Al_2O_3 deposition, the wafers were then transferred from the argon bags to the ALD system in atmospheric conditions during 3–4 minutes. Two different reference wafers were used: the first control sample was prepared by the standard RCA cleaning, which includes a final HF dip before ALD. The second reference contained a thin chemical oxide layer[26,37] grown before the ALD deposition. The interface defect density (D_{it}) and the total charge (Q_{tot}) were measured by the corona-oxide characterization of semiconductors (COCOS) technique (EXPERIMENTAL SECTION and Fig. S4).

Table 1 presents the D_{it} and the Q_{tot} values for the LT-UHV pre-treated n-type and p-type wafers, as well as for the two different reference wafers. We performed two or three measurements on each sample from different locations. From these measurements we selected the lowest measured D_{it} value and the highest measured Q_{tot} value and then calculated the standard deviation from all the corresponding measurement points. The error limits were defined based on the standard deviation. It is remarkable that the LT-UHV treatment provides smaller D_{it} than the chemical oxide reference.[26,37] In contrast, the total charge is larger for the chemical oxide reference than for the LT-UHV pre-treated p-type wafers (Table 1). However, for n-type wafers, the total charge Q_{tot} seems to be higher after the LT-UHV treatments, but further investigations are needed. Furthermore, it is necessary to further investigate, why the decrease of D_{it} for p-Si is higher than for n-Si after the LT-UHV treatment. The result at first sight may indeed look like that the UHV treatment works better for p-Si than for n-Si. However,

if we look at the initial D_{it} values for n-Si, we can see that it is already very low. Therefore, it is not that surprising that the UHV treatment is not affecting n-Si surface as much as p-Si surface. We would like still to emphasize how essential it is for the presented D_{it} comparison that the reference samples were prepared and measured simultaneously using the state-of-the-art chemical oxide recipe,[26,37] providing a well-justified benchmarking. Usually it is difficult to compare directly with the interface characteristics reported in the literature for different samples (e.g. different silicon resistivity and insulator growth conditions), which have been often measured by different methods or setup as well. It can be mentioned that the lowest D_{it} obtained during test trials of this project was $4.1 \cdot 10^{10}$ $eV^{-1}cm^{-2}$ for a separate n-type LT-UHV-treated wafer, suggesting that there is still much room for future optimizing of the LT-UHV recipe. This D_{it} is close to one of the lowest D_{it} values reported in the literature[19] for the $Al_2O_3/SiO_2/Si$ stack manufactured below 450ºC. A frequency dispersion of capacitance-voltage data was used to determine that D_{it}.[19] Interestingly, Dingemans *et al.* used ALD to grow the useful interfacial SiO_2 layer.[19]

The above results were obtained using the LT-UHV pre-treatment (Fig. 1a). The next question is naturally whether the LT-UHV method can be used in complementary way to modify the properties of ready components. Such post-treatment (Fig. 1b) should be possible, as many metal-semiconductor junctions are known to tolerate temperatures below 450ºC. SiO_x/Si-containing photodiode or detector chips were chosen for the LT-UHV post-treatment experiments because they are known to suffer from the following specific surface problem. The photodiode manufacturing process typically requires cutting (or dicing) of the processed wafers into the corresponding chips. After cutting, the sidewalls of the chips are exposed to atmospheric conditions, as they are lacking any proper passivation at those surfaces. Additionally, cutting introduces scratches to the sidewalls, which further reduces the crystal quality. The damaged sidewalls introduce large amounts of additional electronic defect levels

in the band-gap area, which e.g. increase the leakage current of detectors[65] via the increased thermal excitation of the electric carriers. The standard passivation methods, used during the wafer scale processing, are difficult to apply to individual component chips or are not compatible with some device component. Therefore, LT treatments are relevant, when developing passivation methods for sidewalls of the ready component chips, before the final chip packaging or encapsulation. The low temperature is essential here, as the ready components include already metal contacts, limiting the post-treatment temperature a maximum of around 450ºC in many cases.

Table 1. *Defect densities (D_{it}) and total negative charge (Q_{tot}) for p-type and n-type planar Si wafers after the LT-UHV pre-treatment. Two different reference samples were used: 1. Reference includes the traditional RCA cleaning with a final HF dip before the ALD growth. 2. Reference includes the preparation of a chemical oxide before ALD deposition.*[26,37]

	1. Reference sample with RCA and HF	**2. Reference sample with chemical oxide**	**LT-UHV pre-treated sample**
D_{it} ($eV^{-1}cm^{-2}$) for planar p-Si	$5.6 \cdot 10^{11} \pm 8.0 \cdot 10^{10}$	$3.4 \cdot 10^{11} \pm 6.4 \cdot 10^{10}$	$1.3 \cdot 10^{11} \pm 1.4 \cdot 10^{10}$
Q_{tot} (e/cm^{-2}) for planar p-Si	$7.9 \cdot 10^{11} \pm 6.7 \cdot 10^{10}$	$1.8 \cdot 10^{12} \pm 3.1 \cdot 10^{10}$	$5.3 \cdot 10^{11} \pm 1.1 \cdot 10^{11}$
D_{it} ($eV^{-1}cm^{-2}$) for planar n-Si	$1.7 \cdot 10^{11} \pm 7.5 \cdot 10^{10}$	$2.7 \cdot 10^{11} \pm 9.1 \cdot 10^{10}$	$1.5 \cdot 10^{11} \pm 1.5 \cdot 10^{10}$
Q_{tot} (e/cm^{-2}) for planar n-Si	$1.2 \cdot 10^{12} \pm 1.1 \cdot 10^{11}$	$1.3 \cdot 10^{12} \pm 6.6 \cdot 10^{10}$	$2.6 \cdot 10^{12} \pm 1.3 \cdot 10^{11}$

The commercial Si detectors used in our experiments were based on a low doped n-type Si substrate. At the front surface, they included p-type doped regions and a highly n-doped layer at the rear surface. The front surface contains Al_2O_3-coated planar and black-silicon[22,26,29,32,37] surface structures between the p-metal contact rings (Fig. 5 and Fig. S5). According to our observations, the results presented below do not depend on the surface-structure type. Leakage currents were measured, before and after the vacuum treatments, between the backside contact and the inner front-contact ring, as well as between the backside contact and the outermost guard ring (Fig. S5 shows a schematic detector structure). The guard-ring leakage current varied before any post treatment for the different chips. It was lower or higher than the actual detector leakage current measured via the inner ring. This can be linked to different quality of the cutting. The measurements were performed in well-controlled temperature (Fig. S6) and dark conditions.

Single detector chips were treated in the surface-science UHV system. The post-treatments at 200–400ºC with $5\cdot10^{-6}$–$1\cdot10^{-4}$ mbar oxygen (O_2) pressure for 30 min decreased the leakage current between the rear contact and the inner ring by a factor of two approximately, as exemplified in Fig. 5c for one chip (another chip is shown in Fig. S6). A similar decrease in the leakage current was found for five different chips tested. Concomitantly, it was confirmed that the LT-UHV post-treatment did not degrade the optical external quantum efficiency (Fig. S7). The LT-UHV post-treatment can decrease the amount of defect-induced gap levels at the detector sidewall region by re-forming their surface-oxide structure. This scenario is possible, although the inner-contact leakage particularly decreased: The band bending along the direction perpendicular to the sidewalls can readily push the electric carriers, which are thermally excited via sidewall defect levels, toward the detector bulk (Fig. S5 presents a scheme for this explanation). Therefore, the sidewall defects affect not only the outermost ring current, but also the inner-contact current. The found decrease in the leakage can be thus associated

with a decrease in the amount of pushed electrons towards the bulk from the sidewalls. The second possible reason arises from a re-arrangement of hydrogen atoms inside the detector material via diffusion, which can occur also at low temperatures. The hydrogen incorporation is possible during the manufacturing process. It has been previously shown that the hydrogen can act as a point defect, in addition to its beneficial role in passivating point defects of Si-based device material.[66,67] It is essential that the found decrease in the photodiode leakage current is durable. This can be confirmed by the measurements performed after six months that show the same result, as exemplified in Fig. S6. Moreover, it can be expected that the found decrease in D_{it} should be visible also in another type of the leakage, through a metal-oxide-semiconductor stack. Indeed, our preliminary tests suggest a decrease in the capacitor leakage current due to the vacuum treated interface (Fig. S8). As these capacitors contained another insulator, HfO_2 grown by ALD, the results suggest the presented LT-UHV treatment is applicable in a more general way, not only for $Al_2O_3/SiO_x/Si$. Furthermore, these capacitors were prepared on Si(111), which supports that the LT-UHV treatment is useful for different surface orientations.

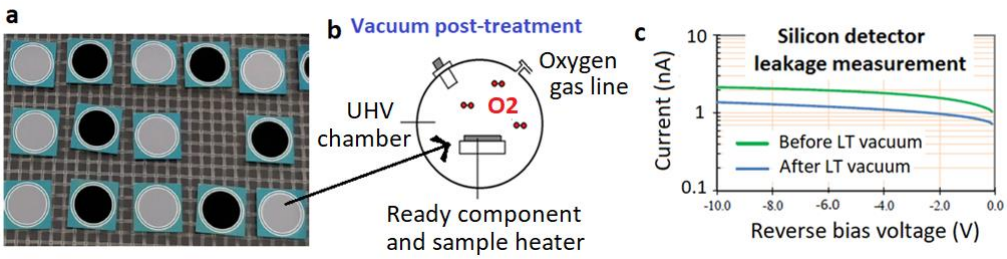

Figure 5. *LT-UHV post-treatment experiments. a) Photograph from the finished silicon detectors (gray planar and black-silicon coated, a detailed structure in Fig S5), which were (b) post-treated in UHV chamber at low temperatures 200–400°C at $5 \cdot 10^{-6}$–$1 \cdot 10^{-4}$ mbar oxygen pressure (O_2) for 30 min. c) Example current-voltage curve to show, how the post-treatment decreases the leakage current of detectors to about half.*

Vacuum technology including UHV systems have been already utilized in specific industrial processes of semiconductor technology: e.g. in molecular-beam-epitaxy growth of semiconductor device heterostructures, as well as in deposition of metal films for the electrical contacts of devices. The potential of the vacuum technologies to improve the application of different materials has been shown previously (e.g. Refs. 60-62). The vacuum technology has been particularly at the heart of surface science, where the UHV conditions are often required to prepare clean and well-ordered surfaces of various solids, and to keep these surfaces clean and crystalline for long enough time to obtain measured data from well-defined materials. However, the temperatures used typically in the UHV-based experiments have been high, and the maximum temperatures that solids tolerate have been often utilized. For instance, pieces of Si crystals have been heated at around 1200ºC to obtain the well-crystalline substrate surface for further investigations. Thus, it has previously remained unclear, how well the UHV technology is able to tackle the LT requirements of semiconductor industry. The benefit of the UHV technology is obviously very clean environment for processing materials, which should naturally decrease contamination-induced point-defect densities for instance. On the other hand, any extra processing step like the UHV heating is also a possible contamination source, which needs to be handled carefully.

CONCLUSIONS

We have investigated the issue, whether it is possible to decrease defect densities of the widely used SiO_x/Si interfaces by means of a low-temperature (LT) ultrahigh-vacuum (UHV) approach, because in many stages of the manufacturing processes of SiO_x/Si-containing applications, the beneficial high temperature treatment (> 700ºC) cannot be utilized to decrease defect-induced losses and malfunctions. The considered LT-UHV treatments can be combined

with the current processing technology in two complementary ways: as a pre-treatment before the insulator growth (e.g. ALD) and as a post-treatment for ready components. We have shown that it is useful to perform the UHV-based heating and oxidation at < 450°C after the wet chemical treatment of Si surfaces and before the ALD growth of insulator films. This approach leads to a decrease in the defect-level density (D_{it}) as compared to the state-of-the-art chemical oxide reference. The decreased D_{it} is consistent with the found decrease in the leakage currents due to the proper LT-UHV treatment, and also with the finding of hitherto not reported crystalline SiO_x, which forms at surprisingly low temperatures in proper oxidation conditions. The observed improvement in the SiO_x/Si passivation together with the result that the reference chemical oxide samples provide a higher fixed charge for the p-type material suggests that in future, it is interesting to study also how the LT-UHV method and the chemical-oxide growth (or ALD of SiO_2) can be combined in optimized way.

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ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website. STM/STS results and LEED patterns for the flash-heated clean Si(100) surface. STM characterization for a low-temperature oxidized Si(111) surface. COCOS spectrum for D_{it}. Photodiode layer structure. External quantum efficiency curves for photodiodes. Capacitance-voltage and leakage current measurements for HfO_2/p-Si(111) capacitors.

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