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Materials and Technology Issues for the Next Generation of Power Electronic Devices

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By 2030, about 80% of all US electricity is expected to flow through power electronics. This will require power electronic devices and circuits with much higher efficiency and smaller form-factor than today's silicon-based systems. III-Nitride semiconductors and other ultra-wide bandgap materials are ideal platforms for the new generation of power electronics thanks to the combination of excellent transport properties and the high critical electric field enabled by their wide bandgap [1]. This talk will discuss recent progress in our group in developing high voltage power transistors and diodes based on wide bandgap materials.

Vertical GaN-based FinFET power transistors have a great potential for 1200 V applications (Figure 1-2)[2]. The high current density, in combination with minimum parasitics, allow these devices to achieve beyond-state-of-the-art switching performance as summarized in Table 1. In addition, their simple structure and absence of p-type layers is expected to significantly lower their manufacturing cost compared to the traditional vertical transistor architectures. The manufacturing cost can be reduced even further by fabricating these devices on either silicon wafers or engineered substrates, although some key trade-offs between leakage currents and performance need to be carefully studied.

The talk will also discuss the opportunities and challenges brought to power electronic devices by ultra-wide bandgap materials beyond GaN. Specifically, some recent results on AlGaN-channel transistors [3] (Figure 3-4) and vertical diamond devices will be benchmarked with the state-of-the-art devices, and a roadmap for future device development will be presented.

The talk will conclude with a summary of recent work on the heterogeneous integration of power switches, gate drivers and control electronics - a key requirement for reaching the full potential of wide bandgap materials. A new GaN CMOS-driver compatible with standard GaN power devices will be demonstrated (Figure 5-6)[4] as an example system.

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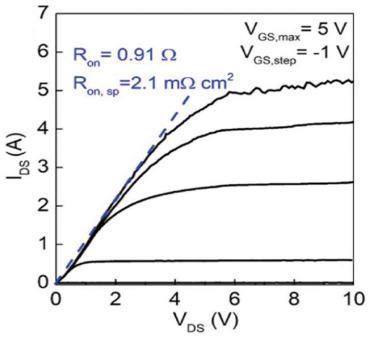

Figure 1: Output characteristics and extracted R_{on} and $R_{sp,on}$ in a vertical GaN power FinFET.

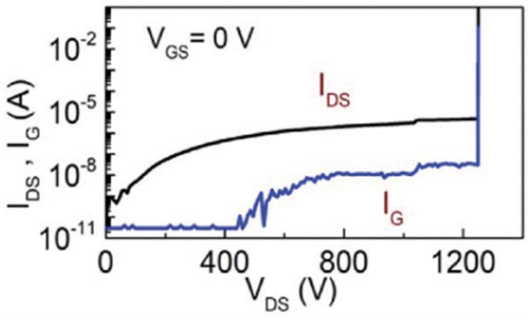

Figure 2: Off-state leakage of a vertical FinFET measured at V_{GS} = 0V, demonstrating a breakdown voltage of 1250 V.

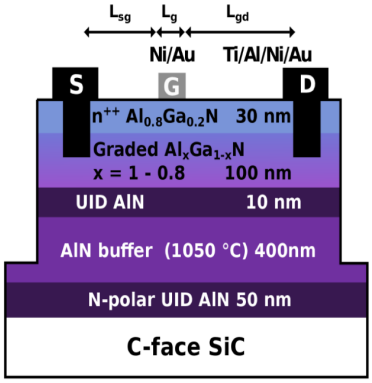

Figure 3: Schematic cross-section of the fabricated N-polar AlGaN/AlN PolFET with recessed contacts.

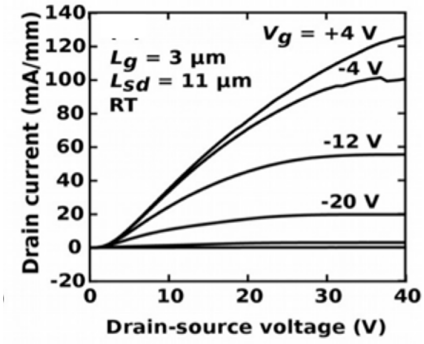

Figure 4: Output characteristics of N-polar PolFET with a 30-nm-thick Al_2O_3 gate dielectric.

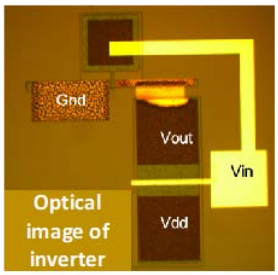

Figure 5: Optical image of a complementary logic GaN inverter fabricated on a GaN-on-Si platform.

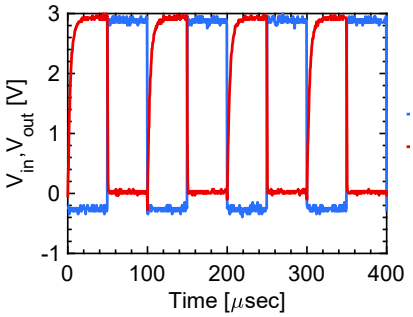

Figure 6: Transient response of the GaN complementary logic inverter shown in Figure 5.

TABLE I. Summary and benchmark of device technologies and their key device metrics for 900-1200 V power switching applications.[2]

Device Technology	Manufacturer / Maker	$R_{on,sp}$ (mΩcm²) (R_{on})	BV (kV)	I_{rating} (A)	Chip Area (mm²)	V_{TH} (V)	C_{iss} (pF)	C_{oss} (pF)	Q_G (nC)	Q_{GD} (nC)	Q_{rr} (nC)	Switching FOM (nΩ·C) R_{on}·(Q_G+Q_{oss}) R_{on}·(Q_G+Q_{oss}+ Q_{rr})
GaN Vertical FinFET (this work)	**MIT**	**2.1** (0.91 Ω)	**1.2**	**5**	**0.45**	**1.3**	**248.3***	**42.2***	**1.24**	**2.72**	**~0**	**3.3** **~2.0 (pad optimized)**
SiC MOSFET (CPM2-1200-0160B)	Cree	2.7 [19] (0.16 Ω)	1.2	20	6.28	2.5	525	47	34	14	105	7.68 24.48 (include Q_{rr})
SiC JFET Cascode (UJN1208Z)	United SiC	1.7*** (0.15 Ω)	1.2	18.4	>1.13***	4.4	738	58	30	6	63	5.4 14.85 (include Q_{rr})
Si IGBT (NGTB15N120FLWG)	ON Semi	~20 (~0.25 Ω)	1.2	15	320	2	3600	110	150	68	1500	54.5 429.5 (include Q_{rr})
Si CoolMOS (IPD90R1K2C3)	Infineon	~8**** (1.2 Ω)	0.9	5	~23.6	3	710	35	28	12	3700	48 4488 (include Q_{rr})
GaN HEMT Cascode [20]	Transphorm	(0.19 Ω)	1.2	>20	N.A.	2.3	N.A.	43.1	10	N.A.	N.A.	N.A.
Vertical GaN MOSFET [5]	TOYODA GOSEI	2.7	1.2	23.2	2.25	3.5	N. A.					
Vertical GaN CAVET [2]	Avogy	2.2	1.5	2.3	0.17	0.5						

Note: *@V_{DS}=200 V; **Source: http://unitedsic.com/cascodes; ***Calculated by using the R_{on} in the data sheet and the reported $R_{on,sp}$, reflecting the active device area (not including pad/edge areas); ****Source: Infineon's application note titled "CoolMOS™ C7: Mastering the Art of Quickness".