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A 0.39–3.56-μW Wide-Dynamic-Range Universal Multi-Sensor Interface Circuit

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Abstract—This paper presents an ultra-low-power, wide-dynamic-range interface circuit for capacitive and resistive sensors. The circuit is implemented as a switched-capacitor circuit using programmable capacitors to achieve high configurability. The circuit was fabricated using a CMOS 0.18-μm process. Different types of capacitive and resistive sensors were measured using the Interface to demonstrate its support for multi-sensor systems with an ultra-low-power budget. Experimental results show that the circuit is able to interface various sensors within the overall capacitance range of 0.6–550 pF and resistance range of 3.7–5100 kΩ, while consuming only 0.39–3.56 μW from a 1.2 V supply. A proximity, gesture, and touch-sensing system is also developed consisting of the designed Interface circuit and a sensor element that is able to detect the displacement of an object up to 15 cm from the sensing electrodes consuming only 0.83 μW from a 1.2 V supply.

Index Terms—Ambient intelligence, C2V, capacitive sensor, charge-sensitive amplifier, CMOS, current source, environmental sensor, force sensor, humidity sensor, Interface circuit, Internet-of-Things (IoT), light sensor, proximity sensor, resistive sensor, switched capacitor circuit, ultra-low-power.

I. INTRODUCTION

Sensors are one of the key elements for enabling emerging technologies such as Internet of things (IoT) and ambient intelligence (AmI) [1]–[4]. In IoT and AmI environments we are surrounded by embedded intelligent objects that sense different quantities of our physical surroundings. As IoT and AmI develop rapidly, there is an increasing demand for microsystems that are equipped with various types of sensors. IoT devices are typically battery-powered or rely on harvesting energy from their environment, therefore limiting their power budget. They often require long lifetimes as well which further limits the power consumption and increases the need for ultra-low-power solutions [5].

The size, cost and power consumption of multi-sensor microsystems can be reduced by using an ultra-low-power, highly configurable, and wide-dynamic-range interface circuit that reads and processes different types of sensors. However, making such an interface circuit is technically difficult since each sensor has its own properties and may have different requirements for readout. General-purpose interface electronics have been researched extensively and several sensor interface circuits have been reported in the literature [6]–[21]. Although they present effective solutions, they suffer from some shortcomings such as supporting only one input type (capacitance or resistance) [6]–[15], having low accuracy [6], [9], [13], a low input dynamic range, [9], [14], or high power consumption [7]–[9], [15]–[20].

This paper presents a universal multi-sensor interface (UMSI) circuit that is highly configurable and achieves a wide capacitive and resistive dynamic range with ultra-low power consumption. The target is to interface various capacitive and resistive sensor elements, such as [22]–[25], over an overall range of three orders of magnitude. The interface is configurable so that only the required range is covered for a given sensor element. This allows for optimizing sensitivity, linearity and power consumption for
The proposed system also offers gesture and touch-sensing capacitive proximity systems. In addition to proximity, the existing single-plate [31] and dual-plate [32] detectable distance range and >10× lower current consumption than the existing single-plate [31] and dual-plate [32] capacitive proximity systems. In addition to proximity, the proposed system also offers gesture and touch-sensing capabilities.

II. DESIGN AND IMPLEMENTATION OF THE UMSI

Fig. 1 illustrates the conceptual block diagram of the UMSI. It is based on a switched-capacitor (SC) front-end interface circuit that utilizes a shared SC operational transconductance amplifier (OTA), to realize a SC capacitance-to-voltage (C2V) converter for capacitance sensing and an SC voltage amplifier for resistance sensing. The system consists of a non-overlapping (NOL) clock phase generator to run the SC circuits; memory registers to configure the front-end operation mode and range for various sensors; a measurement buffer amplifier; a programmable bias current generator for the OTA; and a current reference (implemented off-chip for more flexible testing), required by the resistive sensor.

Fig. 2 (a) shows the schematic of the complete UMSI front-end. It is an SC circuit consisting of a low-power OTA, an 8-bit reference capacitor bank $C_{\text{ref}}$, a 5-bit amplifier feedback capacitor bank $C_r$, multiplexers (MUXs), and switches. Depending on the chosen bit configuration ($B_{\text{mod1}}$, $B_{\text{mod2}}$), the interface operates as a resistive or capacitive sensor interface. $C_{\text{ref}}$ and $C_r$ are controlled using bits $B_{\text{B1}}$-$B_{\text{B7}}$ and $B_{\text{B0}}$-$B_{\text{B4}}$, respectively, to accommodate for a wide range of sensor elements and compensate for process variation. For further flexibility, the MUXs, controlled by $B_{\text{B5}}$-$B_{\text{B6}}$, determine which of the NOL clock signals $\text{clk}_1$ and $\text{clk}_2$ is fed to the corresponding switch, or whether the switch should be disabled. Bottom plate sampling is used to reduce the effects of switch charge injection [33]. It is implemented by disconnecting the virtual ground (node N) from $V_{\text{ref}}$ at falling $\text{clk}_{\text{in}}$ - slightly before turning off the switches controlled by $\text{clk}_1$. Charge injection from the switches controlled by $\text{clk}_2$ does not cause output error.

Fig. 2 (a) also illustrates a simple electrical model of a capacitive sensor element $C_{\text{sen}}$, that incorporates the effects of a parasitic shunt conductance $G_s$ and two parasitic capacitances $C_{p1}$ and $C_{p2}$ which include all parasitic capacitances seen at the nodes $\text{pad}_{\text{sen}}$ and $\text{pad}_{\text{res}}$, respectively [34]. Since the values of these parasitics are typically application dependent and not very stable, the effects of these parasitic elements should be significantly reduced. The correlated double sampling (CDS) technique [35] is used to compensate the amplifier I/f noise and input offset voltage, and reduce the effect of parasitic shunt conductance $G_s$ and parasitic capacitance $C_{p1}$ [6], [34]. The voltage swing at node “N” and input of the OTA is small, arising only from noise and finite gain, and so the effect of parasitic capacitance at these nodes is negligible. The circuit is also insensitive to the parasitic capacitance $C_{p2}$ and the total parasitic capacitance seen at the resistive sensor input $V_{\text{res}}$. The supply voltage $V_{\text{DD}}$ and reference voltage $V_{\text{ref}}$ are 1.2 V and 0.6 V, respectively.

A. Capacitive Mode

Fig. 2 (b) presents the UMSI configured in the capacitive mode. The circuit is a SC charge sensitive amplifier based on [6] and it converts the capacitance $C_{\text{sen}}$ into a proportional sampled voltage $V_{\text{out}}$. During $\text{clk}_1$, $C_{\text{ref}}$ and $C_r$ are reset and a charge of $Q_{\text{sen}} = -V_{\text{ref}} C_{\text{sen}}$ is sampled in $C_{\text{sen}}$. In phase $\text{clk}_2$, a charge $Q_{\text{ref}} = V_{\text{ref}} C_{\text{ref}}$ is sampled in $C_{\text{ref}}$, and the sampled charges are transferred in $C_r$, resulting in output voltage

$$V_{\text{out}} = V_{\text{ref}} \frac{C_{\text{ref}} - C_{\text{sen}}}{C_r} + V_{\text{ref}}$$

(1)

which can be used for determining the $C_{\text{sen}}$ value:

$$C_{\text{sen}} = \frac{C_r}{V_{\text{ref}}} V_{\text{out}} + C_r + C_{\text{ref}}$$

(2)

By substituting the allowed output voltage range $V_{\text{out}} = [V_{\text{min}}, V_{\text{max}}]$ in Eq. (2) we can determine the allowed $C_{\text{sen}}$ range for given values of $C_r$ and $C_{\text{ref}}$. The OTA offset voltage and low frequency noise is sampled in $C_{\text{dse}}$ in phase $\text{clk}_1$, and held during $\text{clk}_2$, to generate a CDS-compensated virtual ground (node N).

B. Resistive Mode

Fig. 2 (c) presents the UMSI configured in the resistive mode. $I_{\text{ref}}$ is used for converting $R_{\text{sen}}$ into the voltage $V_{\text{res}}$.
which is fed to an SC voltage amplifier. During phase clk₁, 
C_{ref} and C_{t} are reset and C_{res} samples the voltage V_{res} - V_{ref} = R_{sen} I_{ref} - V_{ref}. During phase clk₂, C_{ref} samples V_{ref} and 
the resulting charge, as well as the charge sampled in C_{res}, 
is transferred in C_{f}. This results in output voltage 

\[ V_{out} = (R_{sen} I_{ref} - V_{ref}) \frac{C_{res}}{C_{f}} + V_{ref} \frac{C_{ref}}{C_{f}} + V_{ref} \]  

which can be used for determining the R_{sen} value: 

\[ R_{sen} = \frac{C_{t}}{C_{res} I_{ref}} V_{out} + \left( 1 - \frac{C_{f}}{C_{res}} \right) \frac{V_{ref}}{I_{ref}} \]  

Again, by substituting the allowed output voltage range 
V_{out} = [V_{min}, V_{max}] in Eq. (4) we can determine the 
allowed R_{sen} range for given values of C_{t} and C_{ref}. C_{cds} is used for 
CDS compensation the same way as described in Sec. II A.

### C. Operational Amplifier

Since the interface circuit is designed to operate in various 
configurations with various capacitance sizes, the operational 
amplifier should also have flexible properties so that it provides 
the required gain-bandwidth product (GBW) for operating at 
different configurations and clock frequencies while maintaining 
a high enough DC gain for the targeted output swing and 
optimized power consumption. A folded cascode OTA, shown 
in Fig. 3, was designed to fulfill these requirements. Clamp 
transistors (inside the dashed box) were added to improve the 
slew rate [36].

In the designed OTA, the open-loop DC gain stays above 
80 dB for the target output swing of 0.6 V. The GBW remains 
well above 10 x intended clock frequency f_{clk}. It scales linearly 
over a 30 x range with a programmable bias current I_{bias}. 
The differential input transistors of the designed OTA have 
large W/L ratios to keep them in the sub-threshold region over 
the used I_{bias} range. This serves two purposes: first, it optimizes 
the power efficiency of the OTA by maximizing the 
transconductance g_{m} of the input transistors for a given bias 
current. Second, the g_{m} scales linearly with the used I_{bias} = 
1.8mA–54mA (30 x range). This is due to the fact that, in 
sub-threshold operation, the g_{m} is directly proportional to the drain current [36], [37]. Since the GBW of the OTA is proportional 
to the g_{m} of the input stage, it also scales linearly over the used 
I_{bias}. Fig. 4 shows the g_{m} of the differential input transistor of 
the OTA as a function of the used programmable I_{bias}, and as 
a function of the total current consumption I_{DD} of the OTA 
including the current consumption of the biasing network.
The 1/f noise corner remains well below the intended f_{DC} and also scales with I_{bias}, ensuring the effectiveness of CDS for reducing the 1/f noise. The OTA power consumption varies between 0.12–3.58 µW over the used I_{bias} range.

D. Leakage-Compensated Programmable Bias Current Generator

A leakage-compensated wide-trimming-range current source was designed to enable a power-optimal wide trimming range for the operational amplifier speed. Trimming is done digitally by adjusting the number of effective unit devices in the current mirror that sinks the output current. To enable accurate current mirroring ratios and high output impedance, the dimensions of the mirroring transistor unit device need to be well above the minimum. In addition, as the required trimming range is high, the number of required unit devices is high as well.

Generally, current source output current can be digitally controlled by disabling parallel unit transistors through a) disconnecting their drain from the output or b) through switching their gate-to-source voltage to zero. The former method suffers from reduced switch control voltage headroom, especially in low voltage designs, resulting in currents that are too low at high output current settings and low temperatures. Trying to compensate this with larger switch devices will result in too high a leakage due to the high number of large unit devices. The latter method suffers from leakage through disabled unit transistors, resulting in too high currents at small output current settings and high temperatures which is also due to the high number of large unit devices. However, this can be compensated with replica leakage devices, by subtracting the replicated leakage from the output.

The proposed leakage-compensated current source is depicted in Fig. 5. The bias current generator core is a beta multiplier [37], which has a proportional to absolute temperature (PTAT) response. By using a polysilicon resistor R_{poly} and suitable sizing for M_{P1} and M_{P2} the temperature coefficient was slightly adjusted to the desired value. As the body of the PMOS transistor M_{P2} can be tied to source, having the resistor R_{poly} on the PMOS side allows for avoiding the body effect [36], without the need for an isolated/triple-well NMOS transistor. A small PMOS transistor M_{SU}, controlled by a digital start-up signal $S_{U}$, can be used for starting up the core in case of a stable operating point occurring near $I_{core} = 0$. At startup, $M_{SU}$ doesn’t pull the PMOS gates down to ground but one threshold voltage higher, limiting the startup current. Furthermore, under normal operation, the leakage of $M_{SU}$ is very small due to positive gate-source voltage.

The trimmable leakage-compensated sink comprises 6 groups, each consisting of a main sink transistor $M_{S_i}$ and an equal leakage sink transistor $M_{L_i}$. Groups 2 to 5 are binary weighted using unit transistors ($M_{S_i} = M_{L_i} = 2^{i-2} \cdot M_{unit}, i \in 2...5$) and are matched to the core NMOS transistors ($M_{S1} = M_{N2} = 5M_{unit}$), enabling accurate linear trimming. Groups 0 and 1 are equal in size, both half the unit transistor size ($M_{S0} = M_{L0} = M_{S1} = M_{L1} = 0.5M_{unit}$), resulting in less accurate linear trimming, due to worse matching with Groups 2 to 5. However, redundancy in the smallest group enhances the expected accuracy, compared to not having Group 0 at all. This is because it is probable that at least one group of Groups 0 and 1 is more accurate than their expected average accuracy. In addition, using half the unit transistor size as LSB a) reduces the number of total unit transistors from $2^{5-1}$ to $2^{4+1}$ (of which two are half the unit transistor size), and b) allows for a crucially larger unit transistor size, for a given area, to enhance matching.

Each group i is controlled only by bit $B_{Si}$ (and its inverse $B_{Bi}$). As transistor $M_{S_i}$ is disabled through its gate, the corresponding leakage transistor $M_{L_i}$ is enabled through its drain. After mirroring $M_{L_i}$ drain current through $M_{P3}: M_{P4} = 1$, the resulting output current becomes

\[ I_{bias} = I_{sink} - I_{leakcomp} = I_{ideal} + \sum_{i \in D} [I_{S_i, leak} - I_{L_i, leak}] \]

where $I_{ideal}$ is the ideal desired output current, D is the set of indices of disabled groups, and $I_{S_i, leak}$ and $I_{L_i, leak}$ are the currents of a disabled $M_{S_i}$ and $M_{L_i}$, respectively. The Currents $\sum_{i \in D} I_{S_i, leak}$ and $\sum_{i \in D} I_{L_i, leak}$ follow each other over PVT corners and trim word $B_{K}$ values, resulting in leakage compensation: $I_{bias} \approx I_{ideal}$.

The Simulation result for the proposed leakage-compensated bias current generator is presented in Fig. 6 (b), and the corresponding result without the leakage-compensation is shown in Fig. 6 (a). The curve groups consist of simulation results with the lowest trim word 1 (nominally 1.8 nA) and the highest trim word 32 (54 nA), at 6 CMOS corners. The curves have been normalized to room temperature, to show that their temperature coefficient
spread is enhanced roughly 10x from 0.29–0.76 %/°C without the leakage compensation to 0.26–0.31 %/°C with leakage compensation, which, based on simulations, is within acceptable limits to match well enough with the desired value, 0.28 %/°C, which gives the least temperature dependency for the OTA performance. The simulated power consumption of the proposed circuit varies between 43–105 nW, over the trim word range, of which the leakage compensation circuit consumes only 68–281 pW.

E. Capacitors

Configurability for a wide range of capacitive sensors is ensured by using tunable capacitors in the SC circuit, namely capacitor banks $C_{\text{ref}}$ and $C_{f}$. As can be seen from Eq. (1), for a given $V_{\text{out}}$ range, absolute values of $C_{\text{ref}}$ and $C_{f}$ define the midpoint and the magnitude of the allowed $C_{\text{sen}}$ range, respectively. As can been from Eq. (3), in the resistive sensor mode, the allowed $R_{\text{sen}}$ range is determined by capacitor ratios instead of absolute values and, in addition, by the tunable current reference $I_{\text{ref}}$, denoting a well-controlled transfer function and an additional degree of freedom compared to the capacitive sensor mode. Therefore, the capacitor banks $C_{\text{ref}}$ and $C_{f}$ are designed based on the capacitive sensor mode requirements, as requirements posed by the resistive sensor mode are considerably more relaxed.

Increasing capacitor bank resolution increases flexibility in choosing the midpoint of the allowed $C_{\text{sen}}$ range (through choosing $C_{\text{ref}}$), and in choosing the magnitude of the allowed $C_{\text{sen}}$ range (through choosing $C_{f}$). Equivalently, for a given sensor element, increase the capacitor bank resolution enhances flexibility for maximizing sensitivity without saturating the interface circuit. In addition, it increases flexibility for compensating capacitor process variation and mismatch, and sensor element sample-to-sample variation. On the other hand, higher capacitor bank resolution denotes higher parasitic capacitance, switch leakage, routing complexity and area overhead. Process variation and mismatch of the on-chip capacitors and tolerances of the capacitive sensor elements need to be taken into account as parameters when optimizing the capacitor bank resolution, range and structure.

In this design, $C_{\text{ref}}$ and $C_{f}$ are implemented as 8-bit and 5-bit capacitor banks with the capacitance ranges of 1.96–500 pF and 1.96–60.8 pF, respectively. To reduce the above-mentioned drawbacks, both the capacitor banks have been divided into LSB and MSB binary capacitor matrices, consisting of 1.96-pF and 15.7-pF unit capacitors, respectively. The LSB matrix includes also two unit capacitors for implementing the fixed $C_{\text{res}}$ (3.92 pF). Fig. 7 shows the layout floor plan of the capacitor bank matrices. The unit capacitors are placed in a manner to minimize the effects of mismatch, by using the common centroid layout technique, and to simplify the layout routing. Dummy capacitors are placed around the MSB and LSB matrices to keep each unit capacitor identical. The requirement for implementing the $C_{\text{cs}}$ is more flexible, since the matching does not need to be considered. Therefore, it is easily implemented as a 100-pF single capacitor cell.

F. Non-Overlapping Clock Phase Generator

To ensure accurate charge transfer, the SC front-end switches are controlled using non-overlapping clock phases clk1 and clk2, which are generated from the clock signal clk. In addition, clock phase clk1a whose falling edge is advanced in time, compared to the falling edge of clk1, is required.

The non-overlapping clock phase generator and the resulting timing diagram are shown in Fig. 8. The dark grey delaying buffers $D_{\text{h}}$ determine the non-overlapping time between clk1 and clk2. In addition, clock phase clk1a whose falling edge is advanced in time, compared to the falling edge of clk1, is required.

The non-overlapping clock phase generator and the resulting timing diagram is shown in Fig. 8. The dark grey delaying buffers $D_{\text{h}}$ determine the non-overlapping time between clk1 and clk2. Similar delaying inverters $D_{s}$ determine the delay of the falling edges of clk1 and clk2, compared to their advanced edge counterpart clk1a and clk2a, respectively. The timing diagram shows the resulting front-end output signal $V_{\text{out}}$ timing. The output has settled properly and is valid...
inside the time window denoted by the grey area. The arrows denote the time instant that is used for output sampling in the measurements.

The Clock phase clk2a is not used in the presented setups of the UMSI. However, the related delaying inverter D2 and the driving branches are needed to achieve symmetrical clk1 and clk2 timing, by matching the clock phase signal paths and loading thereof, respectively. The parts and signals that are not necessary, are drawn in light grey.

All clock phase outputs are driven by inverting clock drivers that have high driving capability and equal rise and fall times. In addition, as the transmission gate switches require both control signal polarities, accurate inverted counterparts (clk̅) of all the above output clock phase signals, with minimized delay, are required.

G. Other Circuit Blocks

The memory register provides static trim bits required by the UMSI to operate in different configurations. It contains D-type flip-flops, arranged to eight 8-bit registers, that are written using the SPI.

The on-chip measurement buffer amplifier is used not to load the UMSI with the measurement setup. It is implemented using an amplifier identical to the front-end amplifier, used in unity gain configuration.

III. Measurement Results

The UMSI chip was fabricated in a 0.18-µm CMOS process with a total area of 1.89 mm² including the pads. The die microphotograph of the interface chip is shown in Fig. 9. Common centroid layout techniques were utilized in order to reduce the effects of mismatch. A separate on-chip supply domain was used for digital circuits (NOL clock phase generator, MUXs) to reduce the supply noise coupled to the analog blocks. The supply domains were connected together off-chip. Sensitive signal paths such as the capacitive sensor element nodes were protected by surrounding them with ground paths. Data to the memory registers was written through an SPI interface.

There was an unexpectedly high bonding pad leakage arising from the ESD protection diodes, resulting in incorrect operation with a combination of small Csen and low fclk values. Hence, the applied fclk was chosen based on the utilized sense capacitance range. l sensed was adjusted according to fclk and Csen range to ensure a long enough linear settling period and the lowest possible power consumption. The output voltage of the interface was measured with a high resolution 10 MS/s digital oscilloscope. The signal was captured in continuous time while the interface was operating in discrete time at fclk. The resulting signal was sampled in digital post-processing at the chosen fclk (one sample per clock cycle), at the rising edge of clk, as denoted by arrows in Fig. 8(b), to find the actual signal extracted by the UMSI circuit. In order to find the DC transfer curve, multiple signal samples were averaged. It is notable that no averaging was applied in noise performance evaluation. VDD and Vref were generated using a high-precision external power supply.

A. Characterization With Test Capacitors and Resistors

To characterize the UMSI, we used test capacitors and resistors as the sensing elements, because this characterization would be complicated using the actual sensor elements. First, those test capacitors and resistors were measured with a Smart Tweezers ST-5S LCR meter and a HP 34401A multimeter, respectively, for reference, and then, they were connected to the UMSI to obtain a capacitance-to-voltage and resistance-to-voltage mapping.

The UMSI was characterized in capacitive mode by measuring its operation in three separate ranges, given in Table I, within the overall capacitance range of 0.6–550 pF. These specific ranges were chosen to match the capacitance ranges of the target sensor elements [22], [23], as well as to verify operation at the minimum and maximum of the overall range.
of the UMSI in the capacitive mode. The parameter values and a summary of the measurements can be found in Table I. The values of $C_{\text{ref}}$ and $C_t$ are estimated through two-point calibration. The maximum capacitance range that the interface can cover in one setup is equal to the maximum value of $C_t$, i.e. 62.2 pF.

Fig. 10 illustrates the resulting measured output voltage of the UMSI, sensitivity $G_Y$, and linearity error in capacitive mode for three chosen ranges from the overall range of $C_{\text{sen}} = 0.6-550$ pF. The simulation results are shown to demonstrate the agreement between the measured and simulated values. Linearity evaluation was limited by the accuracy of the measurement setup.

Fig. 11 illustrates the measured output voltage of the UMSI, sensitivity $G_Y$, and linearity error in resistive mode for three chosen ranges from the overall range of $R_{\text{sen}} = 3.7-5100$ kΩ with (a) $R_{\text{sen}} = 0.6-15$ kΩ (b) $R_{\text{sen}} = 9.1-137$ kΩ. The simulation results are shown to demonstrate the agreement between the measured and simulated values. Linearity evaluation was limited by the accuracy of the measurement setup.

The linearity evaluation of the interface was limited by the accuracy of the test capacitance measurement instrument and the measurement setup. The sensitivity and linearity evaluation of the UMSI based on the simulation results are also shown in Fig. 10. The measured linearity of the UMSI is well matched with the simulation results. The difference between the simulated and the measured ranges and sensitivity $G_Y$ is mainly because of the difference between the simulated and realized $C_{\text{ref}}$ and $C_t$ due to process variation and mismatch (e.g. max $C_{\text{ref,sim.}} = 500$ pF; while max $C_{\text{ref,real.}} = 517$ pF). In order to characterize the circuit in resistive mode, its operation was again measured in three separate ranges, given in Table I, within the overall resistance range of 3.7-5100 kΩ. These specific ranges were chosen so as to match the resistance ranges of the target sensor elements [24], [25]. As discussed earlier, an external current reference $I_{\text{ref}}$ was used to have more flexibility in the measurement. However, current reference can also be easily implemented on-chip [38]. The parameter values and a summary of the measurements can be found in Table I. Fig. 11 illustrates the measured output voltage of the UMSI, sensitivity $G_Y$, and linearity error as a function of sensing resistance for the three input ranges. The transfer curve of each measurement range is linear to at least 13.5 bits. As was the case for capacitive mode, the evaluation of the linearity was limited by the accuracy of the test resistance measurement instrument. Fig. 11 also depicts the sensitivity and linearity evaluation of the UMSI based on the simulation results. The measured linearity of the UMSI is again well matched with the simulation results. The difference between the simulated and the measured sensitivity $G_Y$ is mainly due to the difference between the simulated and realized $C_{\text{ref}}$ and $C_t$.

Fig. 12(a) shows the measured output voltage of the UMSI for the time duration of 500 clock cycles ($f_{\text{clk}} = 15$ kHz) for $C_{\text{sen}} = 0.6$ pF. The average or mean value of such a sequence represents the reduced-noise data and the practical result. The standard deviation $\sigma$ is 400 $\mu$V, which describes the effective rms noise value. A similar test was also performed for the $V_{\text{ref}}$ and $V_{\text{DD}}$ used in our measurements, and the results are shown in Fig. 12. The rms noise is 926 $\mu$V for the $V_{\text{ref}}$ and 944 $\mu$V for the $V_{\text{DD}}$. The rms noise values of the UMSI as a function of $C_{\text{sen}} = 0.6-15$ pF and $R_{\text{sen}} = 3.7-200$ kΩ are shown in Fig. 13.
The tolerances range (±15%) extracted from [23].

Using data from (a), typical capacitance values of the sensor element calculated capacitance values of the tested sensor element are set to 143 pF and 46.5 pF, respectively. The permittivity (εr) of the foil, and since capacitance is directly proportional to the εr, therefore, the capacitance of the sensor increases.

The testing was performed using a f_{wk} of 1 kHz. The values of C_{ref} and C_f were set to 143 pF and 46.5 pF, respectively. The sensor was tested in a LabEvent L. C34/40 climate chamber capable of humidity and temperature control. The chamber was also used for monitoring the relative humidity (RH) using its internal sensor. The RH of the chamber was varied from 10 to 90%. The temperature of the chamber was maintained at 25°C.

Fig. 14(a) shows the measured output voltage of the UMSI as a function of RH. The capacitance of the sensor was determined by substituting the measured output voltage of the UMSI and the given C_{ref} and C_f in Eq. (2). The calculated capacitance value of the tested sensor as a function of RH is shown in Fig. 14(b). The capacitance values as a function of RH of the sensor element extracted from [23] are superimposed on Fig. 14(b). Note that [23] only provides a typical capacitance as a function of RH graph, and as is mentioned in the datasheet, the capacitance values may have ±15% tolerances. The power consumption of the interface was 2.4 μW from a 1.2 V supply.

C. Capacitive Proximity, Gesture and Touch Sensor

The proposed sensing system, consisting of the UMSI and a capacitive sensor element, converts displacement of the object above the device as well as contact with it to a voltage signal, so that the system offers proximity, gesture and touch-sensing capabilities. These capabilities are achieved using a simple sensor element composed of two coplanar copper electrodes, etched on a prototype single-sided PCB. The sensor element is shown in Fig. 15 (a). These electrodes were connected using wires to the UMSI that was mounted on the test PCB. In order to reduce the parasitic capacitance, the length of the wires was kept short, since the wires are also sensitive to the displacement of the object as well as ambient interference.

Fig. 15 (b) illustrates the conceptual proximity-sensing mechanism for this experiment, which is based on the measurement of an electric field between the two electrodes of the sensor. Without the presence of an object, the electric field is above the device as well as contact with it to a voltage signal, so that the system offers proximity, gesture and touch-sensing capabilities. These capabilities are achieved using a simple sensor element composed of two coplanar copper electrodes, etched on a prototype single-sided PCB. The sensor element is shown in Fig. 15 (a). These electrodes were connected using wires to the UMSI that was mounted on the test PCB. In order to reduce the parasitic capacitance, the length of the wires was kept short, since the wires are also sensitive to the displacement of the object as well as ambient interference.

Fig. 15 (b) illustrates the conceptual proximity-sensing mechanism for this experiment, which is based on the measurement of an electric field between the two electrodes of the sensor. Without the presence of an object, the electric field is...
field is contained between the electrodes of the sensor. When an object with impedance $Z_b$ to ground (e.g., a user’s hand) approaches the sensing electrodes, it affects the near electric field, and consequently changes the equivalent mutual capacitance ($C_{m}$) between the electrodes of the sensor, and therefore, the displacement of an object can be detected.

In order to investigate the capabilities of the sensing system and to observe its response characteristics in real application scenarios, different prototype experiments were conducted. All the experiments were performed using the same $f_{ck}$ of 15 kHz, and the values of $C_{ref}$ and $C_f$ were tuned to 2 pF and 4 pF, respectively. The objects being detected were a 4 cm $\times$ 7 cm copper plate, and the experimenter’s hand. In the first and second experiments, the copper plate was used as the approaching object. First, it was connected to the ground node of the power supply, and, second, it was connected to the hand using a wire. The vertical distance of the object to the sensor element was changed from 0.2 cm to 20 cm in successive steps. The output voltage of the UMSI was measured after each step. In the third experiment, the object to be detected was the hand of the experimenter, which was moved above the sensing electrodes at distances of between 0.8 cm and 20 cm. The resulting output voltages of the UMSI as a function of the vertical distance of the object to the sensor element for these three experiments are shown in Fig. 16(a). The capacitance of the tested sensor was determined by substituting the measured output voltage of the UMSI and the given $C_{ref}$ and $C_f$ in Eq. (2). Fig. 16(b) shows the calculated capacitance value of the sensor as a function of the vertical distance of the object to the sensor element. The power consumption of the system was 0.83 $\mu$W from a 1.2 V supply.

In order to further investigate the capabilities of the system, the output voltage of the interface was measured when a hand performed different gestures on the sensor element, including: approaching the sensor, sweeping horizontally over the sensor, tapping the sensor, and touching the sensor. The measured output voltage of the UMSI as a function of time is shown in Fig. 17(a). The sensor element was very sensitive to the ambient interference, and consequently, the measured signal was noisy. Therefore, the measured signal was filtered using a 10-point moving average filter. Fig. 17(b) shows the filtered signal as a function of time. As mentioned earlier, the sensor system offers both proximity and touch-sensing capabilities. When the experimenter’s hand tapped or touched the electrode of the sensor connected to the padbot, the output voltage of the UMSI decreased. This reduction can be interpreted as an increase in the sensed capacitance according to Eq. (2). Here, the human body affects the equivalent mutual capacitance ($C_m$) between the two electrodes of the sensor, resulting in an increase in the total effective sensing capacitance.

D. Photoconductive Sensor

The sensor discussed in this section is a photoconductive cell [24]. It consists of a thin film of photoconductive material deposited on a ceramic substrate. Increasing illumination
allows more current to flow, and consequently, the resistance of the sensor decreases. Therefore, the presence and absence of light can be detected by measuring the resistance of the sensor.

The testing was performed using a clock of 1 kHz. The values of $C_{\text{ref}}$ and $C_f$ were set to 2 pF and 5.9 pF, respectively. An Amprobe LM-120 light meter was used to measure the light intensity. In order to increase the sensitivity of the measurement, the experiment was performed in two steps. First, the $I_{\text{ref}}$ was set to 2.75 $\mu$A, and the illuminance was varied from 0.83 lux to 39.2 lux. Second, the $I_{\text{ref}}$ was set to 0.11 $\mu$A, and the illuminance was varied from 0.05 lux to 0.71 lux. The measured output voltage of the UMSI as a function of illuminance for the first and second experiments are shown in Fig. 18(a) and 19(a), respectively. The resistance of the sensor was determined by substituting the measured output voltage of the UMSI and the given $C_{\text{ref}}$ and $C_f$ in Eq. (4). The calculated resistance value of the tested sensor as a function of illuminance for the first and second experiments are shown in Fig. 18(b) and 19(b), respectively.

To demonstrate the entire measured illumination range and improve readability, the resistance of the sensor as a function of illuminance from both experiments shown in Fig. 18 and 19 are combined, and shown in logarithmic scale in Fig. 20. The wide dynamic range of the interface allowed the resistance of the sensor to be measured by around three orders of magnitude as the illuminance varied from 0.05 lux to 39.2 lux. The power consumption of the UMSI, including $I_{\text{ref}}$, was 3.56 $\mu$W for the first experiment, and 0.39 $\mu$W for the second experiment, both from a 1.2 V supply.

### E. Resistive Force Sensor

The sensor described in this section is a single-zone force-sensing resistor. It is a robust polymer thick film (PTF) device that shows a decrease in resistance with increasing force applied to the surface of the sensor [25].

The testing was performed using a clock of 1 kHz and the $I_{\text{ref}}$ was set to 2.75 $\mu$A. The values of $C_{\text{ref}}$ and $C_f$ were set to 2 pF and 5.9 pF, respectively. An ESM303 test stand was used to apply force to the sensor, and a MARK-10 force gauge M7-5 was used to measure the applied force. The applied force was varied from 0.32 Newton (N) to 17.79 N. The measured output voltage of the UMSI as a function of force is shown in Fig. 21(a). The resistance of the sensor was determined by substituting the output voltage of the UMSI and the given $C_{\text{ref}}$ and $C_f$ in Eq. (4). The calculated resistance value of the tested sensor as a function of force is shown in Fig. 21(b). The power consumption of the UMSI, including $I_{\text{ref}}$, was 3.56 $\mu$W from a 1.2 V supply.

### F. Comparison

Table II summarizes the performance of the proposed sensor interface and compares it with the previously published capacitive, resistive, and capacitive-resistive sensor interfaces. The UMSI has the second highest linearity and the second widest overall capacitance and resistance range, while having an ultra-low-power consumption. Such performance is achieved by employing the wide range tunable capacitor bank, the low-power amplifier with flexible properties, the leakage-compensated wide-trimming-range bias current generator, and the system level optimization of the circuit. Most of the systems presented in Table II are complete systems with digital or analog output. Therefore, for a fair and reasonable comparison, the UMSI should be compared with their analog front-end when it is applicable.
The proposed proximity, gesture and touch-sensing system can detect the vertical movement of an object up to 15 cm away from the sensor element, while consumes only 0.69 µA. The previously reported single-plate [31] and dual-plate [32] capacitive proximity sensing systems provide a lower detectable range, while consuming 85 µA and 370 µA, respectively, which is >10× higher than the current consumption of the system presented in this paper. As stated before, the proposed system also offers gesture and touch-sensing capabilities.

### IV. Conclusion

This paper presents an ultra-low-power interface circuit implemented in a 0.18 µm CMOS process technology. Unlike single-sensor interface circuits that are tailored towards dedicated sensors for specific applications, the proposed universal interface circuit is flexible and highly configurable, and therefore, can be integrated into emerging multi-sensor technologies such as IoT and AmI.

The results show that the UMSI is able to interface various sensors within an overall capacitance range of 0.6–550 pF and a resistance range of 3.7 kΩ–51 MΩ, while consuming only 0.39–3.56 µW, with a linearity of more than 13.5 bits. The UMSI is also characterized by different sensors, including humidity, photoconductive, and force. The experimental results demonstrate the capabilities and performance of the interface in real application scenarios under different environmental conditions.

A capacitive proximity, gesture and touch-sensing system is also presented in this paper. The developed system, consisting of the UMSI and a simple sensor element, can sense multiple gestures, displacement of an object up to 15 cm from the sensing element, and touching the sensing element. The proposed system consumes only 0.83 µW from a 1.2 V supply.

The competitive performance makes the UMSI a suitable candidate for energy-constrained and high accuracy capacitance and resistance sensing applications.

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### REFERENCES


