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Feijoo, Pedro C.; Pasadas, Francisco; Bonmann, Marlene; Asad, Muhammad; Yang, Xinxin; Generalov, Andrey; Vorobiev, Andrei; Banszerus, Luca; Stampfer, Christoph; Otto, Martin; Neumaier, Daniel; Stake, Jan; Jimenez, David

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Published in:
Nanoscale Advances

DOI:
[10.1039/c9na00733d](https://doi.org/10.1039/c9na00733d)

Published: 01/09/2020

Document Version
Publisher's PDF, also known as Version of record














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Please cite the original version:
Feijoo, P. C., Pasadas, F., Bonmann, M., Asad, M., Yang, X., Generalov, A., Vorobiev, A., Banszerus, L., Stampfer, C., Otto, M., Neumaier, D., Stake, J., & Jimenez, D. (2020). Does carrier velocity saturation help to enhance $f(\text{max})$ in graphene field-effect transistors? *Nanoscale Advances*, 2(9), 4179-4186.
<https://doi.org/10.1039/c9na00733d>

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Cite this: *Nanoscale Adv.*, 2020, 2, 4179

Does carrier velocity saturation help to enhance f_{\max} in graphene field-effect transistors?†

Pedro C. Feijoo, *^a Francisco Pasadas, ^a Marlene Bonmann, ^b Muhammad Asad, ^b Xinxin Yang, ^b Andrey Generalov, ^c Andrei Vorobiev, ^b Luca Banszerus, ^d Christoph Stampfer, ^d Martin Otto, ^e Daniel Neumaier, ^e Jan Stake ^b and David Jiménez ^a

It has been argued that current saturation in graphene field-effect transistors (GFETs) is needed to get optimal maximum oscillation frequency (f_{\max}). This paper investigates whether velocity saturation can help to get better current saturation and if that correlates with enhanced f_{\max} . We have fabricated 500 nm GFETs with high extrinsic f_{\max} (37 GHz), and later simulated with a drift–diffusion model augmented with the relevant factors that influence carrier velocity, namely: short-channel electrostatics, saturation velocity effect, graphene/dielectric interface traps, and self-heating effects. Crucially, the model provides microscopic details of channel parameters such as carrier concentration, drift and saturation velocities, allowing us to correlate the observed macroscopic behavior with the local magnitudes. When biasing the GFET so all carriers in the channel are of the same sign resulting in highly concentrated unipolar channel, we find that the larger the drain bias is, both closer the carrier velocity to its saturation value and the higher the f_{\max} are. However, the highest f_{\max} can be achieved at biases where there exists a depletion of carriers near source or drain. In such a situation, the highest f_{\max} is not found in the velocity saturation regime, but where carrier velocity is far below its saturated value and the contribution of the diffusion mechanism to the current is comparable to the drift mechanism. The position and magnitude of the highest f_{\max} depend on the carrier concentration and total velocity, which are interdependent and are also affected by the self-heating. Importantly, this effect was found to severely limit radio-frequency performance, reducing the highest f_{\max} from ~ 60 to ~ 40 GHz.

Received 20th November 2019
Accepted 23rd July 2020

DOI: 10.1039/c9na00733d

rsc.li/nanoscale-advances

Introduction

The development of new-generation radio-frequency (RF) electronics enables extending the range of advanced applications within the areas of communication, security imaging, quality

control, medicine *etc.*¹ For the sustainable development, new materials with enhanced electronic properties are required. Graphene is considered as a promising channel material for RF field-effect transistors due to its intrinsically high charge carrier mobility (up to $2 \times 10^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and saturation velocity ($4 \times 10^7 \text{ cm s}^{-1}$).^{2–6} However, RF performance of the graphene field-effect transistors (GFETs) was limited until recently by several factors, for example, a relatively high drain conductance due to zero bandgap, a high graphene/metal contact resistance and the extrinsic carrier scattering by charged defects.^{7–11} Continuous efforts in the study of GFETs have resulted in an important improvement of the RF figures of merit (FoMs): the extrinsic cutoff (transit) frequency ($f_{T,x}$) and maximum frequency of oscillation (f_{\max}).^{12–17} This enhancement has been enabled, in particular, by the use of GFET models, which have allowed for clarifying and overcoming RF performance limitations.^{18–27} Recently, values of $f_{T,x} = 34$ GHz and $f_{\max} = 37$ GHz for GFETs with chemical vapor deposited graphene and a gate length (L_g) of 500 nm were reported by some of us.²⁸ These RF FoMs outperform the ones obtained in other graphene-based transistors with similar L_g , although higher values were achieved for shorter L_g .²⁹ Furthermore, these values of $f_{T,x}$ and f_{\max} surpassed

^aUniversitat Autònoma de Barcelona, 08193 Cerdanyola del Vallès, Spain. E-mail: PedroCarlos.Feijoo@uab.cat

^bChalmers University of Technology, SE-41296 Gothenburg, Sweden

^cAalto University, FI-00076 Helsinki, Finland

^d2nd Institute of Physics, RWTH Aachen University, 52074 Aachen, Germany

^eAdvanced Microelectronic Center Aachen, AMO GmbH, 52074 Aachen, Germany

† Electronic supplementary information (ESI) available: Section S1 details fabrication and characterization of graphene devices used in this work. Then, Sections S2 and S3 present the mathematical modelling for the simulation of the DC characteristics of GFETs and calculation of carrier velocity in graphene. Experimental and simulated transfer characteristics of GFETs are represented in Section S4. Next, Section S5 includes the mathematical expressions used to extract small-signal parameter and RF performance from the simulated DC characteristics. Section S6 presents the measurements of the parasitic capacitances of the GFET. Section S7 shows the carrier concentration distribution at biases where the magnitude of transconductance is maximized. Section S8 delves deep into the effect of interface traps on GFET characteristics and RF performance. Finally, Section S9 investigates the RF performance degradation caused by self-heating. See DOI: 10.1039/c9na00733d



those of the best Si MOSFETs with similar gate lengths.³⁰ The achievement has been obtained by a combination of different improvements of the GFET design and fabrication process that have resulted in high saturation velocity, low contact resistance, and reduced extrinsic pad capacitances.

A question that remains to be answered is whether operating the GFET in a saturation velocity regime actually helps to get the highest f_{max} . The resolution to this problem needs a simulation tool that considers the factors that affect the current saturation, namely, short-channel effects, velocity saturation effects, and self-heating effects (SHE). Our preliminary analysis indicated that these effects can be significant when a GFET works at relatively high drain fields, above $1 \text{ V } \mu\text{m}^{-1}$. In previous works, a self-consistent simulator that accounted for short-channel and velocity saturation effects was developed to investigate the RF performance and scalability of GFETs.^{24,25} That simulator has been updated in the present work including the SHE with two purposes: to study the DC and RF performance of the prototype 500 nm GFET presented in ref. 28 and to explore whether there is still room for f_{max} improvement by exploiting the saturation velocity regime.

This paper thoroughly studies the impact of drain current saturation on RF performance as the interplay between carrier concentration (the gradient of which triggers the diffusion current) and velocity, which has only been slightly addressed before.²¹ To investigate GFET performance, we follow an approach that consists firstly in solving the drift-diffusion equation self-consistently with the two-dimensional Poisson's equation to get the DC characteristics.²⁴ This set of equations is, in turn, coupled with the heat transfer equation that models the SHE. Then RF performance is obtained from a quasi-static small-signal model, whose parameters are extracted from linearization of the DC simulations.²⁵ Such a methodology is thoroughly described in Methods. The combined analysis of DC and RF simulations allows us to assess the influence of graphene electrical properties as the saturation velocity and low-field mobility, and other limiting factors as, for instance, the contact resistance, the interface traps and extrinsic capacitances. Thereby, we have obtained insights on the mechanisms defining the DC and RF performance of GFETs, which are discussed in Results and discussion. Particularly, we have addressed the question whether velocity saturation can help to get better current saturation and if that correlates with enhanced f_{max} . Finally, the conclusions are drawn in the Conclusions section.

Methods

Device structure and description of the self-consistent simulator

To investigate the bias dependence of RF performance and its relation with current saturation, we have numerically investigated the prototype GFET with high extrinsic $f_{T,x}$ and f_{max} described in ref. 28. Fig. 1 shows the GFET scanning electron microscope (SEM) image of the device and a schematic view of one of the two fingers. The GFET gate length and total gate width were $L_g = 500 \text{ nm}$ and $W_g = 2 \times 15 \mu\text{m}$, respectively. The

length of each ungated region of the channel was $L_{\text{ung}} = 100 \text{ nm}$. The graphene layer was encapsulated between insulating layers of Al_2O_3 and SiO_2 with thicknesses of $t_t = 22 \text{ nm}$ and $t_b = 1 \mu\text{m}$, respectively. The relatively thick SiO_2 allows for reduction of the parasitic pad capacitances.²⁸ High-resistivity (larger than $10 \text{ k}\Omega \text{ cm}$) silicon was used as substrate with the aim of minimizing the substrate-related microwave loss in the GFET contact pads and transmission lines of the prospective devices.³¹ Details on the GFET fabrication are included in Section S1 of the ESI.†

The GFET was simulated using the method described in ref. 24 and 25, which consists in solving self-consistently 2D Poisson's equation and 1D drift-diffusion transport equation. The dashed rectangle in Fig. 1(b) encloses the active area of the transistor and corresponds to the domain where the Poisson's equation is solved. The simulator obtains the stationary distributions of graphene electrical parameters along the channel as a function of the voltages applied to the gate-source and drain-source terminals (V_{gs} and V_{ds} , respectively). Specifically, it is possible to get the local parameters such as the charge carrier concentration for both electrons (n) and holes (p), the carrier field-dependent mobility (μ), the separate currents and carrier velocities driven by both drift (v_{drift}) and diffusion mechanisms (v_{diff}), the Dirac energy ($E_D = -q\psi$) and the quasi-fermi energy ($E_F = -qV$). The details of the simulator and the different carrier velocity definitions used in this work can be found in Sections S2 and S3, respectively, of the ESI.† Key parameters as the flat-band voltage (V_{gs0}), the residual charge carrier concentration (ρ_0), the low-field mobility (μ_{LF}), and the contact resistance (R_c) were extracted from measured low- V_{ds} transfer curves ($I_{\text{ds}}-V_{\text{gs}}$) with holding time of 1 s at each bias point (see Section S4 of the ESI†). After that, we fitted the measured output characteristics ($I_{\text{ds}}-V_{\text{ds}}$), which were obtained upon application of a holding time of 30 s per measured point. That time is long enough for the trapping/de-trapping processes to stabilize at high fields.³² The fitting parameters are the interface trap density (N_{it}), the energy of optical phonons ($\hbar\Omega$), whose emission limits carrier drift velocity, and the effective thermal resistance (R_{th}). The latter will be discussed below. The model for the saturation velocity v_{sat} is given by:³³

$$v_{\text{sat}}(y) = \frac{2Q}{\pi\sqrt{\pi\rho_{\text{sh}}(y)}} \sqrt{1 - \frac{Q^2}{4\pi v_F^2 \rho_{\text{sh}}(y)}} \frac{1}{N_{\text{OP}} + 1} \quad (1)$$

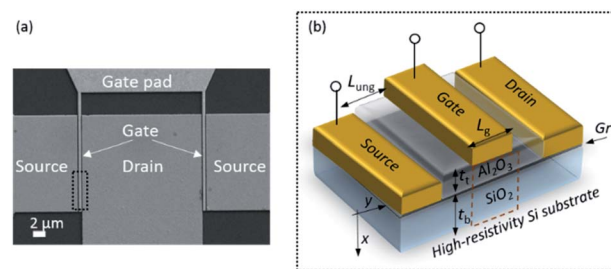


Fig. 1 (a) GFET SEM image and (b) schematic view (not drawn to scale) of the gate region indicated in (a). The dashed rectangle encloses the domain where the Poisson's equation is solved.



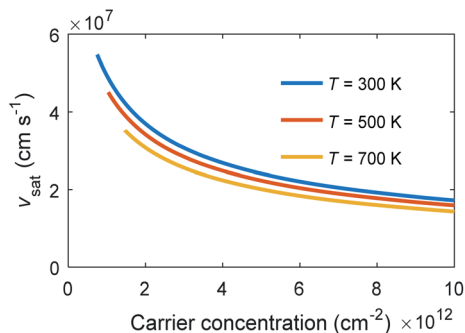


Fig. 2 Carrier saturation velocity as a function of the carrier concentration for different temperatures. The value of the optical phonon energy used has been $\hbar\Omega = 0.10$ eV.

where T is the temperature, and $\rho_{\text{sh}}(y) = n(y) + p(y)$ is the local carrier concentration at the position y in the channel. The phonon occupation N_{OP} depends on temperature as:

$$N_{\text{OP}} = \frac{1}{\exp\left(\frac{\hbar\Omega}{kT}\right) - 1} \quad (2)$$

Eqn (1) and (2) show that saturation velocity strongly depends on carrier concentration. Moreover, an increase in temperature slightly decreases v_{sat} . These dependencies can be seen in Fig. 2, where v_{sat} has been represented for typical values of carrier concentration at several temperatures.

We have used the following equation to model the field-dependent mobility $\mu(y)$ as a function of the local electric field and saturation velocity, and thereby, also on $\rho_{\text{sh}}(y)$ and T :

$$\mu(y) = \frac{\mu_{\text{LF}}}{\left\{1 + \left[\left(\frac{\mu_{\text{LF}}}{v_{\text{sat}}(y)} \left|\frac{\partial\psi}{\partial y}\right|\right)^\gamma\right]\right\}^{\frac{1}{\gamma}}} \quad (3)$$

Here, a value of 1 has been used for the parameter γ , consistently with numerical studies of electronic transport in single layer graphene relying on Monte Carlo simulations.³⁴

Unlike our previous works, we have included the SHE in the self-consistent loop of the GFET simulator. This means that we assume that the temperature of the GFET rises because the heat dissipated in graphene by the Joule effect finds difficulty to spread out of the device through the surrounding layers. By using the simplest thermal model, the temperature of the graphene channel can be expressed as:

$$T - T_0 = R_{\text{th}} P_{\text{dis}} \quad (4)$$

where $T_0 = 300$ K is the temperature of the heat sink, assumed to be the environment temperature of the transistor and R_{th} is an effective thermal resistance that embraces all the paths through which the heat is dissipated. P_{dis} is the dissipated power in the GFET, which takes the following form:

$$P_{\text{dis}} = \left| I_{\text{ds}} V'_{\text{ds}} \right| \quad (5)$$

where $V'_{\text{ds}} = V_{\text{ds}} - I_{\text{ds}} R_c$ is the intrinsic drain-to-source voltage. This model considers an average temperature for the whole graphene sheet, so it neglects any local temperature deviation. It also neglects any temperature deviation at the proximities of the contacts, which could be a problem for graphene devices with L_g below 300 nm.³⁵ Our previous measurements indicate that we can neglect the heat dissipated through the gate stack and at the proximity of the contacts,²⁸ so the applied model is expected to work properly for the analyzed device.

Using the values for mobility and carrier concentration obtained in this study we estimate the mean free path (MFP) by the semiclassical model described in ref. 6 in the 10–100 nm range. Since the MFP is much shorter than the source-to-drain length ($L_g + 2L_{\text{ung}}$), it is confirmed that the drift-diffusion transport mechanism is appropriate for describing the electronic transport in the examined GFET. Transistors with shorter channel lengths should be analyzed with ballistic or quantum models, which is beyond the scope of this work.

Small-signal model of the GFET and derived RF performance

For the analysis of the RF performance, we consider the GFET as a two-port network in common-source configuration. The device is characterized by its extrinsic admittance matrix Y . This matrix is calculated in two steps. First, the intrinsic admittance matrix Y' is determined by the intrinsic small-signal equivalent circuit model assuming quasi-static operation.³⁶ Then the extrinsic Y matrix is obtained embedding the intrinsic GFET in a simplified extrinsic circuit of lumped elements, which consists of parasitic resistances at each of the three terminals and parasitic capacitances at both the input and the output ports. Since $t_b \gg t_t$, the back-gate capacitance is much smaller than the top-gate capacitance, so we can neglect the influence of the substrate capacitance in Y' . Tunneling currents through any of the dielectrics are also neglected.

Transconductance g_m and output conductance g_{sd} can be obtained from the derivatives of I_{ds} respect to the intrinsic bias voltages $V'_{\text{gs}} = V_{\text{gs}} - I_{\text{ds}} R_c / 2$ and V'_{ds} , respectively. Then, the small-signal capacitances are determined from the charges associated to each of the terminals (Q_i , with $i = s, d$ or g). They have been defined assuming a charge conserving Ward-Dutton's linear charge partition scheme.³⁶ The transcapacitances $C_{\text{gs}}, C_{\text{gd}}, C_{\text{sd}}, C_{\text{dg}}$ are obtained as the derivative of charge at terminal i with respect to the intrinsic voltage at terminal j , $C_{ij} = -dQ_i/dV'_j$. For the calculation of the small-signal parameters, we assume that the temperature is constant at a given bias point. A full description of the small-signal parameter and extrinsic admittance matrix calculation can be found in Section S5 of the ESI.† Finally, the RF FoMs $f_{T,x}$ and f_{max} are extracted from the current gain and unilateral power gain that result from the Y matrix.³⁷

Results and discussion

First, we reproduced the experimental DC characteristics following the methodology described in Methods. Fig. 3(a) shows the measured output characteristics of the GFET and



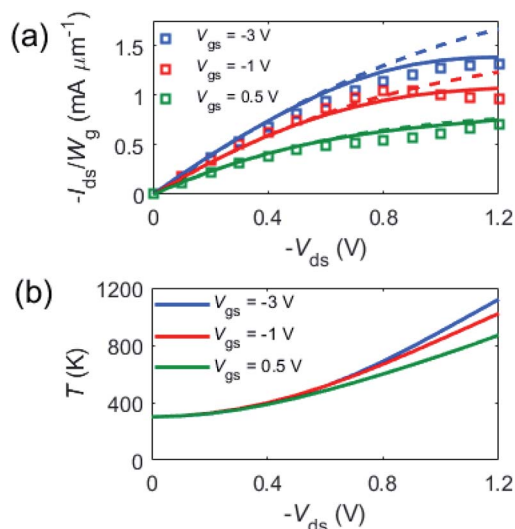


Fig. 3 (a) Measured (squares) and modelled (solid lines) DC output characteristics of a GFET. Dashed lines correspond to the simulated current neglecting SHE. (b) GFET temperature as a function of the drain bias due to self-heating.

their comparison with the simulations, where the parameters used are presented in Table 1. The estimated N_{it} was found to be lower than $10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$, a value below which the influence of interface traps is negligible, as shown in Section S8 of the ESI.† The best fitting value of the R_c is $11 \text{ } \Omega$, which includes the metal/graphene contact resistance at both drain and source together with the access resistances of the ungated graphene regions. Thus, the width specific contact resistivity results in $R_c W_g/2 = 165 \text{ } \Omega \text{ } \mu\text{m}$. The width specific metal/graphene contact resistivity of approximately $90 \text{ } \Omega \text{ } \mu\text{m}$, evaluated applying the drain resistance model to the transfer characteristic, agrees with the value of $95 \text{ } \Omega \text{ } \mu\text{m}$ obtained by transfer length measurements (which exclude access resistance). From the fitting done in Fig. 3(a), we obtained a value of $2.7 \times 10^4 \text{ K W}^{-1}$ for the R_{th} , which agrees with the order of magnitude of calculations based on the model by Pop *et al.*,^{22,33} of around $3\text{--}4 \times 10^4 \text{ K W}^{-1}$. Our simulator also allowed us to calculate GFET temperature as a function of the bias, shown in Fig. 3(b), and ranging between 300 and 1000 K. The simulated temperatures are similar to the ones obtained in previous works analyzing gate leakage current as a thermo-sensitive parameter.³⁸

Table 1 Optimized parameters fitted from current–voltage characteristics

| Parameter | Optimized value |
|---------------|--|
| V_{gs0} | 2.2 V |
| ρ_0 | $2.9 \times 10^{11} \text{ cm}^{-2}$ |
| μ_{LF} | $2.0 \times 10^3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ |
| R_c | 11 Ω |
| N_{it} | $<10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ |
| $\hbar\Omega$ | 0.10 eV |
| R_{th} | $2.7 \times 10^4 \text{ K W}^{-1}$ |

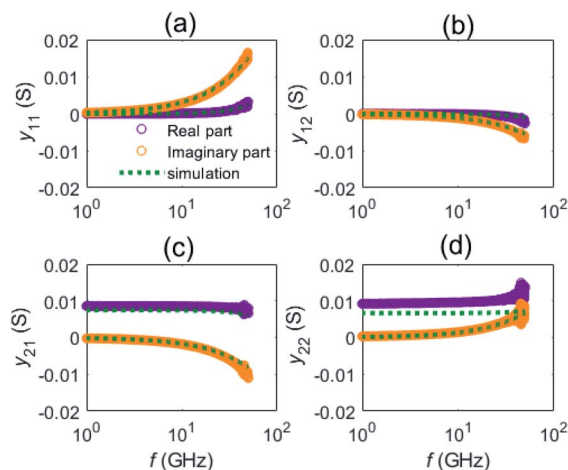


Fig. 4 Measured (circles) and modelled (dotted lines) Y -parameters as a function of the frequency for a GFET biased at $V_{ds} = -1.1 \text{ V}$ and $V_{gs} = 0.5 \text{ V}$, corresponding to the highest measured $f_{T,x} = 34 \text{ GHz}$ and $f_{max} = 37 \text{ GHz}$.

Next, we have benchmarked the small-signal model against the experimental Y -parameters. Fig. 4 shows the measured Y -parameters in the 1–50 GHz range at $V_{ds} = -1.1 \text{ V}$ and $V_{gs} = 0.5 \text{ V}$, which correspond to the bias with the highest measured $f_{T,x} = 34 \text{ GHz}$ and $f_{max} = 37 \text{ GHz}$. The four elements of the complex admittance matrix are compared against our calculations. The intrinsic Y' was directly extracted from the quasi-static small-signal model, while the values of gate series resistance R_g , the parasitic gate-to-source and drain-to-source capacitances, C_{pgs} and C_{pds} , respectively, were optimized to fit the measured Y -parameters. Both series resistances at drain and source, R_d and R_s , were assumed to be $R_c/2$. In addition to the good agreement between simulated and measured Y -parameters in the whole range of examined frequencies, Fig. S4 in the ESI† shows that the extracted values of C_{pgs} and C_{pds} , presented in Table 2, are similar to the ones measured from an open GFET structure (*i.e.* without the graphene layer), which confirms the validity of our approach.

Using the parasitic elements found in the previous step, we analyzed the bias dependence of $f_{T,x}$ and f_{max} . The results are compared with measurements in Fig. 5, showing similar trends. A more detailed insight on the bias dependence of RF performance can be obtained from the map of f_{max} shown in Fig. 6(a). A total of four maxima with f_{max} of $\sim 40 \text{ GHz}$ are observed and labelled as A, B, C, and D, where A and C maxima occur at

Table 2 Values of the parasitic elements in the GFET extrinsic network

| Parameter | Optimized value |
|-----------|-----------------|
| R_g | 10 Ω |
| R_s | 5.5 Ω |
| R_d | 5.5 Ω |
| C_{pgs} | 4.6 fF |
| C_{pds} | 7.6 fF |



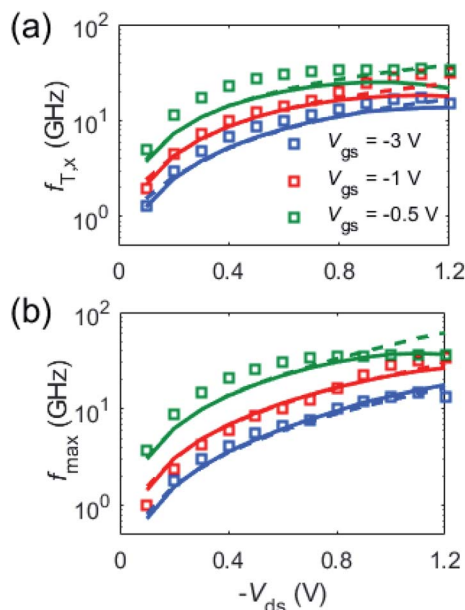


Fig. 5 Measured (squares) and modelled (solid lines) of (a) $f_{T,x}$ and (b) f_{max} as a function of the drain bias. Dashed lines represent f_{max} and $f_{T,x}$ switching off the self-heating effect.

positive drain bias while B and D maxima at negative drain bias. Note that when gate voltage is equal to the Dirac voltage (*i.e.* $V_{gs} = V_D \approx V_{gs0} + V_{ds}/2$), transconductance g_m changes its sign, which makes $f_{max} \sim 0$. On top of that, for a given drain bias polarity, *e.g.* negative, the B maximum is located at $V_{gs} < V_D$, which corresponds to a unipolar p-channel with the pinch-off close to the drain side, while at $V_{gs} > V_D$, the D maximum corresponds to a unipolar n-channel with pinch-off close to the source side (see carrier distributions shown in Section S7 in the ESI†). Those maxima A, B, C and D are located at biases where there is a drop in the total carrier concentration close to the source or to the drain edges.

It has been argued that the highest f_{max} needs current saturation in GFETs. To get the desired current saturation, it has been proposed that GFET operation close to the carrier velocity saturation regime is helpful.^{17,21,39,40} Here we critically review this idea by means of Fig. 6, which helps to visualize the connection between the drift velocity and the small-signal parameters (g_m and g_{sd}). Firstly, in Fig. 6(a) we have plotted the bias dependence of f_{max} , which displays four maxima. Notably, the bias locations of those maxima roughly coincide with the $|g_m|$ peaks (see Fig. S5 in the ESI†), so the $|g_m|$ maxima seem to be an adequate approximate rule to select the bias point if the intended FoM is f_{max} . However, there may be other options to choose the bias point depending on the targeted FoM, for instance, maximization of linearity, noise minimization, *etc.*

For a deeper insight in Fig. 6, we analyzed f_{max} evolution at two different constant V_{gs} , the first at $V_{gs} = 1.1$ V passing through the maximum B (dashed blue line), and the second at $V_{gs} = -1.0$ V (dashed green line) passing far away from the maximum B. The resulting plot is shown in Fig. 6(b). We chose bias B because it presents a higher voltage gain (ratio $|g_m/g_{sd}|$)

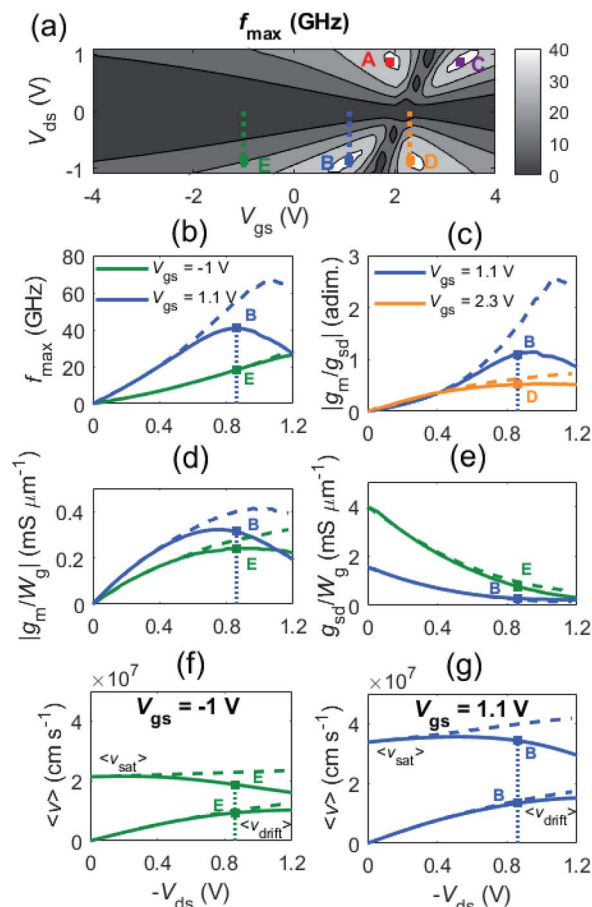


Fig. 6 (a) Bias dependent f_{max} map. It presents four maxima labelled as A, B, C and D. Dashed lines represent the locus of considered drain bias points for f_{max} plot shown in (b) and $|g_m/g_{sd}|$ plot in (c). Transconductance, g_m , and output conductance, g_{sd} , are represented in (d) and (e), respectively. (f) and (g) show average drift velocity and saturation velocity, respectively. Dashed lines correspond to the case where SHE have been switched off.

than bias D, as can be seen in Fig. 6(c). GFETs tend to present very low voltage gains due to the relatively large values of g_{sd} ^{41–44} but in this work we show that this is not an obstacle to reach high power gain. For $V_{gs} = 1.1$ V case, the B maximum is reached at $V_{ds} = -0.86$ V, while for $V_{gs} = -1.0$ V there is no an absolute maximum of f_{max} , being f_{max} a monotonous function of V_{ds} , instead. Analyzing the average drift velocity in Fig. 6(f), we confirm the expectation that, far from the B maximum, the higher the drift velocity is (even approaching the saturation velocity), the better f_{max} and the current saturation are, as shown in Fig. 6(b) and (e), respectively. This behavior indeed happens for biases far away from the Dirac voltage, where the channel behaves as unipolar. However, the largest f_{max} is observed at biases near the crossover between unipolar and bipolar behavior such as the B point, where it does not hold that the highest drift velocity, represented in Fig. 6(g), gives the largest f_{max} , represented in Fig. 6(b). Fig. 6(d) and (e) show that a high value of g_m together with a relatively low value of g_{sd} , *i.e.* a high voltage gain, is needed to reach the highest f_{max} possible.



The bias point B and the bias corresponding to the maximum of $|g_m|$ slightly differ because f_{\max} depends in a complex way not only on g_m , but on g_{sd} , the transcapacitances and the parasitic elements.⁴⁵

On the other hand, f_{\max} is not the highest possible when the GFET is operated far away from Dirac voltage, and this can be explained by the degraded g_m and g_{sd} , as shown in Fig. 6(d) and (e), respectively. The degradation of g_m and g_{sd} at bias E respect to the bias B is caused, in turn, by a decrease in the drift velocity because of the larger carrier concentration. The bias that maximizes RF performance is thus the result of a complex interplay between carrier concentration and carrier velocity in graphene, where self-heating plays a significant role.

A local analysis of the carrier velocities along the channel at both biases E and B (Fig. 7) reveals more details on the central question of this paper, namely, if velocity saturation is needed for the highest f_{\max} . As there are two transport mechanisms at play (drift and diffusion), we have introduced in S3 of the ESI,[†] as a matter of convenience, the definitions of drift, diffusion and total velocities that can be directly compared with the saturation velocity. At the E bias, where the channel is unipolar p-type, Fig. 7(d) shows that v_{drift} dominates over v_{diff} and is roughly 50% of v_{sat} . The ratio $v_{\text{drift}}/v_{\text{sat}}$ could be increased up to $\sim 100\%$ with a higher drain bias; for instance, it is 64% for $V_{\text{ds}} = -1.2$ V, according to Fig. 6(f). However, at the B point, where the pinch-off is near the drain side, diffusion contribution is much higher with $v_{\text{diff}}/v_{\text{drift}}$ around 40% near the drain, being $v_{\text{drift}}/v_{\text{sat}} \sim 45\%$, as can be seen in Fig. 7(b). Therefore, our results do not support that operating in the regime of velocity saturation results in the highest f_{\max} .

To assess the impact of SHE, we have shown in Fig. 3(a) how SHE affects drain current, after switching it on and off in the simulations. It can be observed that current saturation is

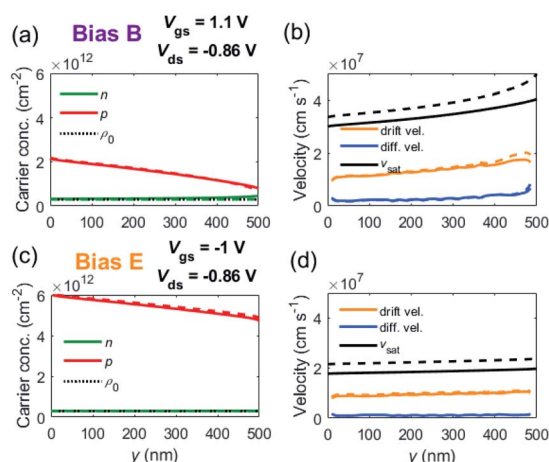


Fig. 7 Distribution along the channel of relevant parameters at bias points labelled as B and E in Fig. 6(a). Solid lines correspond simulations with activated SHE ($T = 571$ K at bias B and 723 K at bias E) and dashed lines to simulations switching off the SHE ($T = 300$ K). (a) Electron and hole concentration at bias B and (c) at bias E. (b) Saturation velocity and carrier velocity broken down into drift and diffusion velocities at bias B and (d) at bias E.

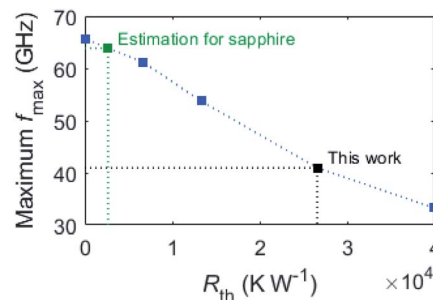


Fig. 8 Maximum f_{\max} as a function of the R_{th} . It has been calculated within the 3rd quadrant of the coordinate plane ($V_{\text{gs}} - V_{\text{D}}$, V_{ds}) with $|V_{\text{ds}}| < 1$ V. Without SHE, f_{\max} can reach 65 GHz.

a result of self-heating, which is triggered at $|V_{\text{ds}}| > 0.6$ V. Additionally, Fig. 5–7 also show the SHE impact on the different parameters of the GFET. At biases near maximum values of f_{\max} , SHE are prominent and graphene temperature reaches ~ 700 K. Importantly, Fig. 8 shows that SHE degrade the value of f_{\max} from 65 to 40 GHz, mainly due to a decrease in v_{drift} , which reduces g_m from 0.4 to 0.3 $\text{mS } \mu\text{m}^{-1}$ despite the larger $v_{\text{drift}}/v_{\text{sat}}$ ratio. This way, it can be concluded that high temperatures limit the RF performance of GFETs. Pop's model for thermal resistance^{22,33} can estimate a reduction of up to 90% if the SiO_2 was substituted by a material like sapphire, which exhibits a thermal conductivity 30 times higher. This would mean an increase in f_{\max} to almost the level of SHE-free GFETs, according to Fig. 8 and assuming that all the power is dissipated through the substrate. More details on the impact of SHE on RF performance can be found in Section S9 of the ESI.[†]

Conclusions

In this work we analyze the influence of carrier velocity saturation on the RF performance of GFETs by means of a drift-diffusion self-consistent simulator. The model includes a number of effects defining the current saturation, namely, the two-dimensional electrostatics, saturation velocity effects, and self-heating effects, which are especially relevant at short channels and/or large drain bias. First, we optimized the model parameters to fit the experimental DC characteristics of a prototype GFET. Then, the measured Y parameters were reproduced by fitting the values of the parasitic capacitances and the gate series resistance using the GFET small-signal equivalent circuit. We simulated the bias dependence of the measured RF FoMs and we discussed the role played by saturation velocity in defining the highest f_{\max} . For biases far from the Dirac voltage, where the channel is unipolar and highly concentrated, a higher drift velocity results in a larger f_{\max} . However, the largest f_{\max} are located at biases close to the onset of bipolar conduction and far from the saturated velocity regime. In that scenario the pinch-off point is close to either the source or drain edge and drift velocity there is no longer saturated. This is caused by the combined effects of carrier concentration and total velocity, which are interdependent. Notably, we found a significant degradation of f_{\max} at high drain



biases because of the self-heating. Based on these results, further optimization of the GFET design for applications in advanced RF electronics can be done by selecting the appropriate bias and reducing the effects of self-heating.

Authors contributions

D. J., J. S. and A. V. conceived the study. P. C. F. conducted the research. F. P. and P. C. F. developed the theoretical models. C. S., L. B., A. V., A. G. and X. Y. developed the technology. X. Y. and M. B. contributed on device fabrication. A. V., M. A. and M. B. characterized fabricated devices. D. J., J. S., A. V., M. A., M. B. and P. C. F. contributed on the analysis of results. C. S. and L. B. grew high-quality chemical-vapour-deposited graphene. D. N. and M. O. developed advanced technology and carried out the transfer of graphene onto Si substrate. D. J., A. V., M. B. and P. C. F. wrote the manuscript. J. S., A. G. and F. P. provided feedback on the manuscript drafts.

Conflicts of interest

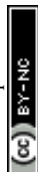
There are no conflicts to declare.

Acknowledgements

This work was funded in part by the European Union's Horizon 2020 Research and Innovation Program under Grant GrapheneCore2 785219 and No. GrapheneCore3 881603, in part by the European Regional Development Funds (ERDF) allocated to the Programa Operatiu FEDER de Catalunya 2014–2020, with the support of the Secretaria d'Universitats i Recerca of the Departament d'Empresa i Coneixement of the Generalitat de Catalunya for emerging technology clusters to carry out valorization and transfer of research results (reference of the GraphCAT project: 001-P001702). It has also been partially funded by the *Ministerio de Economía y Competitividad* under Grant TEC2015-67462-C2-1-R, in part by the *Ministerio de Ciencia, Innovación y Universidades* under grant RTI2018-097876-B-C21 (MCIU/AEI/FEDER, UE), in part in part by the Swedish Research Council under Grant No 2017-04504, and in part by the Academy of Finland.

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