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Enhancing Frequency Stability of Weak Grids with Modified Distributed Virtual Inertia Method

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***Abstract*—In small−scale power systems, distributed virtual inertia (DVI)−based converters can effectively participate in primary frequency regulation. In this method, the synthetic inertia provision is fulfilled by discharging the preserved energy of dc−side capacitors employed in grid−interactive converters. Nevertheless, the eigenvalue analyses provided by small−signal state−space model of the converter reveal that the DVI function induces instability to the converter operating in weak grid connection. To address this issue aimed at improving grid frequency stability during frequency events, a new compensator is presented in this work. The compensator is designed so as eliminates the negative effect of DVI regulator on system stability. The effectiveness of proposed approach is illustrated by the time−domain simulations in MATLAB. The results show that the frequency rate of change following a frequency perturbation is enhanced by 40.38% compared with the scenario in which the synthetic inertia functionality is nullified.**

***Index Terms*—Grid−following voltage source converter (VSC), synthetic inertia, frequency regulation, renewable energy source (RES).**

I. Introduction

Modern electric power systems encounter new critical issues arising from significant shares of decentralized renewable energy generation (REG). Inertia requirement is the paramount challenge in foregoing grids as synchronous generators (SGs) are replaced with power electronic−based generators [1]. This is because the inverter−interfaced units do not naturally provide inertial and damping responses of SGs to the host grid. Thus, the system frequency may exceed the acceptable range following a severe power generation−demand imbalance, leading to e.g. undesirable load−shedding or even large−scale blackouts [2], [3].

Overall system inertia is considered as a major factor affecting two indices 1) rate of change of frequency (RoCoF), and 2) frequency nadir — the minimum frequency that grid experiences after a disturbance [4]. The more system inertia, the better short−term frequency regulation. On the other side, reducing grid inertia is one of the parameters that impose a limit on further penetration of renewable energy sources (RESs) into power grids [5]−[7]. The solution can be found in the control scheme of interfaced converters, where numerous papers have been dedicated to REG participating in grid frequency control.

A. Literature Survey

Ref. [8] proposed the synchronous generator emulation control (SGEC) technique for voltage source converters (VSCs) employed in HVDC stations. This controller introduces an inertia element into the frequency−power droop function, determining the command reference of the frequency. Thus, the inertia response and primary frequency regulation are emulated. In [9], the authors introduced a fast frequency regulator by wind farm doubly−fed induction generators (DFIGs) with auxiliary dynamic demand control. This method coordinates the DFIG and controllable loads to jointly provide synthetic inertia after grid frequency perturbations. Research work conducted in [10] used an ultra−capacitor to improve the frequency stability. Therein, an integral operator is paralleled with the droop loop and a distribution function. Ref. [11] proposed a modified control method for battery energy storage systems (BESS) employed in autonomous microgrids with high shares of inverter−interfaced generators. In this approach, the frequency controller, comprised of a droop function and inertia emulator, governs the BESS active power transfer during the primary frequency control level. A virtual inertia emulator−based model predictive control (MPC) has been presented in [12]. This method finds the optimal control actions of the conversion system by predicting its future behaviors, resulting in the reduction of energy storage system capacity required for frequency control. Ref. [13] also proposed the centralized and decentralized MPC−based controllers for converter−interfaced generators operating in grid−forming mode. The controllers manipulate converter power injections

to limit the frequency nadir and RoCoF metrics after a disturbance. A synthetic inertia emulator called distributed virtual inertia (DVI) for mimicking inertial response of real SGs has been presented in [14] and [15]. The DVI concept uses the dc−side capacitors employed in the dc−link of grid−connected converters as the energy buffer aimed at short−term frequency stability improvement. This method can be applied without increasing system cost and complexity.

B. Problem Description and Paper Contribution

The small−signal state−space analysis affirms that the differential operator df/dt and its corresponding gain in the DVI technique induces instability to the converter controller operating in weak grid connection. Thus, this paper concerns the stability of grid−following converters augmented with the DVI functionality. To address the aforesaid issue aimed at improving grid frequency stability during frequency events, a new compensator is designed and applied to the d−axis inner current controller working in synchronous reference frame (SRF). Consequently, the proposed control framework can provide the maximum DVI support and keep the system stable. The rest of the paper is organized as follows. Section II describes the control platform of a typical grid−tied converter and its general formulations in the state−space forms. The instability problem raised by the DVI loop is then illustrated in Section III using the small−signal state−space theorem. Section IV presents the compensation method and its design process. Then, the effectiveness of DVI−based VSC is depicted in Section V by the time−domain simulations in MATLAB/Simulink. Finally, Section VI summarizes the original contribution and main outcomes of the paper.

II. Grid−Interfaced Converter Control Technique

A. System Platform

Fig. 1 illustrates the block diagram of a grid−following VSC system connected to a weak grid. The primary side of the converter can be fed by renewable energy sources, e.g. solar panels or wind turbines. The employed LC filter mitigates high−order current harmonics generated by the switching process. Moreover, the grid is presented as equivalent Thevenin model with grid strength defined by short−circuit ratio (SCR):

$$SCR = \frac{u_{p,rated}^2/Z_g}{p_{out,rated}}, \tag{1}$$

where Z_g, $u_{p,rated}$, and $p_{out,rated}$ stands for network impedance at the fundamental frequency, rated voltage and power of the converter, respectively. Specifically, the system with SCR>3 is known as a strong grid while SCR≤3 represents a weak grid condition.

Owing to synchronization process performed by the phase−locked loop (PLL), the VSC includes two synchronous coordinates: one is the grid frame (denoted by dq) and the other one is controller frame (denoted by dq^c) [16]. The former frame is defined by point of interconnection voltage (u_p). And, the latter one is introduced by the PLL dynamics following a

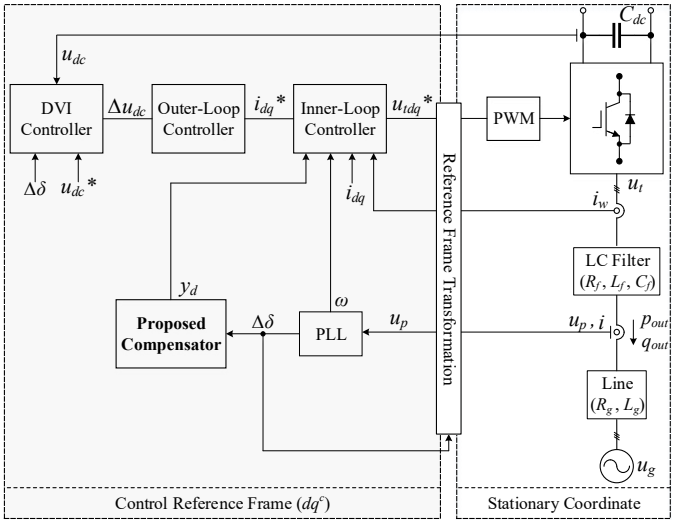


Fig. 1: Grid−interactive VSC augmented with the DVI function.

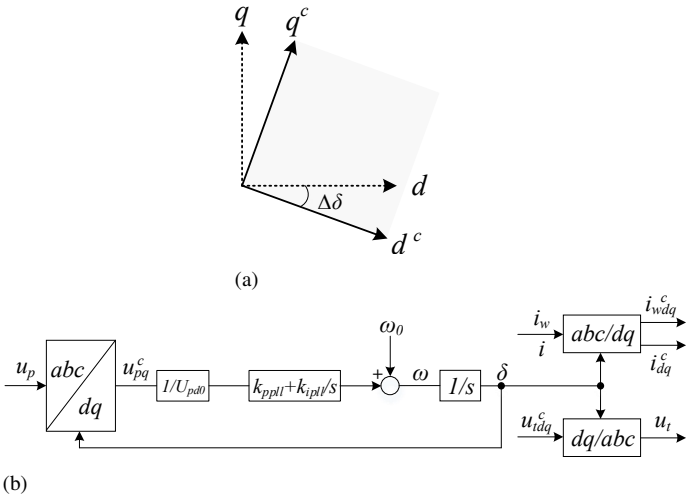


Fig. 2: (a) Reference coordinates associated to the grid and the controller, (b) SRF−PLL.

perturbation. In steady state, the two frames are aligned and adhered to each other. During frequency event (e.g. power generation−demand mismatch), the PLL output (δ) fluctuates to re−synchronize the converter with the network. Hence, the SRFs are no longer aligned and the dq^c frame lags the grid frame as depicted in Fig. 2(a).

In order to model the PLL dynamics, the measured signals i_w, i and u_p in the grid coordinate are rotated to the dq^c aimed at control process as demonstrated in Fig. 2(b). Then, the converter voltage references u_{td}^{c*} and u_{tq}^{c*} produced by the controller are re−transformed to the dq coordinate. Assuming the difference angle between two frames (denoted by $\Delta\delta$) is small enough, this procedure is modeled mathematically in the complex space vector form as:

$$u_p^c = (1 - j\Delta\delta)u_p,\ i^c = (1 - j\Delta\delta)i$$
$$i_w^c = (1 - j\Delta\delta)i_w,\ u_t^* = (1 + j\Delta\delta)u_t^{c*}. \tag{2}$$

B. State−Space Realization of the System

In this subsection, the state−space representation of the system in Fig. 1 is obtained in details. Then, the equations are linearized at equilibrium points for stability analyses.

1) Synchronization unit: The structure of the employed PLL is depicted in Fig. 2(b). First, the point of interconnection voltage (u_p) is decomposed to the d^c- and q^c- components using Park transformation. The grid frequency is then estimated by setting normalized q^c- voltage component to zero through a proportional−integral (PI) controller ($G_{pll} = k_{ppll} + k_{ipll}/s$). Next, the grid frequency is passed through an integrator to attain the synchronization angle (δ) applied to coordinate transformations (i.e. from abc or dq frame to dq^c frame and vice versa). The state−space model of the aforesaid process is expressed mathematically as:

$$\dot{\delta} = \omega = \omega_0 + (k_{ppll}/U_{pd0})u^c_{pq} + \varphi_\delta \tag{3}$$

where φ_δ is defined as:

$$\varphi_\delta = (k_{ippl}/U_{pd0}) \int u^c_{pq} dt. \tag{4}$$

2) DC−link voltage: Presuming energy losses across converter switches and LC filter is negligible, the equation describing power balance between two sides of the interfaced converter is:

$$p_{in} - p_{out} = C_{dc} \frac{du_{dc}}{dt} u_{dc}. \tag{5}$$

Then, the state−space model of dc−bus voltage is:

$$\dot{u}_{dc} = \frac{p_{in} - \frac{3}{2}(u_{pd} i_d + u_{pq} i_q)}{C_{dc} u_{dc}}. \tag{6}$$

3) LC filter and grid: To suppress current harmonics produced by the converter switching process, an LC filter is employed at the output of the VSC. The reference voltages u^*_{td} and u^*_{tq} are assumed to appear at the input side of the employed filter after re−transforming from the dq^c coordinate to the grid coordinate. The aforesaid assumption only disregards the energy losses across converter switches [17]. Using complex−valued space vectors presentation, the SRF state−space equations governing the ac−side dynamics are established as:

$$\dot{i}_w = \frac{1}{L_f} u_t - \frac{1}{L_f} u_p - (\frac{R_f}{L_f} + j\omega) i_w \tag{7}$$

$$\dot{u}_p = \frac{1}{C_f} i_w - \frac{1}{C_f} i - j\omega u_p \tag{8}$$

$$\dot{i} = \frac{1}{L_g} u_p - \frac{1}{L_g} u_g - (\frac{R_g}{L_g} + j\omega) i. \tag{9}$$

4) Inner−loop current controllers: The output $d-$ and $q-$ current components (i.e. i_d and i_q) are set to their reference values using two separate PI−controllers ($G_i = k_{pi} + k_{ii}/s$) as illustrated in Fig. 3. The $d-$axis current reference is obtained by regulating the dc−link voltage to its nominal value, while the reactive power requirement defines $q-$axis current reference. It is noteworthy that all the measured quantities in Fig. 3 are in the controller SRF. Hence, the current controllers are modeled mathematically as:

$$u^c_{td} = u^c_{pd} - \omega L_f i^c_{wq} + k_{pi}(i^*_d - i^c_d) + \varphi_{id} \tag{10}$$

$$u^c_{tq} = u^c_{pq} + \omega L_f i^c_{wd} + k_{pi}(i^*_q - i^c_q) + \varphi_{iq} \tag{11}$$

in which φ_{id} and φ_{iq} are, respectively:

$$\varphi_{id} = k_{ii} \int (i^*_d - i^c_d) dt \tag{12}$$

$$\varphi_{iq} = k_{ii} \int (i^*_q - i^c_q) dt. \tag{13}$$

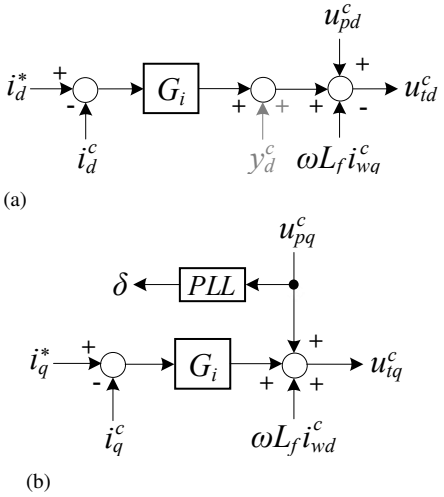


Fig. 3: Current controller, (a) $d-$channel, (b) $q-$channel.

5) DC−voltage controller augmented with DVI loop: This loop aims at regulating the dc−side voltage to the nominal value of u^*_{dc} by a PI−controller ($G_u = -k_{pu} - k_{iu}/s$). Furthermore, the ancillary signal (u^{anc}_{dc}) provided by DVI technique is added to the voltage controller for primary frequency regulation (Fig. 4). The applied approach links frequency oscillations (raised by power generation−demand mismatch) to the control scheme so as $\Delta\delta$ yields the dc−link voltage deviations. It is worth mentioning that δ is the time−derivative of grid angular frequency ω. Therefore, the dc−voltage control is mathematically presented by:

$$i^*_d = k_{pv}[u_{dc} - u^*_{dc} - u^{anc}_{dc}] + \varphi_u \tag{14}$$

in which u^{anc}_{dc} and φ_u are, respectively:

$$u^{anc}_{dc} = k(\omega - \omega_0) \tag{15}$$

$$\varphi_u = k_{iu} \int [u_{dc} - u^*_{dc} - u^{anc}_{dc}] dt. \tag{16}$$

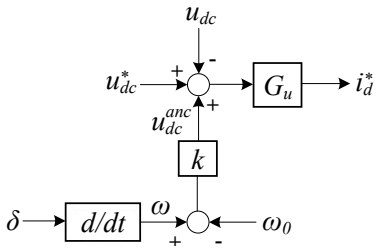


Fig. 4: DC−bus voltage controller equipped with the DVI functionality.

III. Small−Signal Stability Analyses

In this section, the instability issue caused by DVI function is studied. In this regard, the foregoing equations (2)−(16) are linearized around equilibrium points. Hence, the small−signal state−space representation of the VSC in Fig. 1 is obtained in the standard form of:

$$[\Delta \dot{x}_{uncomp}] = [A_{uncomp}][\Delta x_{uncomp}] + [B_{uncomp}][\Delta u] \tag{17}$$

where Δx_{uncomp} and Δu stands for state vector and input vector defined, respectively as:

$$\Delta x_{uncomp} = [\Delta\delta\ \Delta\varphi_\delta\ \Delta i_{wd}\ \Delta i_{wq}\ \Delta u_{pd}\ \Delta u_{pq} \\ \Delta i_d\ \Delta i_q\ \Delta u_{dc}\ \Delta\varphi_u\ \Delta\varphi_{id}\ \Delta\varphi_{iq}]^T \tag{18}$$

$$\Delta u = [\Delta p_{in}\ \Delta i^*_q]^T. \tag{19}$$

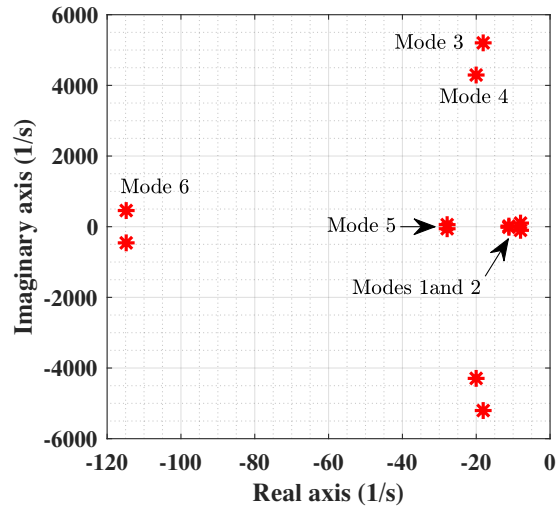
The state variables $\Delta\varphi_\delta$, $\Delta\varphi_u$, $\Delta\varphi_{id}$ and $\Delta\varphi_{iq}$ correspond to integral parts of the PLL, outer−loop voltage controller, d−axis current controller, and q−axis current controller, respectively. The detailed specifications of the system under study is provided in Table I.

TABLE I: System Parameters

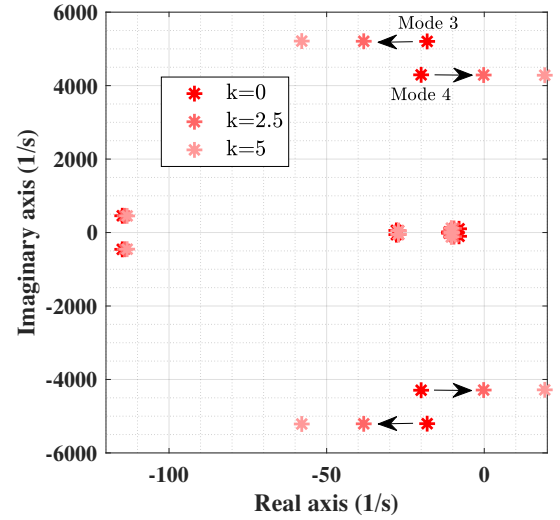
Parameter	Value	Parameter	Value
R_f, R_g	0.1, 2.5 Ω	k_{ppll}, k_{ipll}	50, 320
L_f, L_g	2, 8 mH	k_{pi}, k_{ii}	1, 1000
C_f, C_{dc}	50 μF, 3 mF	k_{pu}, k_{iu}	0.1, 2
ω_0	$2\pi\times$ 50 rad/s	u^*_{dc}	700 V
k, k_d	20 , 4.8 $V.s$	p_{in}	15 kW
ζ_d	0.8	i^*_q	0/9 A
ω_d	2000 rad/s	$u_p(L-L)$	400 V

Fig. 5(a) depicts eigenvalue locus of the VSC system under weak grid condition (SCR=3) whilst there is no frequency disturbance (i.e. generation and demand are balanced). The eigenvalues define 6 different modes. According to Lyapunov stability theory and Fig. 5(a), the VSC is sympathetically stable. When the grid is subjected to a small frequency perturbation, the ancillary DVI technique yields migration of modes 3 and 4 towards the left and right hand side of s−plane, respectively while the effect on other modes is negligible [see Fig. 5(b)].

The higher DVI gain (k), the better short−term frequency regulation; nonetheless, it exacerbates the system stability as



(a)



(b)

Fig. 5: System eigenvalues when (a) k=0 (b) k changes.

observed from Fig. 5(b). Thus, we can conclude that the DVI approach (aimed at primary grid frequency regulation) leads to instability of the VSC connected to weak grid.

IV. Proposed Compensation Technique

To eliminate the instability problem originated from ancillary DVI controller, a new compensator is presented in this work. As illustrated in Fig. 3(a), the compensation signal y^c_d introduces one degree−of−freedom to the d−channel of the VSC controller. The mathematical presentation of this supplementary signal in Laplace domain is:

$$y^c_d(s) = \frac{2\zeta_d\omega_d k_d s}{s^2 + 2\zeta_d\omega_d s + \omega^2_d}(\dot{\delta} - \omega_0). \tag{20}$$

The proposed compensator is designed based on the fact that the PLL output (δ) entered to the d−channel through DVI function is the detrimental factor of the system stability in weak grids [see Fig. 3(a) and Fig. 4]. Thus, the

time−derivative of PLL output is chosen as the input signal to (20). The signal $\dot{\delta} - \omega_0$ is then entered to a band−pass filter in order to attain $y_d^c(s)$, where k_d, ζ_d and ω_d are the corresponding gain, damping ratio, and cut−off frequency, respectively. It should be emphasized that $y_d^c(s)$ is zero in steady state operation. Therefore, it does not affect the tracking of controlled variables.

Two state variables γ_1 and γ_2 are defined by (20) with the small−signal state−space realization of:

$$\begin{bmatrix}\dot{\Delta\gamma}_1\\ \dot{\Delta\gamma}_2\end{bmatrix} = \begin{bmatrix}-2\zeta_d\omega_d & 1\\ -\omega_d^2 & 0\end{bmatrix}\begin{bmatrix}\Delta\gamma_1\\ \Delta\gamma_2\end{bmatrix} + \begin{bmatrix}-2\zeta_d\omega_d k_d k_{ppll}\\ 0\end{bmatrix}\Delta\delta + \begin{bmatrix}2\zeta_d\omega_d k_d\\ 0\end{bmatrix}\Delta\varphi_\delta + \begin{bmatrix}2\zeta_d\omega_d k_d k_{ppll}/U_{pd0}\\ 0\end{bmatrix}\Delta u_{pq} \quad (21)$$

and $\Delta y_d^c = \Delta\gamma_1$, which are added to the uncompensated system presented by (17). Hence, the final state−space model of the compensated VSC can be presented by:

$$[\Delta\dot{x}_{comp}] = [A_{comp}][\Delta x_{comp}]. \quad (22)$$

Fig. 6 depicts the eigenvalue locus of the compensated system in terms of different k_d and ζ_d. Note that a worst−case scenario (i.e. k=20 and SCR=3) is considered in the compensator design process. The parameter k_d varies between [0 , 4.8] $V.s$ and ζ_d takes two values, 0.7 and 0.8. As observed from this figure, the dominant modes 3 and 4 move towards the right and left hand side of s−plane, respectively by increasing the gain k_d. This signifies that the adverse impact of DVI function on the system eigenvalues is compensated by the ancillary signal y_d^c [see Figs. 5(b) and 6]. Two points should be mentioned here: 1) the proposed compensator does not have any effect on the other modes, and 2) the motion of modes 3 and 4 occurs in a faster rate for higher ζ_d and ω_d. At k_d=4.8 $V.s$, ζ_d=0.8 and ω_d=2000 rad/s, the unstable mode 4 is relocated to -41$\pm j$4500 (see Fig. 6). Hence, the proposed compensator can provide maximum DVI support and keep the VSC stable in weak grid connection.

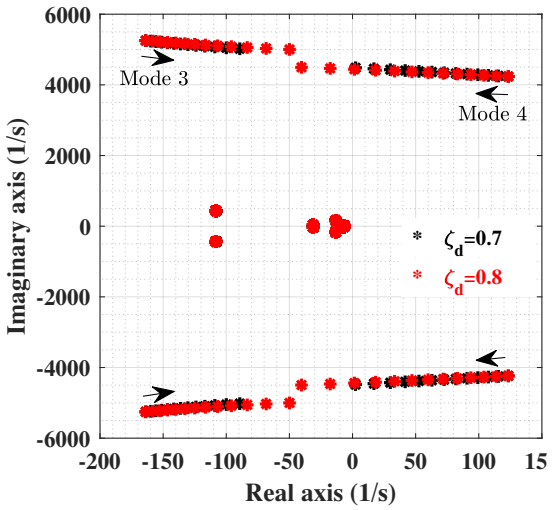


Fig. 6: The effect of proposed compensator on eigenvalues locus ($0 \leq k_d \leq 4.8$ $V.s$).

V. Results and Discussions

Some simulations are carried out in MATLAB to verify the above−mentioned theoretical analyses and proper operation of the presented compensator in (20). The parameters of the VSC understudy are provided in Table I. Furthermore, the maximum permissible dc−bus voltage fluctuations is assumed 13%.

A. Uncompensated−System

The VSC system response without proposed compensation technique is assessed in this subsection. Fig. 7 depicts the injected active and reactive power to the weak grid when the power commands change by ±33.3% and +100%, respectively. The corresponding dc−bus voltage is also illustrated in Fig. 7. It is clear that the controlled variables p_{out}, q_{out} and u_{dc} reach desired steady state values which confirm the proper operation of the VSC model under grid−normal condition. As previously mentioned, however, the DVI loop is sufficient to induce system instability when a grid frequency disturbance occurs. Notice, the DVI functionality aims at primary frequency support following a grid contingency. To demonstrate the instability issue resulted from this loop, the model is perturbed through a load change at t=2 s and

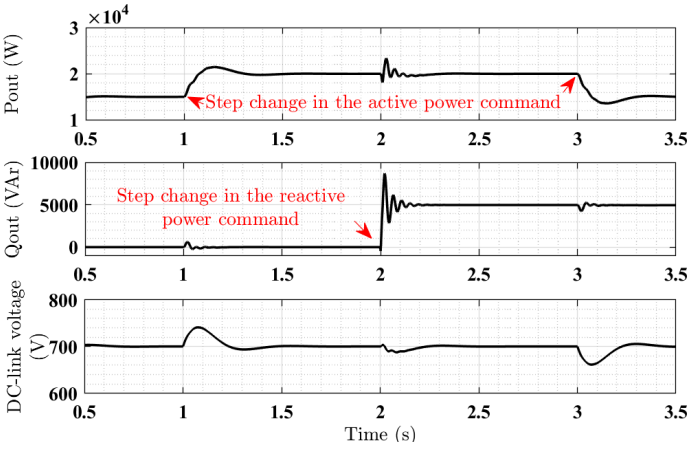


Fig. 7: Uncompensated system response: output power, and dc−bus voltage.

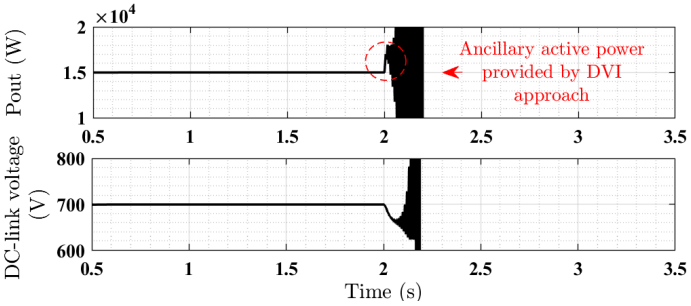


Fig. 8: Active power injection and dc−link capacitor voltage deviations, when the load fluctuation arises at t=2 s.

the obtained results are presented in Fig. 8. As observed from this figure, the system subjects to instability right after the disturbance, which successfully confirms the accuracy of small−signal analyses presented in Section III.

B. Compensated−System

To enhance the grid frequency stability by means of the DVI loop, the proposed compensator is implemented in the control block. Fig. 9 depicts the power exchange between the converter and the network considering a load perturbation at t=2 s. As observed from this figure, p_{out} increases instantly from 15 kW to 17.2 kW when the disturbance arises. This extra active power is analogous with the released kinetic energy of SGs to restore the power balance. The dc−bus voltage deviations is also presented in Fig. 9. It is clear that the voltage decreases to 610 V after the disturbance by the DVI loop. This means that the released energy from the capacitor C_{dc} can support the grid frequency during transient time. Furthermore, the frequency oscillations is brought in Fig. 10. This figure shows that the grid experiences a lower frequency nadir if the DVI loop is activated; and the rate of change of frequency is improved by 40.38% in comparison with the scenario in which the DVI regulator is canceled out.

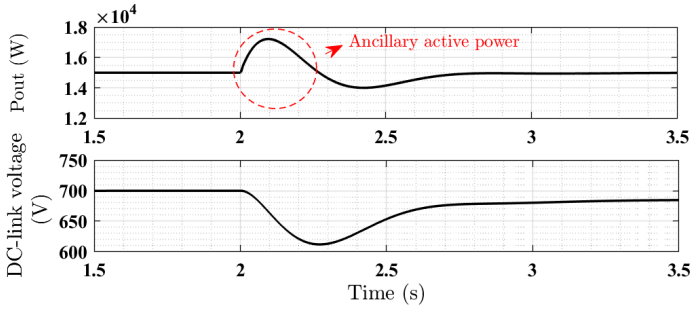


Fig. 9: Output power, and dc−link capacitor voltage deviations in the compensated system.

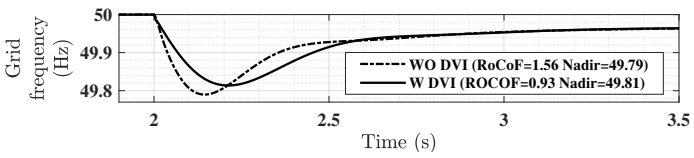


Fig. 10: Grid frequency deviations (WO DVI and W DVI stands for without and with DVI functionality, respectively).

VI. Conclusions

This paper concerned with the instability of grid−interactive converters equipped with distributed virtual inertia (DVI) method in weak grids. It is noteworthy that the DVI is a simple method whereby the inertia characteristic of real SGs is emulated through the preserved energy in the dc capacitors of converters employed in the small−scale modern power grids. As stated in Sections III and V, however, this technique yields instability of the conversion system connected to weak grid. In order to address this issue aimed at improving grid frequency stability during frequency events, a new compensator has been presented and validated by simulations in Matlab. The results illustrated that the DVI function can reduce frequency nadir following a load disturbance, and the frequency rate of change is enhanced by 40.38% in comparison with the scenario in which the ancillary DVI regulator is deactivated.

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