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A Universal Controller for Grid-Connected Voltage-Source Converters

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***Abstract*—Power-synchronization control (PSC) and vector current control (VCC), the latter including cascaded outer loops, are, respectively, considered to be grid-forming and grid-following schemes. They have significant structural differences. Despite that, it is here shown that the two schemes can be unified by making a series of minor modifications to PSC. This results in a universal controller, allowing various combinations of the two schemes to be explored. Fundamentally, it allows PSC to be used as guideline for a robust VCC design, permitting stable and well-performing operation irrespective of the grid strength.**

***Index Terms*—Grid-connected converters, grid-following control, grid-forming control, robustness, voltage-source converters.**

I. Introduction

THE PROLIFERATION of renewable energy sources interfaced to the grid by voltage-source converters has spurred a significant interest in grid-forming control [1], [2]. Thereby, it is partly implied voltage-stiff operation—i.e., operation with near-constant converter-voltage magnitude—mimicking the back electromotive force of a synchronous machine, and partly the emulation of a swing equation, accomplishing grid synchronization by a power controller (PC), which may include inertial response, if desired [3]. These two parts are essential for preserving the stability of a grid having a high penetration of converter-interfaced generation [4].

In contrast, grid-following control features current-stiff operation—i.e., the converter voltage is set by a current controller (CC) [5]. Grid synchronization is accomplished via a phase-locked loop (PLL), normally applied to the point-of-common-coupling (PCC) voltage [6]. While grid-forming control mimics a synchronous machine, grid-following control is inherited from vector control of ac motor drives. Too high concentration of grid-following converters may lead to various converter–grid instability phenomena [7]. Even one grid-following converter may exhibit stability problems when connected to a weak grid [8].

However, grid-forming and grid-following controls do not reside in fully isolated realms; there are grid-following ingredients in most grid-forming schemes. A PLL was initially proposed to be included in the Synchronverter [9]. For damping purposes, power-synchronization control (PSC) [10] includes what here is called an active-resistance control law (ARC). The active resistance is, in effect, the proportional gain of a CC. In addition, to prevent overcurrent during abnormal situations, grid-forming control may feature an embedded CC (ECC) [10].

Conversely, in grid-following schemes, the CC is cascaded with outer loops in a scheme often collectively called vector current control (VCC). In addition to the aforementioned PLL, these loops may include an ac-bus-voltage controller (AVC) [11]. The AVC introduces voltage stiffness, i.e., a grid-forming feature [12]. Loops for inertial and frequency responses can be added as well [13]. Such a principle is followed in the pioneering work on the virtual synchronous machine [3], even though this scheme is generally considered to be grid-forming.

From this discussion it is evident that there is a grey zone between grid-forming and grid-following controls. Many converters are operated as fully grid-following, particularly when connected to a strong grid (which makes an AVC superfluous). Conversely, fully grid-forming operation is, in fact, undesirable, since it would result in very poor damping (owing the lack of an active resistance) and risk for overcurrent (owing to the lack of a CC or an ECC).

The outline and contributions of the paper are as follows. VCC and PSC are briefly revisited in Section II. The main contribution is the derivation, in Section III, of a universal controller which encompasses the extremes, i.e., grid-forming and grid-following controls, as well as the grey zone in between. Its derivation is based on showing that a slightly modified PSC scheme fits within a VCC scheme which employs a generic AVC. In addition, a hybrid synchronization controller that combines a PLL with a PC is introduced. The universal controller allows exploring various combinations of VCC and PSC ingredients. The main focus is on using PSC as a guideline for a robust VCC design, which permits stable operation irrespective of the grid strength, i.e., even when connected to a very weak grid. The result is similar to certain so-called "active damping" schemes [14]–[16]. Performance comparisons of the modified PSC and the robustly designed VCC are made experimentally in Section IV.

II. Fundamentals

A. Notation, Main Circuit, and Control Principles

Throughout the paper, boldface letters denote complex space vectors. A superscript s denotes a space vector referred to the

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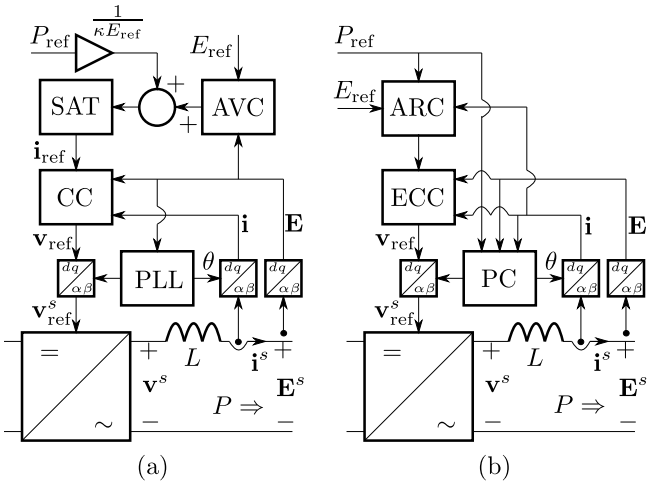

Fig. 1. Circuit and block diagrams of (a) VCC and (b) PSC.

stationary $\alpha\beta$ reference frame. The absence of this superscript denotes the corresponding vector referred to the synchronous dq reference frame, which has angle θ as reference. Italic letters denote scalar variables and real transfer functions (although the latter may operate on complex space vectors, in the dq frame coupling from d to d and from q to q). The reference for a controlled variable is denoted by appending the sub- or superscript ref. The Laplace variable s is to be considered as the operator $s = d/dt$, where appropriate.

Figs. 1(a) and (b) respectively show the circuit and block diagrams of VCC and PSC. The main circuits are in both cases identical, consisting of a filter, approximated as the pure inductance L, between the converter and PCC buses. The respective bus-voltage vectors are $\mathbf{v}^s$ and $\mathbf{E}^s$, whereas the output current is $\mathbf{i}^s$. P is the active output power at the PCC, calculated by taking the real part of the complex output power

$$\mathbf{S} = \kappa \mathbf{E}^s (\mathbf{i}^s)^* = \kappa \mathbf{E} \mathbf{i}^*, \qquad \kappa = \frac{3}{2K^2} \tag{1}$$

where the superscript $*$ denotes complex conjugate and K is the space-vector scaling constant. The dq frame is statically aligned with the PCC voltage, so that $\mathbf{E} = E$ (i.e., real), giving in the steady state

$$P = \mathrm{Re}\{\mathbf{S}\} = \kappa E i_d \qquad Q = \mathrm{Im}\{\mathbf{S}\} = -\kappa E i_q \tag{2}$$

where Q is the reactive output power at the PCC.

Vector $\mathbf{v}^s$ is effectuated from its reference $\mathbf{v}^s_{\rm ref}$ by pulsewidth modulation. This comes with a lag and switching harmonics are added. In addition, $\mathbf{v}^s_{\rm ref}$ may need to be saturated (at least transiently) to avoid overmodulation. For the purpose of dynamic studies, harmonics and saturation may be disregarded. In addition, the lag can usually be neglected, except when high-frequency properties are studied. Since this is not done here, for analysis purposes it is always assumed that $\mathbf{v} = \mathbf{v}_{\rm ref}$.

B. VCC

This scheme employs a conventional dq-frame CC, comprising a proportional part, a dq decoupler compensating the steady-state voltage drop across the inductive filter, and a feedforward of the PCC voltage through a low-pass filter $H(s)$ [with $H(0) = 1$], illustrated in Fig. 2 and given as

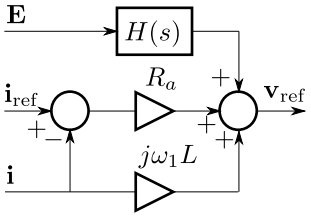

Fig. 2. CC with proportional part, dq decoupler, and PCC-voltage feedforward.

$$\mathbf{v}_{\rm ref} = R_a(\mathbf{i}_{\rm ref} - \mathbf{i}) + j\omega_1 L \mathbf{i} + H(s)\mathbf{E} \tag{3}$$

where ω_1 is the nominal angular synchronous frequency. Suitable recommendations for selection of the proportional gain R_a (so denoted for analogy with PSC, see below) and the feedforward filter $H(s)$ are based on the desired closed-loop-system bandwidth α_c, as [5]

$$R_a = \alpha_c L \qquad H(s) = \frac{\alpha_c}{s + \alpha_c}. \tag{4}$$

In turn, the selection recommendation for α_c is up to one tenth of the angular sampling frequency ω_s of the converter control system [17]

$$\alpha_c \leq 0.1\omega_s. \tag{5}$$

Owing to the feedforward term, the decoupler, and the assumption of a purely inductive filter, (3) ideally allows $\mathbf{i}$ to track the dc component of $\mathbf{i}_{\rm ref}$—i.e., in the $\alpha\beta$ frame the fundamental positive-sequence component—with zero static error, despite the lack of an integral part in (3). In practice, however, there will be a residual control error resulting from various parasitic effects, such as a nonnegligible filter resistance. To remove this, a compensation for the resistive voltage drop and/or a low-gain integral part can be added to (3), as can resonant parts for the control of the fundamental negative-sequence component and/or harmonics.

At least two outer loops, the PLL and the AVC, feed references to the CC in a cascaded fashion.

The PLL computes the dq-frame reference angle as

$$\theta = \frac{1}{s}\left[\omega_1 + F_p(s)\mathrm{Im}\{\mathbf{E}\}\right] \tag{6}$$

where $F_p(s)$ is the PLL controller, usually proportional or proportional–integral, cascaded with a low-pass filter for disturbance suppression [6]. Thereby, the dq frame is synchronized with the PCC voltage by forcing the q component of $\mathbf{E}$ to zero in the steady state. The closed-loop PLL dynamics typically have bandwidth at least one order of magnitude lower than α_c.

The AVC partly determines $\mathbf{i}_{\rm ref}$. Together with the synchronizing effect of the PLL, the AVC ensures that $\mathbf{E} = E_{\rm ref}$ in the steady state. Thus, $P = \kappa E_{\rm ref} i_d$ statically [see (2)], which motivates adding a d component

$$i_P^{\rm ref} = \frac{P_{\rm ref}}{\kappa E_{\rm ref}} \tag{7}$$

to $\mathbf{i}_{\rm ref}$ to achieve an open-loop active-power control. We obtain

$$\mathbf{i}_{\rm ref} = \text{SAT}\left\{i_P^{\rm ref} + \text{AVC}(E_{\rm ref}, \mathbf{E})\right\} \tag{8}$$

where a vectorial saturation (SAT) is added for limiting the magnitude of $\mathbf{i}_{\rm ref}$ to the maximum permissible value. The SAT is normally transparent (i.e., not effectuated), but its inclusion is particularly important for helping to prevent overcurrent in abnormal situations.

$E_{\rm ref}$ can either be constant or be adjusted online, e.g., by a reactive-power droop [18]. The latter is important particularly in a strong-grid connection, in order to avoid excessive reactive-power exchange. It is here assumed that the adjustment of $E_{\rm ref}$ is made slower than the other control loops, allowing $E_{\rm ref}$ to be considered constant for analysis purposes.

The AVC is allowed to be generic, but conventionally it uses the d component (i.e., real part) of the control error $E_{\rm ref} - \mathbf{E}$ as input and sets the q component of $\mathbf{i}_{\rm ref}$, i.e., it is dq asymmetric[1]

$$\text{AVC}(E_{\rm ref}, \mathbf{E}) = -jF_v(s)(E_{\rm ref} - \text{Re}\{\mathbf{E}\}). \tag{9}$$

In order to achieve zero static control error, controller $F_v(s)$ must include an integral part. The response in $\mathbf{E}$ to a change in $\mathbf{i}$ depends on the grid impedance, which is often not fully known and may vary. Partly for this reason, $F_v(s)$ is often designed empirically [19].

C. PSC

The PSC block diagram depicted in Fig. 1(b) includes the ARC, which, via the ECC (see [10] for details), sets the voltage reference as

$$\mathbf{v}_{\rm ref} = \text{ECC}\{\mathbf{V} + R_a(\mathbf{i}_{\rm ref} - \mathbf{i})\} \tag{10}$$

where $\mathbf{V}$ normally is selected real, $\mathbf{V} = V$, and R_a is the active resistance. [In Section III-A, $\mathbf{V}$ is instead selected as a function of $E_{\rm ref}$, hence, $E_{\rm ref}$ enters the ARC block in Fig. 1(b).] Similar to the SAT in (8), the ECC is normally transparent, but modifies $\mathbf{v}_{\rm ref}$ when risk for overcurrent is imminent; see [10] for details. The ARC and ECC blocks, thus, respectively correspond to the CC and SAT blocks in Fig. 1(a), but perform current limitation in the opposite order.

Reference $\mathbf{i}_{\rm ref}$ is in conventional PSC selected as a first-order low-pass filtering of the current itself

$$\mathbf{i}_{\rm ref} = H_a(s)\mathbf{i}, \qquad H_a(s) = \frac{\alpha_a}{s + \alpha_a}. \tag{11}$$

The filter bandwidth α_a is recommended to be selected in the range 0.1–0.2 per unit (p.u.) [20]. The second term in (10) is therefore ensured only to give a transient contribution. A recent enhancement, called reference-feedforward PSC [21], involves instead selecting the d component of $\mathbf{i}_{\rm ref}$ similarly to (7), giving

$$\mathbf{i}_{\rm ref} = i_P^{\rm ref} + jH_a(s)\text{Im}\{\mathbf{i}\}. \tag{12}$$

[For this reason, $P_{\rm ref}$ appears as an input to the ARC block in Fig. 1(b).] This is shown to give improved dynamic performance compared to the conventional selection (11).

[1]If desired, Re$\{\mathbf{E}\}$ can in (9) be replaced by $|\mathbf{E}|$ with minor difference in the dynamic impact, since the dq frame is aligned with the PCC voltage.

The PC, in effect, replaces the PLL. It is given by

$$\theta = \frac{1}{s}[\omega_1 + K_p(s)(P_{\rm ref} - P)]. \tag{13}$$

Often, proportional control is used, i.e., $K_p(s) = K_p$. This yields a frequency droop, i.e., when the instantaneous angular grid frequency $\omega_g = \dot{\theta}$ deviates from the nominal ω_1, the active power will in the steady state deviate from its reference as $P = P_{\rm ref} + (1/K_p)(\omega_1 - \omega_g)$. Inertia emulation can be included in $K_p(s)$ by cascading a first-order low-pass filter [20], yet the same frequency droop is obtained as long as $K_p(0) = K_p$. The droop can be eliminated, if desired, by adding an integral part to $K_p(s)$.

For stability robustness, K_p shall not exceed the following selection recommendation [20]:[2]

$$K_p = \frac{\omega_1 R_a}{\kappa E_{\rm ref}^2}. \tag{14}$$

While the VCC selection recommendation for R_a, (4), is implicit in the desired closed-loop-system bandwidth α_c, for conventional PSC, there is the explicit selection recommendation [20]

$$R_a = 0.2 \text{ p.u.} \tag{15}$$

By not exceeding this recommendation, performance deterioration that could occur for large absolute values of the current operating point $\mathbf{i}_0$ is prevented [20]. Recommendation (15) is used for the evaluation of reference-feedforward PSC in [21] as well. Yet, for this variant, it has not been demonstrated that exceeding (15) results in degrading performance.

III. Unification of VCC and PSC

VCC and PSC obviously have significant structural differences. Yet, by making four modifications of PSC, it is possible to unify the two schemes.

A. Modifications of PSC

1) PCC-Voltage Orientation: Since the second term in the ARC (10) only gives a transient contribution, $\mathbf{v} = \mathbf{V}$ statically. That is, conventional PSC, with $\mathbf{V} = V$, uses the converter voltage as dq-frame reference, whereas VCC uses the PCC voltage. This discrepancy can be amended by instead selecting $\mathbf{V} = E_{\rm ref} + j\omega_1 L\mathbf{i}$. Thereby, (10) is modified to[3]

$$\mathbf{v}_{\rm ref} = \text{ECC}\{R_a(\mathbf{i}_{\rm ref} - \mathbf{i}) + j\omega_1 L\mathbf{i} + E_{\rm ref}\}. \tag{16}$$

Provided that the ECC is transparent, this leads to $\mathbf{E} = E_{\rm ref}$, statically.

[2]The original recommendation is $K_p = \omega_1 R_a/(\kappa V^2)$. $V \to E_{\rm ref}$ to conform with the PSC modifications made in Section III-A.

[3]To make exploiting the similarities to (3) easier, the terms in (16) are placed in different order than in (10).

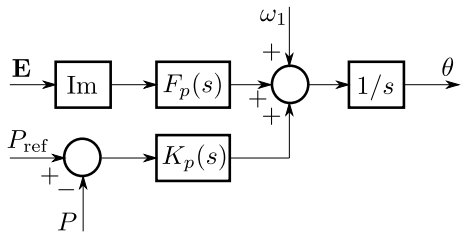

Fig. 3. Hybrid synchronization controller, merging PLL and PC.

2) PLL Addition: PLL action needs to be added to the PC (13) to acquire the correct initial phase angle prior to commencing closed-loop grid-connected operation. In addition, PLL action may be required for fault ride-through [10]. It is straightforward to include PLL action by adding the second term of (6) to (13), yielding the hybrid synchronization controller depicted in Fig. 3, given as

$$\theta = \frac{1}{s}[\omega_1 + F_p(s)\text{Im}\{\mathbf{E}\} + K_p(s)(P_{\text{ref}} - P)]. \tag{17}$$

The PLL addition may be used only during the mentioned situations [22]. Alternatively, it may be used at all times, thus, introducing a permanent grid-following feature to the synchronization control of PSC.

Remark 1: A related scheme is presented in [23]. It differs in that the PLL uses its own dq-frame angle, whereas in (17), θ is common for the PC and the PLL. Unlike (17), the PLL in [23] does not contribute to synchronization, it merely eliminates the PC-induced frequency droop.

3) Alternative Current-Reference Selection: Via the feedback of $\mathbf{i}$ in the modified ARC (16), a closed-loop system is formed. Assuming that the ECC is transparent and $\mathbf{v} = \mathbf{v}_{\text{ref}}$, this system can be found by combining (16) with the dq-frame relation $(s + j\omega_1)L\mathbf{i} = \mathbf{v} - \mathbf{E}$ (obtained by inspecting Fig. 1) and solving for $\mathbf{i}$, giving

$$\mathbf{i} = G_c(s)\mathbf{i}_{\text{ref}} + Y_c(s)(E_{\text{ref}} - \mathbf{E}) \tag{18}$$

where

$$G_c(s) = \frac{R_a}{sL + R_a} \qquad Y_c(s) = \frac{1}{sL + R_a}. \tag{19}$$

Next, current-reference selection (11) for conventional PSC is taken into account by substituting (18) in (11) and solving for $\mathbf{i}_{\text{ref}}$, yielding

$$\mathbf{i}_{\text{ref}} = Y_r(s)(E_{\text{ref}} - \mathbf{E}) \tag{20}$$

where

$$\begin{aligned} Y_r(s) &= \frac{Y_c(s)H_a(s)}{1 - G_c(s)H_a(s)} = \frac{\alpha_a}{s[(s + \alpha_a)L + R_a]} \\ &\approx \frac{\alpha_a}{s(sL + R_a)} \end{aligned} \tag{21}$$

the approximation assuming $\alpha_a L \ll R_a$, which generally holds. This is an interesting result. It shows that (11) can be recast as an integral AVC (with a cascaded low-pass filter), whose gain is proportional to the bandwidth of filter $H_a(s)$. Equation (20) can be implemented in place of (11), under the stated assumptions with unchanged dynamic properties.

Adding i_P^{ref} to (20), a hybrid between conventional and reference-feedforward PSC is obtained. This allows the current-reference selection to conform with (8), less SAT

$$\mathbf{i}_{\text{ref}} = i_P^{\text{ref}} + \underbrace{Y_r(s)(E_{\text{ref}} - \mathbf{E})}_{\text{AVC}(E_{\text{ref}},\mathbf{E})}. \tag{22}$$

The resulting closed-loop system is found by substituting (22) in (18), giving

$$\mathbf{i} = G_c(s)i_P^{\text{ref}} + Y_c'(s)(E_{\text{ref}} - \mathbf{E}) \tag{23}$$

where

$$Y_c'(s) = \frac{s + \alpha_a}{s[(s + \alpha_a)L + R_a]} \approx \frac{s + \alpha_a}{s(sL + R_a)}. \tag{24}$$

4) Replacement of ECC by SAT: At a glance, it could be surmised that adding SAT to (22), making it identical to (8), would prevent overcurrent. This would allow removing the ECC from the modified ARC (16), increasing its similarity to the CC (3). Yet, the third term in (16), E_{ref}, differs from the third term in (3), $H(s)\mathbf{E}$. The inclusion of $H(s)\mathbf{E}$ in (3) is a necessity for overcurrent prevention, since it acts to cancel disturbances in $\mathbf{E}$ that are within the bandwidth of $H(s)$. On the other hand, the inclusion of E_{ref} in (16) gives voltage stiffness, which is a prerequisite for grid-forming control. The solution to this dilemma is to add a proportional term to the AVC in (22), as

$$\text{AVC}(E_{\text{ref}}, \mathbf{E}) = \frac{1}{R_a}[E_{\text{ref}} - H(s)\mathbf{E}] + Y_r(s)(E_{\text{ref}} - \mathbf{E}). \tag{25}$$

The current reference is then formed according to (8) and fed to the CC (3), see Fig. 2. When SAT in (8) is transparent, term $-H(s)\mathbf{E}/R_a$ in (25) multiplies with R_a in (3) and cancels term $H(s)\mathbf{E}$, putting E_{ref} in its place. Thereby, (3) effectively turns into (16) (but, as desired, less ECC). Consequently, for normal operation when SAT is transparent, the PCC-voltage feedforward term in (3) is inactive, whereas it helps to prevent overcurrent during abnormal events when SAT is effectuated. Thus, the closed-loop system (23) remains unchanged.

Since E_{ref} is considered constant and $H(0) = 1$, we get $H(s)E_{\text{ref}} = E_{\text{ref}}$. Hence, (25) can more compactly be expressed as

$$\text{AVC}(E_{\text{ref}}, \mathbf{E}) = Y_v(s)(E_{\text{ref}} - \mathbf{E}), \;\; Y_v(s) = \frac{H(s)}{R_a} + Y_r(s). \tag{26}$$

With R_a and $H(s)$ selected according to (4), $Y_v(s) = Y_c'(s)$ as given by (24), repeated here for convenience, also rearranged to explicitly show the structure of a proportional–integral controller cascaded with a low-pass filter, as

$$Y_v(s) = \frac{s + \alpha_a}{s(sL + R_a)} = \frac{s + \alpha_a}{sR_a}H(s). \tag{27}$$

B. Similarity of the PSC AVC to "Active Damping" VCC Schemes

PSC was originally invented to facilitate a stable interconnection with a very weak grid [24]—a situation where VCC often fails to give stability. One reason for the success is the usage of a PC instead of a PLL. The unification of VCC and

PSC indicates another reason: a significantly different AVC. While the AVC (9) conventionally used in VCC is asymmetric and couples from d to q, the PSC AVC (26) is symmetric and real, coupling from d to d and from q to q.

Interestingly, similar schemes have been proposed for stability enhancement of VCC, often termed "active damping." In [14], a real bandpass filter connects (in our terminology) $\mathbf{E}$ to $\mathbf{i}_{\rm ref}$. Since a proportional–integral CC is used, the net result is somewhat similar to (26) with $\alpha_a = 0$, since the pole at $s = 0$ of the CC cancels the zero at $s = 0$ of the bandpass filter. The scheme proposed in [15] is similar to (26) with $\alpha_a = 0$, but, in addition, proposes to let the "active damping" act via an auxiliary, slow, PLL. This is because the impact of the regular PLL, within the PLL bandwidth, tends to nullify the effect of the "active damping" in the q-to-q signal path. In [16], this problem is instead tackled by using an integrating "active damping" scheme in the q-to-q signal path, in a similar fashion as the q-to-q coupling in (26). The similarity to "active damping" schemes serves as another explanation to the good stability properties of PSC in weak grids. It also suggests that adding a PLL to the PC according to (17) may not degrade the stability properties (subject to further investigation).

There are also similarities to the "synchronous power controller" proposed in [12]. The fundamental differences are that the CC is implemented in the $\alpha\beta$ frame, that the AVC is a resistive–inductive virtual admittance (which is equivalent to a proportional controller cascaded with a low-pass filter), and that the active power is controlled via the angle of the voltage reference (in our terminology $\mathbf{E}^s_{\rm ref}$).

C. PSC as Guideline for Robust VCC Design

Since the PSC AVC (25) resembles an "active damping" scheme, it can directly be applied for a robust VCC design, i.e., one that achieves stability and good performance irrespective of the grid strength, where weak grids are particularly challenging. VCC implies the usage of a conventional AVC according to (9). A hybrid AVC—or, equivalently, a conventional AVC together with "active damping"—is obtained by adding (9) to (26), giving

$$\text{AVC}(E_{\rm ref}, \mathbf{E}) = Y_v(s)(E_{\rm ref} - \mathbf{E}) - jF_v(s)(E_{\rm ref} - \text{Re}\{\mathbf{E}\}). \tag{28}$$

Here, $Y_v(s)$ can be generalized as

$$Y_v(s) = G_a \frac{s + \alpha_a}{s} H(s) \tag{29}$$

where $G_a = 1/R_a$ gives (27). This can be considered as the "ultimate gain," where term $H(s)\mathbf{E}$ in (3) is cancelled and replaced by $E_{\rm ref}$ (for SAT transparent). For $G_a = 0$, (28) reverts to the conventional AVC. Gain selections between these extremes represent the grey zone between grid-following and grid-forming controls with regard to voltage stiffness.

The obtained scheme is structurally identical to that in [15], except that an auxiliary PLL is not used. While the "active damping" in [15] is proportional only, $Y_v(s)$ is (for $\alpha_a > 0$) proportional–integral with a cascaded low-pass filter. Unlike [15], $Y_v(s)$ is, with $G_a = 1/R_a$, analytically parametrized, obviating empirical tuning.

VCC implies, in addition, that a PLL is used instead of a PC. Since these are two very different principles for synchronization control, the PC gain-selection recommendation (14) cannot be translated to a PLL design recommendation. On the other hand and perhaps somewhat surprisingly, it can provide a guideline for the design of $F_v(s)$, as we shall now show. Adding the conventional AVC as in (28) modifies the closed-loop system (23) to

$$\mathbf{i} = G_c(s)i_P^{\rm ref} + Y_c'(s)(E_{\rm ref} - \mathbf{E}) - jG_c(s)F_v(s)(E_{\rm ref} - \text{Re}\{\mathbf{E}\}). \tag{30}$$

The PC gives a dq-frame dynamic impact via the dq and $\alpha\beta$ transformations made in the control system. Similar to the PLL impact, it is nonlinear and linearization gives dependence on the current operating point $\mathbf{i}_0$ [5]. As shown in the Appendix, for negligible $\mathbf{i}_0$ and α_a, the impact is structurally identical to (30), namely

$$\begin{aligned}\mathbf{i} =& G_c(s)i_P^{\rm ref} + Y_c'(s)(E_{\rm ref} - \mathbf{E}) \\ & - j\frac{\kappa K_p E_{\rm ref}^2 G_c^2(s)}{R_a^2 s}(E_{\rm ref} - \text{Re}\{\mathbf{E}\}).\end{aligned} \tag{31}$$

By selecting

$$F_v(s) = \frac{\kappa K_p E_{\rm ref}^2 G_c(s)}{R_a^2 s} = \frac{\omega_1 G_c(s)}{R_a s} = \frac{\omega_1}{s(sL + R_a)} \tag{32}$$

where the second equality is obtained by applying (14), (30) and (31) become identical. The result is an analytically parametrized integral controller, cascaded with a low-pass filter. Coincidentally, it is identical to (21) with $\alpha_a = \omega_1$. If (4) is followed, $G_c(s) = H(s)$ in (32). In addition, a generalization of the gain similarly to (29) can be made, as

$$F_v(s) = \frac{K_v}{s} H(s) \tag{33}$$

where (32) is obtained by letting $K_v = \omega_1/R_a$.

Fig. 4 illustrates (8) and (28) in dq-to-dq signal paths (i.e., in component form). Notice that the integrator of the conventional AVC and that in the q-to-q signal path of the PSC AVC are merged together.

Remark 2: Recommendations (28) and (32) give VCC [with $K_p(s) = 0$ in (17)] designed so that the small-signal dynamics are identical to those of PSC [with $F_p(s) = F_v(s) = 0$ in (17)], for negligible $\mathbf{i}_0$ and α_a as well as negligible PLL dynamics [as the latter are not accounted for in (30)]. Therefore, it is expected that the VCC design will inherit the robustness to the grid strength of reference-feedforward PSC demonstrated in [21]. Performance comparisons without the mentioned restrictive assumptions are made in the next section.

Remark 3: If $K_p(s) = 0$, it is necessary to choose $\alpha_a = 0$, at least for the integrator gain in the d-to-d signal path of Fig. 4. This is because without a PC, the active-power control is open loop, facilitated by (7). Consequently, nothing prevents the mentioned integrator from accumulating a bias which adds to $i_d^{\rm ref}$, giving a nonzero static control error $P_{\rm ref} - P$. The q-to-q signal path does not pose a similar problem; because of the merging of integrators, a bias will not be accumulated.

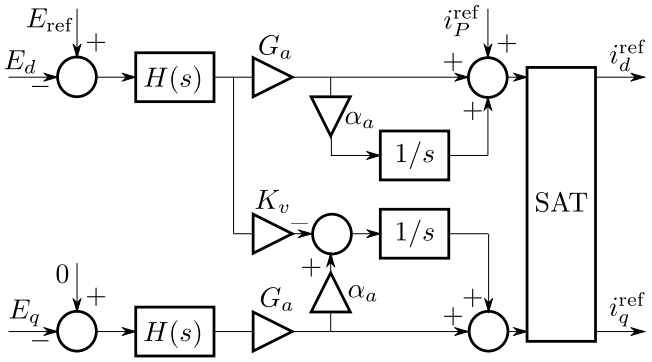

Fig. 4. Current-reference computation resulting from (8) and the hybrid AVC (28), shown in dq-to-dq signal paths.

TABLE I
EXPERIMENTAL SETUP DATA

Variable/parameter	Actual value	Normalized value
Rated power	12.5 kVA	1 p.u.
Rated voltage	$\sqrt{2/3} \cdot 400$ V	1 p.u.
Rated current	$\sqrt{2} \cdot 18$ A	1 p.u.
Maximum current	$1.5 \cdot \sqrt{2} \cdot 18$ A	1.5 p.u.
Base impedance	12.8 Ω	1 p.u.
Filter inductance L	3.3 mH	0.081 p.u.
Filter resistance R	0.51 Ω	0.040 p.u.
Filter capacitance C	8.8 μF	0.036 p.u.
Fundamental frequency	50 Hz	1 p.u.
Rated dc-bus voltage	650 V	2 p.u.
Sampling frequency	10 kHz	200 p.u.
Switching frequency	5 kHz	100 p.u.

TABLE II
PARAMETER SELECTIONS

	K_p	α_a [p.u.]	α_p [p.u.]	$F_v(s)$
PSC	(14)	0.1	0	0
VCC	0	0	0.1	(32)
HYB	0.5×(14)	0.1	0.1	0.5×(32)

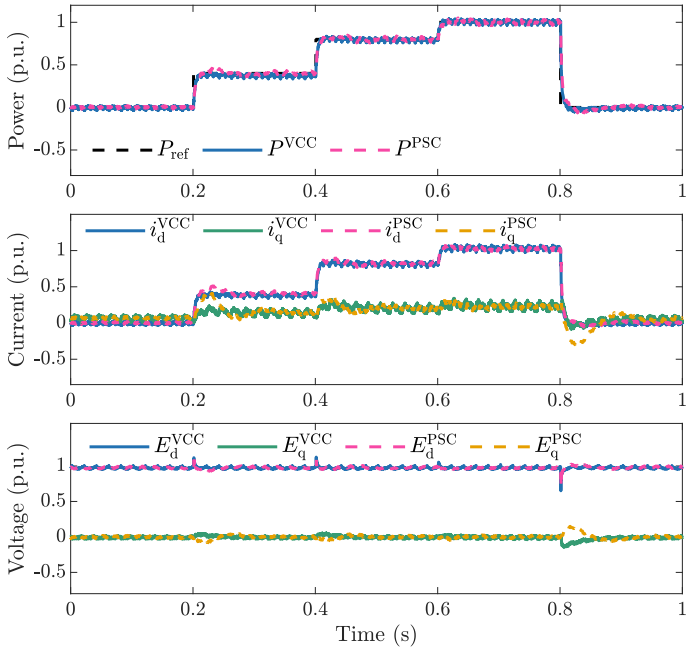

Fig. 5. Power-reference step responses for SCR $= 5$ and $\alpha_c = 4$ p.u.

IV. EXPERIMENTAL EVALUATION

The derived universal controller, defined by Figs. 2, 3, and 4, is here evaluated experimentally. The setup—see Table I for data—uses back-to-back converters, allowing the dc-bus voltage to be controlled from the converter not under consideration. Filter resistance R is determined empirically and includes the converter losses. In addition, there is a shunt capacitor (with capacitance C) at the PCC, forming an inductive–capacitive–inductive (*LCL*) filter with the grid inductance L_g. Three different values of L_g are considered, as defined by the short-circuit ratio (SCR), which is the inverse p.u. value of $L + L_g$. For the considered SCR $= \{5, 2, 1\}$, the *LCL*-filter resonance is respectively $\{24, 20, 19\}$ p.u., all values within the range recommended in [25], to avoid induction of high-frequency instability due to the lag in the effectuation of $\mathbf{v}_{\text{ref}}^s$.

Evaluations are made for the parameter selections that, respectively, give PSC (including the modifications in Section III-A) and VCC (with PSC as design guideline, as described in Section III-C). The differing parameters are detailed in Table II, where the third row represents the suggestion for a PSC/VCC hybrid, which is evaluated in one test only. R_a and $H(s)$ are common and selected according to (4), while $G_a = 1/R_a$ in the AVC (28). The synchronization controller (17), see Fig. 3, employs proportional-only PLL and PC, parametrized respectively as $F_p(s) = \alpha_p/E_{\text{ref}}$, where α_p is the desired PLL closed-loop bandwidth [5], and $K_p(s) = K_p$. Since the filter resistance is nonnegligible, a compensation term $R\mathbf{i}_{\text{ref}}$ is added to the CC (3). Reflecting a grid voltage slightly lower than the rated, $E_{\text{ref}} = 0.975$ p.u.

One fundamental objective is robust performance, i.e., it should be possible to successfully use the same controller, without retuning, irrespective of the SCR. Therefore, evaluation is made for SCR $= \{5, 2, 1\}$, respectively representing a (relatively) strong, a weak, and a very weak grid. Identically to [21], the test sequence involves four reference steps, to $P_{\text{ref}} = \{0.4, 0.8, 1, 0\}$ p.u. respectively at $t = \{0.2, 0.4, 0.6, 0.8\}$ s. In addition to the comparisons of time traces, the average absolute active-power control error $\overline{|P_{\text{ref}} - P|}$, as computed over the displayed time interval, is considered as performance index.

A. Strong Grid, SCR $= 5$

To challenge design recommendation (15) for conventional PSC, we select $\alpha_c = 4$ p.u., giving $R_a = 0.32$ p.u. Fig. 5 shows that VCC and PSC give virtually identical results, with $\overline{|P_{\text{ref}} - P|}_{\text{VCC}} = 0.019$ p.u. and $\overline{|P_{\text{ref}} - P|}_{\text{PSC}} = 0.020$ p.u.

B. Weak Grid, SCR $= 2$

Also in this case, VCC and PSC exhibit similar performance, see Fig. 6. The differences compared to the strong-grid case are longer rise times for both schemes and that VCC gives slight overshoots in P. The latter are consequences of

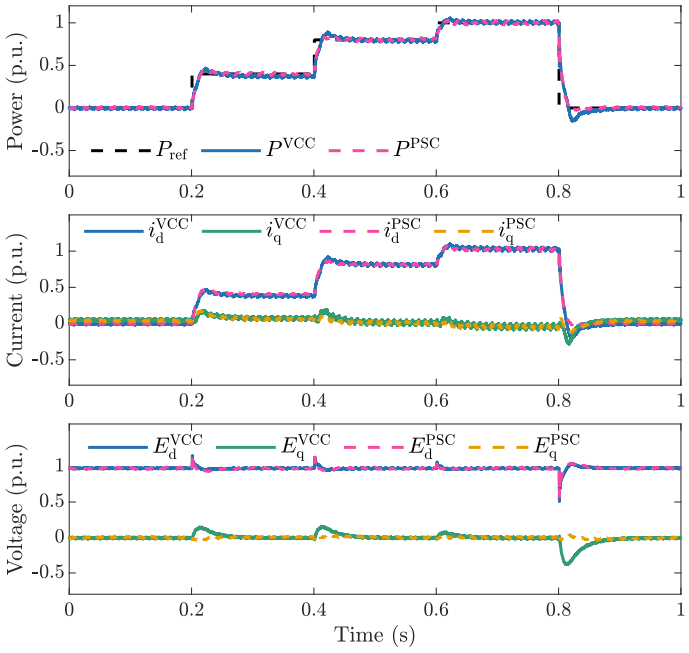

Fig. 6. Power-reference step responses for SCR $= 2$ and $\alpha_c = 4$ p.u.

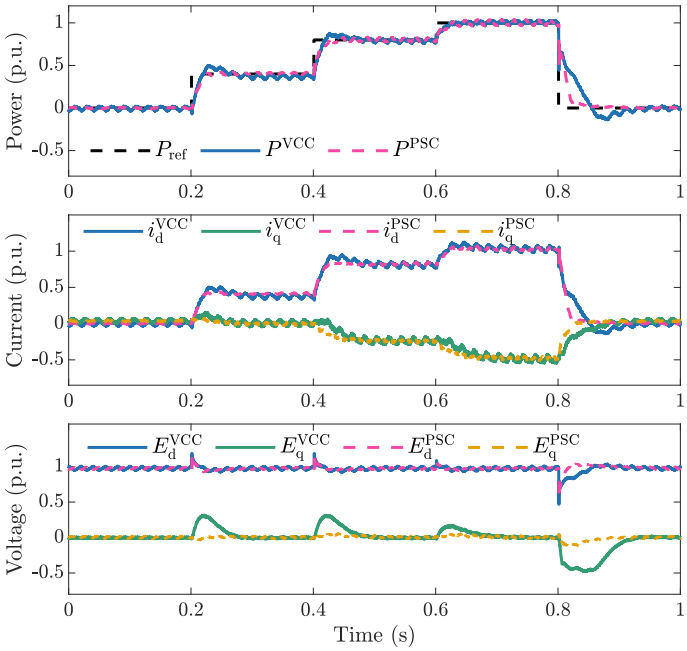

Fig. 7. Power-reference step responses for SCR $= 1$ and $\alpha_c = 4$ p.u.

larger transients in E_q, caused by the use of a PLL instead of a PC. The lack of overshoot awards PSC the slightly better performance index: $\overline{|P_{\text{ref}} - P|}_{\text{PSC}} = 0.018$ p.u., whereas $\overline{|P_{\text{ref}} - P|}_{\text{VCC}} = 0.025$ p.u.

C. Very Weak Grid, SCR $= 1$

The trends observed for SCR $= 2$ are accentuated, see Fig. 7. Particularly for the final step in P_{ref}, PSC performs significantly better than VCC, giving $\overline{|P_{\text{ref}} - P|}_{\text{PSC}} = 0.029$ p.u. and $\overline{|P_{\text{ref}} - P|}_{\text{VCC}} = 0.047$ p.u.

To further challenge (15), another experiment, now with $\alpha_c = 8$ p.u. $\Rightarrow R_a = 0.64$ p.u. is made, see Fig. 8. Here, $\overline{|P_{\text{ref}} - P|}_{\text{PSC}} = 0.015$ p.u. and $\overline{|P_{\text{ref}} - P|}_{\text{VCC}} = 0.062$ p.u., i.e., doubling α_c almost cuts in half the performance index for PSC. The performance index for VCC would have been reduced as well, had it not been for the deteriorated final step response. It can be observed that PSC exhibits slight ringing for $P_{\text{ref}} = 1$ p.u. This phenomenon gradually worsens as α_c is increased beyond 8 p.u., eventually giving instability for $\alpha_c \approx 11.5$ p.u. $\Rightarrow R_a \approx 0.93$ p.u. So, for the modified PSC variant, there is an upper limit for R_a, yet much more generous than recommendation (15).

For completeness, the fault ride-through performance for this operating case is illustrated, see Fig. 9. Here, a symmetric fault is emulated by reducing the grid voltage (denoted in the figure as $\mathbf{u}$) to 50% of the nominal value. Owing to the grid-forming property of both schemes, this leads to injection of reactive current, which restores the PCC voltage to its reference.

D. Hybrid Scheme

The drawback of VCC is found to be step-response overshoot, whereas the drawback of PSC is ringing for operation

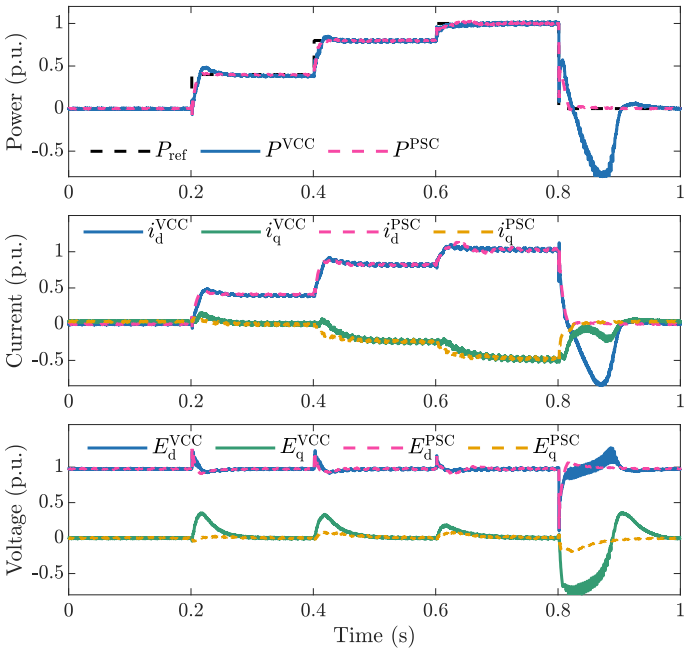

Fig. 8. Power-reference step responses for SCR $= 1$ and $\alpha_c = 8$ p.u.

with large current and large R_a. This suggests that it may be fruitful to explore hybrids between the schemes, with the objective to eliminate the respective drawbacks. One suggestion is the parameter selection shown in the third row of Table II. Since the design (32) of the conventional AVC is based on small-signal dynamic equivalence with the PC, to give a fair comparison, the gains of both are set to half their recommended values. Their summed linearized impact is then ideally unchanged relative PSC and VCC. In addition, α_c is increased to 10 p.u., giving more distinctive ringing

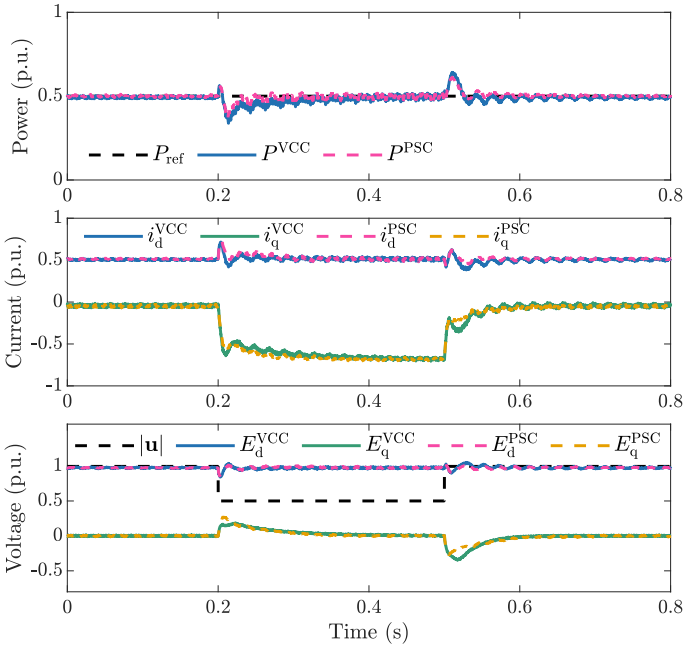

Fig. 9. Fault ride-through for SCR $= 1$ and $\alpha_c = 8$ p.u.

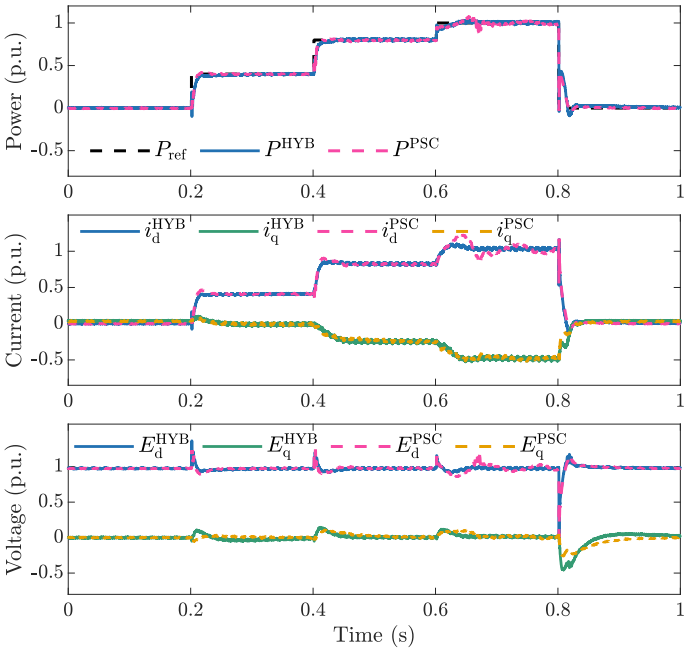

Fig. 10. Power-reference step responses for SCR $= 1$ and $\alpha_c = 10$ p.u.

of PSC for $P_{\text{ref}} = 1$ p.u., see Fig. 10. The hybrid scheme exhibits neither ringing nor overshoot, and its performance index approaches that for PSC: $\overline{|P_{\text{ref}} - P|}_{\text{HYB}} = 0.018$ p.u. versus $\overline{|P_{\text{ref}} - P|}_{\text{PSC}} = 0.015$ p.u.

V. Conclusion

In this paper it was shown that, by making four minor modifications of PSC, this scheme meshes with VCC in a universal controller. This insight was utilized primarily to facilitate a robust VCC design with PSC as guideline. Comparative evaluation of PSC and the robustly designed VCC was made, showing—as expected—overall similar performance, but with some details differing. Dynamic analysis of the universal controller is a suitable topic for further research, as is the exploration of PSC/VCC hybrids and potentially novel variants.

Appendix

The objective is to calculate the linearized dynamic impact of the dq-frame reference angle θ that results for PSC as given by the closed-loop system (23) and the synchronization controller (17) with $K_p(s) = K_p$ and $F_p(s) = 0$. The impact originates from the $\alpha\beta$ transformation of $\mathbf{v}_{\text{ref}}$ as well as the dq transformations to obtain $\mathbf{i}$ and $\mathbf{E}$ that are made in the control system. But since negligible $\mathbf{i}_0$ and α_a are assumed, the effects of the dq transformations vanish. For $\mathbf{i}$ it is because $\mathbf{i}_0 = 0$ quenches the impact and for $\mathbf{E}$ because the proportional part of the AVC cancels with the PCC-voltage feedforward in the CC, leaving only the integral part, whose gain is proportional to α_a, see (27).

Linearizing $\mathbf{v}_{\text{ref}}^s = e^{j\theta}\mathbf{v}_{\text{ref}}$ yields

$$\mathbf{v}_{\text{ref}}^s \approx e^{j\theta_0}(1 + j\Delta\theta)\mathbf{v}_{\text{ref}} \approx e^{j\theta_0}(\mathbf{v}_{\text{ref}} + j\mathbf{v}_0\Delta\theta) \tag{34}$$

where $\mathbf{v}_0 = E_{\text{ref}} + j\omega_1 L\mathbf{i}_0$ is the operating point around which the linearization is made. Owing to the assumption of a negligible $\mathbf{i}_0$, $\mathbf{v}_0 = E_{\text{ref}}$. Furthermore, from (13), $\theta_0 = \int \omega_1\, dt$ and

$$\Delta\theta = \frac{K_p}{s}(P_{\text{ref}} - P). \tag{35}$$

Equation (34) shows that, in the dq frame, the linearized dynamic impact of θ is accounted for by adding $jE_{\text{ref}}\Delta\theta$ to $\mathbf{v}_{\text{ref}}$. Since $\mathbf{v}$ affects $\mathbf{i}$ in the same way as $-\mathbf{E}$, the impact can be calculated by substituting $\mathbf{E} \to \mathbf{E} - jE_{\text{ref}}\Delta\theta$ in (23), giving

$$\mathbf{i} = G_c(s)i_P^{\text{ref}} + Y_c'(s)(E_{\text{ref}} - \mathbf{E} + jE_{\text{ref}}\Delta\theta). \tag{36}$$

Since $\mathbf{i}_0$ is negligible, $\mathbf{i}$ is a small-signal variable. Linearization of the relation $P = \kappa\text{Re}\{\mathbf{E}\mathbf{i}^*\}$ therefore simply implies $\mathbf{E} \to E_{\text{ref}}$, i.e.,

$$P = \kappa E_{\text{ref}}\text{Re}\{\mathbf{i}^*\} = \kappa E_{\text{ref}}\text{Re}\{\mathbf{i}\}. \tag{37}$$

Substituting (36) in (37) yields, with (7)

$$P = G_c(s)P_{\text{ref}} + \kappa E_{\text{ref}}Y_c'(s)(E_{\text{ref}} - \text{Re}\{\mathbf{E}\}). \tag{38}$$

Here, the first term represents the immediate response to a reference change, which occurs with the fairly high bandwidth $\alpha_c = R_a/L$ of $G_c(s)$. The second terms accounts for the response in the PCC voltage, which is markedly slower, as it depends on the grid impedance and the slower-acting PC. Thus, it is reasonable to consider $G_c(s) \approx 1$ in (38), giving $P_{\text{ref}} - P \approx -\kappa E_{\text{ref}}Y_c'(s)(E_{\text{ref}} - \text{Re}\{\mathbf{E}\}) \Rightarrow \Delta\theta \approx -(K_p/s)\kappa E_{\text{ref}}Y_c'(s)(E_{\text{ref}} - \text{Re}\{\mathbf{E}\})$. Substitution of this relation in (36) results in

$$\begin{aligned}\mathbf{i} =& G_c(s)i_P^{\text{ref}} + Y_c'(s)(E_{\text{ref}} - \mathbf{E}) \\ &- j\frac{\kappa K_p[E_{\text{ref}}Y_c'(s)]^2}{s}(E_{\text{ref}} - \text{Re}\{\mathbf{E}\}).\end{aligned} \tag{39}$$

For $\alpha_a = 0$, (24) gives $Y_c'(s) = 1/(sL + R_a) = G_c(s)/R_a$. Substituting this relation in (39) results in (31).

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