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A 30-GHz Switched-Capacitor Power Amplifier for 5G SoCs

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***Abstract*—Switched-capacitor power amplifier has gained popularity within the radio frequency integrated circuit community, since it is CMOS compatible offering high integration density and good performance particularly in terms of linearity. In this paper we present a study on the use of switched-capacitor power amplifier at millimeter-wave frequency range. We identify the major design challenges in this paper, and demonstrate the feasibility of switched-capacitor power amplifier with a 30-GHz design case. Our analysis describes the effects of power amplifier device parasitics and their contribution to dynamic power consumption, revealing that these are a major factor in degradation of switched capacitor power amplifier efficiency at millimeter waves. Two circuits, one for 3 GHz and the other for 30 GHz, were designed and simulated with 28-nm bulk CMOS technology. At 3 GHz, the designed switched capacitor power amplifier structure with 6-bit resolution features maximum output power of 19.4 dBm and efficiency of 59% whereas the output power of 18.6 dBm with 21% efficiency is achieved at 30 GHz. The switched-capacitor power amplifier preserves its good linearity at higher frequencies as well, and our design demonstrates an adjacent channel leackage ratio of -34.4 dB at 30 GHz for a 100-MHz OFDM-modulated signal.**

I. Introduction

Evolution of integrated microwave circuits is driven by three major trends. On application side new communication bands are introduced e.g. by the 5G New Radio (NR), and microwave sensors and radars are becoming ubiquitous in our daily life. At paradigm level we are observing the translation from single-block designs to system-on-chip (SoC) level integration. Thirdly, nanometer-scale CMOS technology offers adequate performance of the active devices at millimeter-wave frequencies and enables high integration density.

From transceiver integration point of view, one of the key elements is the power amplifier. Its contribution on die area and power consumption is significant, while high performance with a modulated signal is essential. Switched-capacitor power amplifier (SCPA) has become a popular PA concept in the RF IC domain, since the structure is CMOS friendly, i.e., easy to integrate, and it provides high linearity [1]. Until now SCPAs have been demonstrated at RF frequencies below 5 GHz [2]–[5], and there has been some doubts about the feasibility of this concept at higher frequencies.

In this paper we are examining the potential of SCPA at microwaves. We review the operation of the SCPA in Section II, and point out the high frequency design challenges. In Section III, we describe 3-GHz and 30-GHz versions of a 6-bit SCPA circuit, designed for 28-nm bulk CMOS technology.

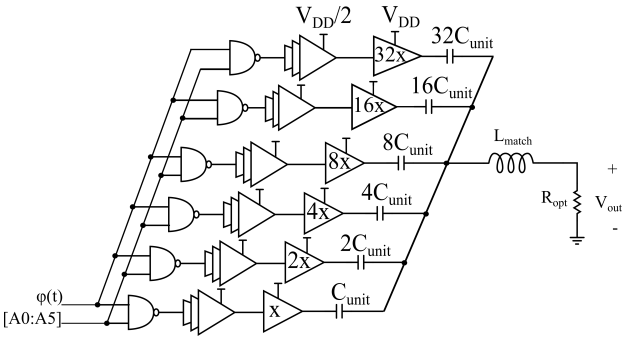

Fig. 1: Block level diagram of an 6-bit SCPA.

Section IV presents the simulation results of these circuits with 100-MHz and 400-MHz OFDM-modulated signals. The performance is compared at 3 GHz and 30 GHz in order to identify high frequency challenges and their effects on SCPA performance. Results indicate the feasibility of the SCPA concept also at 5G New Radio FR2 frequencies at 20-40 GHz. Finally, the conclusions are given in Section V along with further directions.

II. Operation of Switched-Capacitor PA

Switched power amplifiers have emerged as basic entity for highly efficient digital transmitters [6]–[9]. This popularity owes to the technology scaling and digital nature of rail-to-rail signalling [4]. An SCPA employs several switching PAs, typically class-D, connected in parallel acting as a voltage source for the capacitor array as shown in Fig. 1. The PA units are switching ON/OFF the capacitor array where the switching logic is dictated by the input code $A_1 - A_N$ along with phase modulated input signal $\varphi(t)$. By selecting an appropriate code, the selected PA units drive a combination of capacitors C_{ON} whereas the unselected ones (C_{OFF}) are held at signal ground. The capacitances driven ON/OFF are $C_{ON} = (n/N)\,C$ and $C_{OFF} = \left(\frac{N-n}{N}\right) C$ where $n = 1 \ldots N$ and C represents the total capacitance of the array. As a consequence, a capacitance-ratio dependent voltage division takes places at the output node, given by

$$V_{scale}(t) = V_{DD}\left(\frac{C_{ON}}{C}\right) = V_{DD}\left(\frac{C_{ON}}{C_{ON} + C_{OFF}}\right) \quad (1)$$

The scaled signal V_{scale} flows through the output resonator generating the RF fundamental signal V_{out}. SCPA is designed

for a certain output power with a load impedance R_{opt}. The maximum output power is achieved when all the capacitors are switched ON resulting into $P_{out,max}$ across R_{opt}. Furthermore, the output power P_{out} is also dependent on the PA device sizes which affect the turn-ON resistance r_{ON}. This resistance r_{ON} can be minimized by choosing optimally large PA device sizes. The output power is given by

$$P_{out} = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2 \left[\frac{Vdd^2}{R_{opt}\left(1+\frac{r_{ON}}{R_{opt}}\right)}\right] \tag{2}$$

The efficiency of SCPA, given by Eq. 3, is denoted by the system efficiency (SE) that contains the various power consumption elements of the SCPA operation:1) The dynamic power required to charge/discharge the capacitor array having capacitance C is given by P_{sc}. 2) The term P_{sw} describes the power drained to the input and output capacitance C_{sw} of the PA units. 3) The driver stage and input stage are accounted for with P_{drv} and P_{clk} respectively.

$$SE = \frac{P_{out}}{P_{out}+P_{sc}+P_{sw}+P_{drv}+P_{clk}} \tag{3}$$

An SCPA intrinsically employs rail-to-rail switching at these frequencies. Indeed, the switching operation is limited by the transistor transition frequency f_T and the SCPA switching frequency f. The ratio f_T/f mandates the ON/OFF time of PA units and its effect worsen for larger switching frequencies. Therefore, the reduction in SCPA efficiency and output power P_{out} is obvious at higher frequencies [10].

The dimensions of passive devices are reduced significantly at millimeter-wave frequencies. This aspect leads to passive components which are comparable to active devices (ie. PA units in SCPA) with respect to dimensions. In particular, the PA units have intrinsic parasitics which are comparable to the on-chip passives being driven i.e. the capacitor array. To analyze the parasitics and their effect on power consumption of SCPA, consider the four-transistor cascode stage shown in Fig. 2 which is the driving stage for the capacitor array. This PA unit consist of PMOS devices M_P and NMOS devices M_N having gate and drain capacitances $C_{gg} \approx C_{gs}+C_{gd}$ and $C_{dd} \approx C_{gd}+C_{ds}$ respectively. These device parasitics are comparable to the unit capacitance C_{unit} ie., $C_{gg}+C_{dd} \approx kC_{unit}$. Similarly, the input/output capacitance of all PA unit devices C_{sw} can be related to the total capacitance of the array being driven by $C_{sw} \approx kC$ as shown in Eq. 4. It states that the switching loss P_{sw} is equivalent to driving the whole capacitor array when all PA units are switched ON i.e. $n = N$ and $k \geq 1$. The factor k scales P_{sw} depending on the device parasitics and the capacitance of the array.

$$P_{sw} = \left(\frac{n}{N}\right) C_{sw} V_{DD}^2 f \approx \left(\frac{n}{N}\right) kCV_{DD}^2 f \tag{4}$$

The intrinsic capacitances are also reflected in the PA unit output namely $C_{out} \approx \alpha C_{unit}$ where the factor α is also dependent on the PA devices as shown in Fig. 2. This capacitance adds to the capacitance C_{unit} which implies that the PA units need to drive additional capacitance. To model

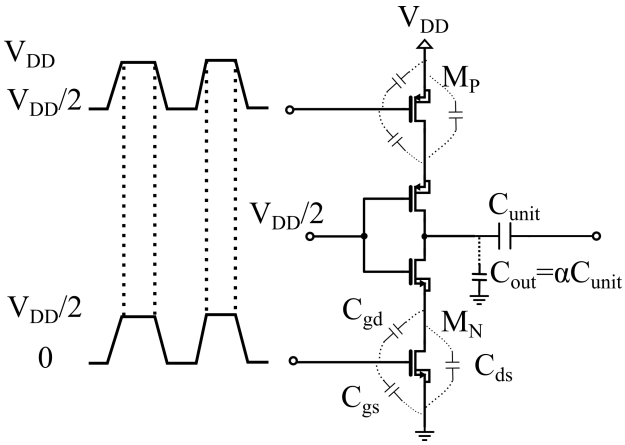

Fig. 2: A single PA unit of SCPA.

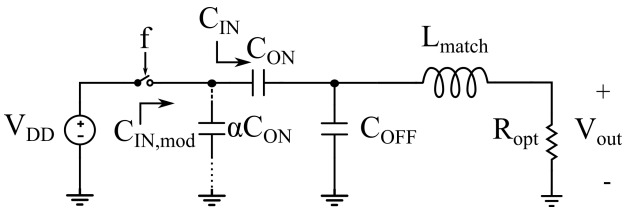

Fig. 3: Equivalent circuit for input capacitance.

this effect, the equivalent circuit of an N-bit SCPA is presented in Fig. 3. In this circuit, the overhead capacitance is desribed as αC_{ON} which modifies the input capacitance C_{IN} seen by PA units to $C_{IN,mod}$. The modified input capacitance $C_{IN,mod}$ and respective power P_{sc} are

$$\begin{aligned} C_{IN,mod} &= \alpha C_{ON} + C_{IN} \\ &= \alpha\frac{n}{N}C + \frac{n}{N^2}(N-n)C \\ &= \frac{n}{N}C\left[\alpha + \left(1-\frac{n}{N}\right)\right] \end{aligned} \tag{5}$$

$$\begin{aligned} P_{sc} &= C_{IN,mod}V_{DD}^2 f \\ &= \left[\frac{n}{N}.\left(\alpha+\left(1-\frac{n}{N}\right)\right)\right] CV_{DD}^2 f \end{aligned} \tag{6}$$

Eq. 6 depicts that the dynamic loss P_{sc} has increased by the factor α which corresponds to additional power consumption. The factor α can be determined from the relation $\alpha \approx C_{dd}/C_{unit}$. Ideally, the dynamic power P_{sc} is minimum for $n = 0$ or $n = N$ and maximum at $n = N/2$. However, Eq. 6 shows that the dynamic power P_{sc} is not zero for $n = N$. It is shown with analysis that the factors k and α express device parasitic effects in terms of dynamic power loss. Larger parasitic effects ie., $k > 1$ and $\alpha > 1$ leads to increased dynamic losses which deteriorates the SCPA efficiency. For an SCPA at millimeter waves with $n = N$, the maximum efficiency SE_{max} is

$$\begin{aligned} SE_{max} &\approx \frac{P_{out}}{P_{out}+P_{sw}+P_{sc}} \\ &= \frac{P_{out}}{P_{out}+(k+\alpha)CV_{DD}^2 f} \end{aligned} \tag{7}$$

III. Circuit Implementation

An 6-bit SCPA is designed for 5G NR FR2 operating at 30 GHz and implemented in 28-nm CMOS technology as shown in Fig. 1. It consists of binary weighted PA units with MOM capacitor array $C_{unit} - 32C_{unit}$ and matching inductor L_{match}. Each PA unit comprises of a 4-transistor cascode topology built with 0.9 V transistors as discussed in Section II. The switching logic and the drivers are implemented as an ideal blocks. The 30-GHz SCPA performance is demonstrated and compared with another SCPA designed for operation at 3 GHz in order to highlight the millimeter wave design challenges and their effects on SCPA output power and efficiency. All devices including the passives have foundry provided mm-wave models that are valid in those frequency ranges. Table I presents the design parameters along with the PA unit device parasitics for 3 GHz and 30 GHz, respectively. For an N-bit binary SCPA design at frequency f, the design parameters are $C = 2^{N-1}C_{unit}$ and $L_{match} = 1/(2\pi f R_{opt} C)$.

TABLE I: SCPA design parameters

Frequency (GHz)	3	30
C (pf) / C_{unit} (fF) / L_{match} (pH)	6.63 / 442 / 420	0.663 / 44.2 / 42
C_{gg}/ C_{dd}/ C_{sw} (fF): M_P	58 / 40 / 98	
C_{gg}/ C_{dd}/ C_{sw} (fF): M_N	45 / 34 / 79	
$k = C_{sw}/C_{unit}$: M_P/M_N	0.23 / 0.18	2.3 / 1.8
$\alpha = C_{dd}/C_{unit}$: M_P/M_N	0.1 / 0.08	1 / 0.77

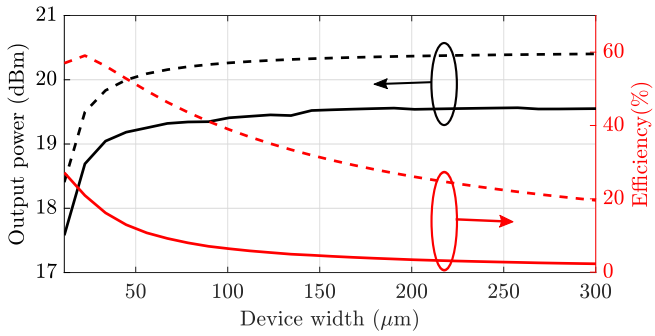

Fig. 4: Peak efficiency and output power for various PA device widths: 3 GHz (dashed) and 30 GHz (solid).

To determine the optimal device sizes in each PA unit, the SCPA design is simulated at 3 GHz and 30 GHz for various PA device widths. The optimal sizing results into maximum efficiency achievable for a given SCPA circuit. Fig. 4 describes the peak efficiency and corresponding output power for 3 GHz with optimal PA unit device widths $20\,\mu m \sim 50\,\mu m$ while the 30 GHz case should have device widths less than $50\,\mu m$. For 30 GHz, the device width greater than $50\mu m$ leads to increased switching losses. Therefore, a larger device requires trade off with reduced efficiency. The optimal device widths for PMOS / NMOS $(M_P/M_N : 25\,\mu m/22\,\mu m)$ are selected for both frequencies in order provide fair comparison. The associated device parasitics are presented in Table I. At 30 GHz, it can be seen that the factors relating device parasitics, $1.8 < k < 2.3$ and $0.77 < \alpha < 1$, are mainly contributing towards dynamic losses as shown in Eq. 7.

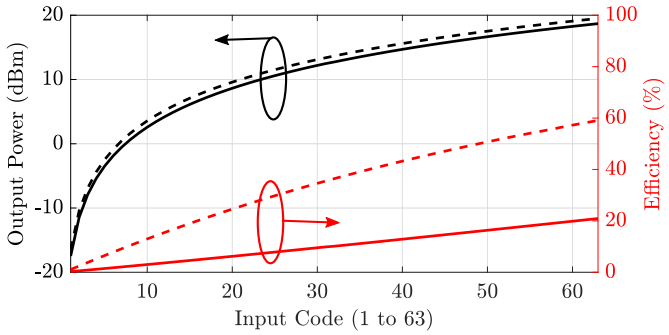

Fig. 5: Comparison of simulated output power and efficiency versus input code for 3 GHz (dashed) and 30 GHz (solid) cases.

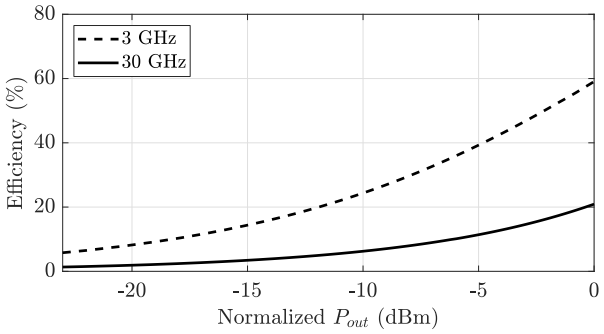

Fig. 6: Comparison of simulated output power vs efficiency.

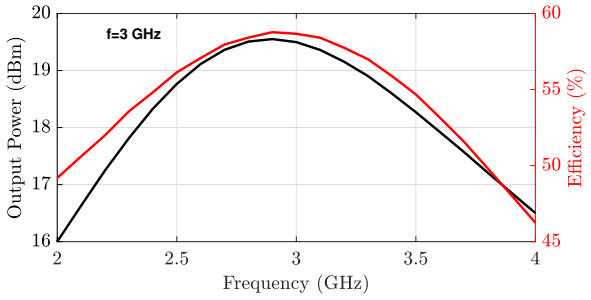

Fig. 7: Case 3 GHz: Simulated output power and efficiency versus frequency.

IV. Simulation Results

The effect of dynamic losses in SCPAs are investigated with simulations. The SCPA performance metrics illustrated in Fig. 5−Fig. 8 verifies that the output power of SCPA has

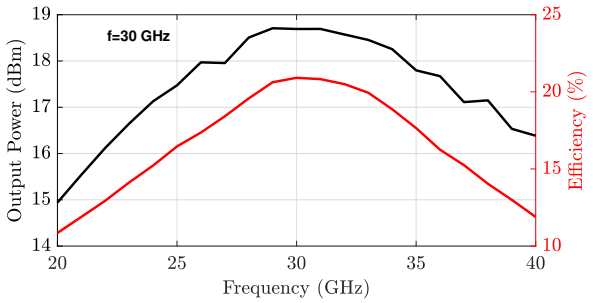

Fig. 8: Case 30 GHz: Simulated output power and efficiency versus frequency.

slightly reduced by 0.8 dB at 30 GHz. In particular, the SCPA features output power and efficiency of 19.4 dBm / 59% at 3 GHz while achieving 18.6 dBm / 21% at 30 GHz. The efficiency deterioration is significant which proves that the switching losses in SCPA has significantly increased. Hence, the device parasitics and high switching losses are the major factors contributing towards dynamic power consumption which in fact degrades SCPA efficiency at mm-waves. An OFDM modulated signal with bandwidths 100 MHz and 400 MHz is also applied to both SCPA structures to determine the ACLR performance. Fig. 9 shows the SCPA output signal spectrum at 3 GHz and 30 GHz respectively. At 30 GHz, an ACLR of -34.4 dB was observed for 100 MHz OFDM modulated signal while demonstrating -32.8 dB for 400 MHz signal.

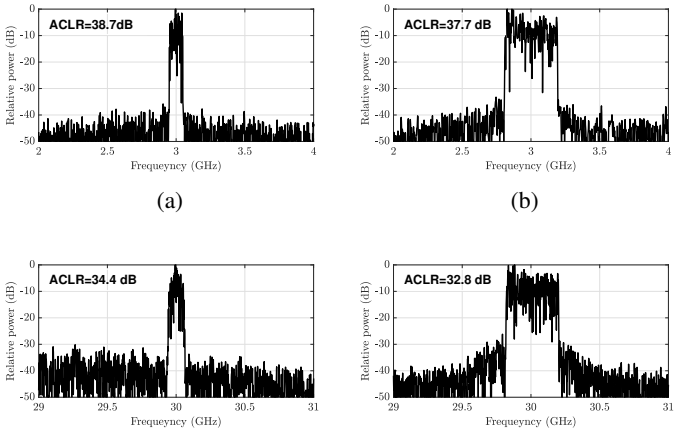

Fig. 9: Simulated ACLR of SCPAs for (a)–(b) 3 GHz case and (c)–(d) 30 GHz case with 100 MHz and 400 MHz OFDM signal.

V. Conclusions

Switched-capacitor power amplifier consists of a capacitor and switched-mode amplifier array. Amplifier is typically class-D configuration, which is in essence a CMOS inverter - the very fundamental element of modern integrated electronics. Thus, SCPA is highly suitable candidate for System-on-Chip level integration. In this paper we have studied a SCPA circuit operating at 30 GHz. The basic operation and challenges at high-frequency switching were analyzed. The effect of device parasitics on SCPA efficiency was analyzed, and verified with transistor-level simulations for two test cases at 3 GHz and 30 GHz respectively. The results show that the output power and efficiency at 3 GHz, 19.4 dBm / 59%, drop to 18.6 dBm / 21% at 30 GHz. Linearity of the SCPA was simulated with 100-MHz and 400-MHz bandwidth OFDM-modulated signals. Corresponding ACLR values of -38.7 dB and -37.7 for 3 GHz case, and -34.4 dB and -32.8 dB for 30-GHz case demonstrate that SCPA preserves sufficient linearity at millimeter-wave frequencies as well. Degradation in power efficiency can be tolerated in such designs where the PA contribution to overall power budget is moderate, like for short range 5G links where majority of the power budget goes for digital signal processing.

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