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A 1.5–5-GHz Integrated RF Transmitter Front End for Active Matching of an Antenna Cluster

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***Abstract*— A recently proposed method for realizing frequency-reconfigurable antennas across a wideband is based on adjusting the feed amplitudes and phases of a multiport antenna. In this article, we demonstrate the feasibility of the method, for the first time, with a conjunction of an integrated RF transmitter and a four-element antenna cluster. The implementation performs on-chip amplitude and phase tuning with supply scaling and delay tuning circuits to tune the antenna cluster without requirement of matching network. The antenna cluster is built with four closely spaced antenna elements implemented on a printed circuit board. The transmitter integrated circuit (IC) is implemented in a 28-nm CMOS process with the chip size of 0.85 mm × 0.95 mm, including pads. The proof-of-concept implementation demonstrates tunability across a wideband from 1.5 to 5 GHz.**

***Index Terms*— Multiport antenna, reconfigurable antenna, transmitter, wideband antenna tuning.**

I. Introduction

With the proliferation of new radio standards, the wireless devices need to operate across ever wider range of spectrum. To ensure operation in the densely populated sub-6-GHz spectrum, the current challenge is to realize a frequency tunable or reconfigurable antenna with a wide tuning range. On the other side, it makes the RF front-end design an arduous task to achieve multiband communication. In particular, the integrated transmitter requires wideband matching networks for multiband transmission, which significantly deteriorates the device form factor. Traditionally, a reconfigurable antenna can support more than one frequency band (noncontiguous) via p-i-ndiodes [1]–[6] or varactor diodes [7]–[10], though linearity, power handling capability, and complex dc biasing are issues. Similarly, RF-MEMS devices can tune antenna frequency response even though the packaging and reliability still remain a design challenge [11]–[16]. The RF switches and switchable matching networks may help in achieving a wide frequency tuning range; however, the soaring number of radios and frequency bands will require additional tuning circuitry in a limited volume [17]–[23]. In the context of transmitter, a reconfigurable antenna ideally requires one or more multiband transmitters along with on-chip/off-chip tuning networks and RF switches [24]. Some transmitters have been proposed [25]–[27], yet the die area and the bulky off-chip tuning networks are major issues. Also, the reliability factor comes into play while accommodating additional external components. Hence, alternative compact solutions are needed for wideband antenna tuning.

Recently, a novel antenna tuning technique was presented [28], where the frequency response of an antenna with multiple feed points is altered by varying the feed signal amplitudes and phases in different feed points. It may resemble beamforming techniques where the array elements

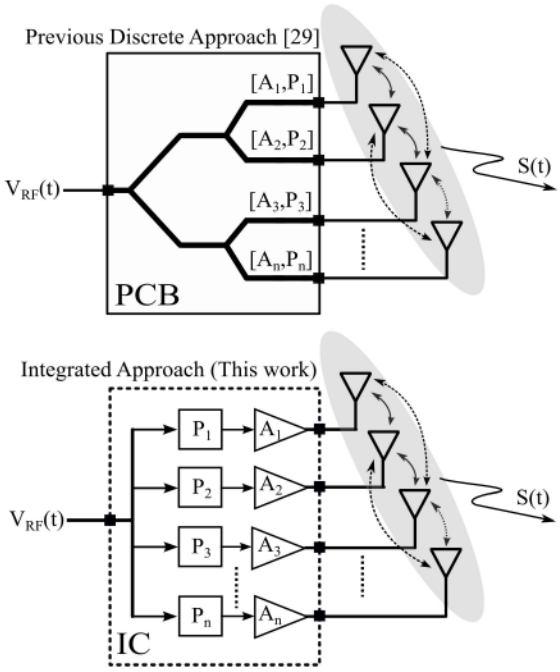

Fig. 1. Illustration of multiport antenna tuning concept reported in [28], demonstrated with transmission-line-based approach [29] versus integrated tuning approach proposed in this article. The annotation (A_i, P_i) represents the weighted amplitude and phase for the ith antenna feed of an N-port antenna. The input/output signals are described as $V_{RF}(t)$ and $S(t)$, respectively, while the arrows represent mutual coupling among antenna elements.

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are weighted in a similar fashion to steer the beam or adjust the polarization [30]. However, the novel antenna tuning method focuses on adjusting the frequency characteristics of the antenna cluster. The method offers wideband antenna tuning in the sub-6-GHz spectrum, especially from 1.5 to 5 GHz without matching circuits. The concept utilizes mutual coupling among antenna elements in such a way that the optimal antenna feeding signals result in a tuned antenna at the desired frequency. A proof of concept in the antenna regime has been demonstrated in [29] for two frequencies (2 and 4.3 GHz) as shown in Fig. 1. However, it was based on a static solution where the weighted excitations, i.e., amplitudes and phases, are devised with transmission lines (power dividers and phase shifters) having certain geometries. Feasibility of the concept with integrated transceivers was studied in [31] using a simplified theoretical model for a transmitter.

The objective of this article is to demonstrate the wideband multiport antenna tuning concept with a transmitter generating multiple RF signals with discrete amplitudes and phases. In addition, the matching or tuning circuits between transmitter and multiport antenna are omitted in order to observe the wideband tuning of antenna entirely with the weighted excitations. Most importantly, this article derives a design approach for the transmitter in order to tune the frequency characteristics of the multiport antenna cluster. To the best of the author's knowledge, this is the first report that describes the transmitter capable of 3.5-GHz wideband antenna tuning in the sub-6-GHz spectrum.

This article is organized as follows. Section II provides a brief review of the multiport antenna tuning concept and a description of the antenna prototype used in this work. Section III introduces the resolution analysis to determine the amplitude and phase tuning specifications for the transmitter. Section IV presents the transmitter architecture and circuit implementation details of the amplitude and phase tuning blocks. Section V then details the measurement results of the complete system containing transmitter and the antenna cluster, followed by conclusions in Section VI.

II. Antenna Concept and Design

A. Antenna Cluster Technique

The new concept of reconfigurable antenna system utilizes several coupled antenna elements that are fed with specific weighted signals to make them operate as a single antenna with a specific operation frequency and good efficiency. By optimizing the weights at a specific operation frequency, the operating frequency of the antenna can be changed. To enable the concept, a transmitter capable of generating the complex weighted excitation must be used.

The antenna tuning is achieved with optimal weighted excitations that result in reduced reflections at different feed points of the antenna cluster. In particular, the reflected voltage waves $\mathbf{b}$ from the multiport antenna feeds can be solved from the input voltage waves $\mathbf{a}$ with the help of antenna scattering matrix as $\mathbf{b} = \mathbf{Sa}$. The total active reflection coefficient (TARC) can be calculated for a specific excitation $\mathbf{a}$

$$\mathrm{TARC} = \sqrt{\frac{\mathbf{a}^{\mathrm{H}}(\mathbf{S}^{\mathrm{H}}\mathbf{S})\mathbf{a}}{\mathbf{a}^{\mathrm{H}}\mathbf{a}}}. \tag{1}$$

The TARC describes the total reflected and coupled power in all the ports. Alternatively, the same information can be given via the matching efficiency

$$\eta_{\mathrm{match}} = 1 - \mathrm{TARC}^2 = \frac{\mathbf{a}^{\mathrm{H}}(\mathbf{I} - \mathbf{S}^{\mathrm{H}}\mathbf{S})\mathbf{a}}{\mathbf{a}^{\mathrm{H}}\mathbf{a}} \tag{2}$$

where $\mathbf{I}$ is the identity matrix.

Equation (2) is a Rayleigh quotient, whose maximum value corresponds to the largest eigenvalue of $\mathbf{I} - \mathbf{S}^{\mathrm{H}}\mathbf{S}$, i.e.,

$$\eta_{\mathrm{match,max}} = \max[\mathrm{eig}(\mathbf{I} - \mathbf{S}^{\mathrm{H}}\mathbf{S})]. \tag{3}$$

The corresponding eigenvector gives the required complex weight coefficients. Deviation from these optimum weights will reduce the matching efficiency. Because the scattering matrix varies as a function of frequency, the optimum weighting coefficients are also different for different frequencies. The tuning is performed by modifying the weights to the ones suited for the desired frequency. An advantage of this method is that the scattering matrix of the antenna changes (due to the environment or the user), and then, the weights can be reoptimized for the new situation. In this way, the loss in antenna performance can be compensated for. While we limit our analysis to the free-space case in this work, this possibility has been studied in [32].

B. Antenna Prototype Design

The antenna consists of four elements, each exhibiting self-resonance at a different frequency between 1.5 and 5 GHz. It is designed on a 1.5-mm-thick circuit board with the width and length of 136 and 68 mm, respectively. The size is representative of a smartphone. At one corner of the board, there is a 15×15 mm^2 area where the antenna elements are placed.

The design is shown in Fig. 2 and described in detail in [29]. The design is mainly based on evaluating the TARC and then tuning the design accordingly. As the number of parameters in the scattering matrix of a four-port antenna is quite high, the exact relation between individual parameters and resulting antenna performance is difficult to determine. The role of the mutual coupling has been studied for a two-port in [33]. The results for the two-port suggest that both the coupling and the reflection should be of similar magnitude for optimal tuning results. The phase of the coupling is also relevant.

As is typical for antennas in a mobile chassis, the pattern is mostly omnidirectional with some variations as a function of frequency. Because the elements are spaced very close to each other, the combined radiation pattern is similar to the individual antenna element patterns. The close proximity of the antennas does not enable any meaningful control over the radiation patterns, and thus, only the impedance properties of the antennas are considered.

Fig. 3(a) shows the reflection coefficients for each element separately, to give a brief estimate on the resonant frequencies of each antenna element. Fig. 3(a) also shows the TARC

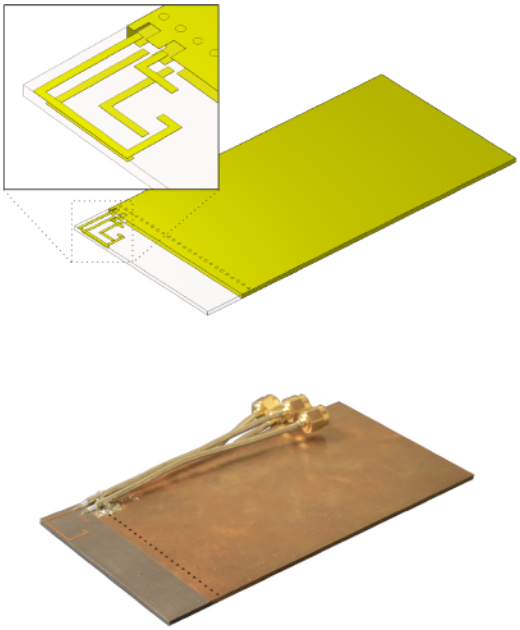

Fig. 2. Antenna used in this work consists of four antenna elements [29].

calculated from (1) under optimal feeding. The TARC shows that the antenna cluster elements perform collaboratively better than they could individually. Note that the TARC curve is the envelope of the best possible TARC value at each frequency point, not the instantaneous TARC with a fixed excitation performance across the entire band. In addition, the TARC is also evaluated with the Eldo circuit simulator, showing exact agreement.

Calculating the optimal TARC also gives the corresponding weight coefficients. The antenna has four elements, so we denote the complex weight coefficients as follows:

$$\mathbf{a} = \begin{bmatrix} a_1\angle\varphi_1 \\ a_2\angle\varphi_2 \\ a_3\angle\varphi_3 \\ a_4\angle\varphi_4 \end{bmatrix}. \tag{4}$$

Fig. 3(b) shows the optimal amplitudes of the weights. Comparing with Fig. 3(a), the largest amplitudes in the elements correspond to the resonant frequencies. It is somewhat intuitive that the antenna element that is matched the best by itself will be responsible for the majority of the excitation, with the others being used in smaller capacity to further improve matching and reduce coupling. Similarly, the phases of the weights are shown in Fig. 3(c). In this case, the phases are shown in relation to element four, which is shown as a phase of 0°. These phases φ_i can be equivalently described by the delays $\tau_i = -\varphi_i/(360f) + 1/f$, where $i = 1, \ldots, 4$ and f represents the frequency of the weighted signal.

The transmitter system should be able to match these amplitude and phase or delay profiles as closely as possible for optimal tuning of the antenna. From the amplitude and phase profiles, we can observe that a set of fixed values will produce relatively large frequency bands because the profiles are relatively smooth. This suggests that the method is not overly sensitive, and the resolution of the weight settings should be feasible. In Section III, this is studied in more detail.

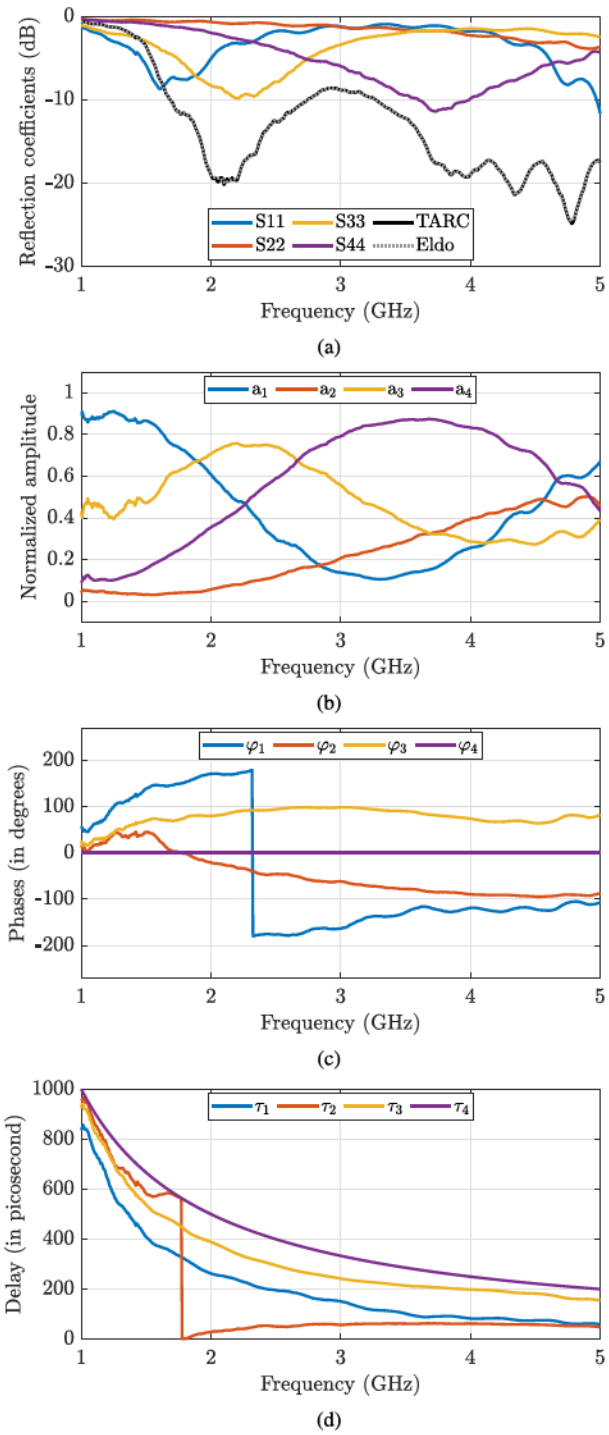

Fig. 3. (a) Input reflection coefficients (S_{ii}) of the four-port antenna with the TARC benchmark in MATLAB and Eldo simulations. (b) Amplitude profile of antenna cluster. (c) Phase profile of antenna cluster. (d) Delay profile of antenna cluster.

III. Resolution Analysis

The accuracy of the weighted signals, i.e., optimal amplitude and phase profiles, dictates antenna tuning performance and the transmitter complexity. The variations in weighted

signal characteristics are analyzed with a resolution analysis performed in conjunction with Eldo simulations. As a result, the TARC performance is examined for several different scenarios. These results ultimately assist in defining the system-level specifications for the transmitter.

A. Amplitude Resolution

The effect of amplitude variations is studied by introducing a controlled amount of error in feeding signal amplitudes, while the phases are kept intact. For instance, the weighted signal for the 2-GHz case based on the amplitude and phase profiles is given by

$$\begin{bmatrix} a_1\angle\varphi_1 \\ a_2\angle\varphi_2 \\ a_3\angle\varphi_3 \\ a_4\angle\varphi_4 \end{bmatrix}_{f=2\text{GHz}} = \overbrace{\begin{bmatrix} 0.61\angle 171^\circ \\ 0.05\angle -21^\circ \\ 0.71\angle 80^\circ \\ 0.36\angle 0^\circ \end{bmatrix}}^{\text{Exact}} \approx \overbrace{\begin{bmatrix} 0.6\angle 170^\circ \\ 0\angle 340^\circ \\ 0.7\angle 80^\circ \\ 0.4\angle 0^\circ \end{bmatrix}}^{\text{Quantized}}. \quad (5)$$

To analyze the amplitude variations for 2-GHz scenario, the weighted signal amplitude is perturbed and fed to the antenna cluster. The exact signal is intentionally quantized to highlight the limited accuracy, which consists of amplitudes ranging from 0 1 V with steps of 0.1 V, while the phases are rounded to multiple of 5°. An exact weighted signal in (5) tunes the antenna precisely at 2 GHz, as shown in Fig. 4(a). Likewise, a quantized weighted signal is also presented to clarify the amplitude perturbation and its effect on the TARC performance. For comparison, an excitation case is also illustrated where all the feeds are turned on with the same amplitudes and phases, i.e., $a_i = 1$ and $\varphi_i = 0^\circ$ leading to poor antenna tuning profile. The resolution study is performed by assuming that only the Feed i amplitude is being modified, while other amplitudes and the phases are intact, i.e., vary the amplitude a_i such that the other amplitudes $a_{i\neq j}$ and the phases of all amplitudes φ_i are intact where $i, j = 1, \ldots, 4$. As the error size Δ is increased for Feed 1 amplitude a_1, the TARC profile shifts from 2 to 2.4 GHz, indicating that the tuning performance is exacerbated, as shown in Fig. 4(a). Nevertheless, the TARC performance seems reasonable for the case $a_1 \pm 3\Delta$ with TARC ≈ -10 dB around 2 GHz. This implies that the antenna tuning is still possible even if we decrease the Feed 1 amplitude to one half of its required weight.

The extent of TARC degradation due to amplitude variations can be analyzed across the spectrum. For instance, we have analyzed a case where the amplitudes $\{a_1 \ldots a_4\}$ accommodate a certain amount of error at the same time. Fig. 4(b) shows such cases where the amplitudes $\{a_1 \ldots a_4\}$ are subjected to error sizes of 10% and 50%, while the phases are kept intact. It is clear that the antenna tuning is degraded based on the amount of error being introduced. Nevertheless, the relative and frequency-dependent nature of amplitudes mainly dictates the antenna tuning. By disturbing a feed amplitude a_i that may have a minor effect on antenna tuning performance in a certain frequency band, however, its effect may be severe where its major contribution is required. To understand this,

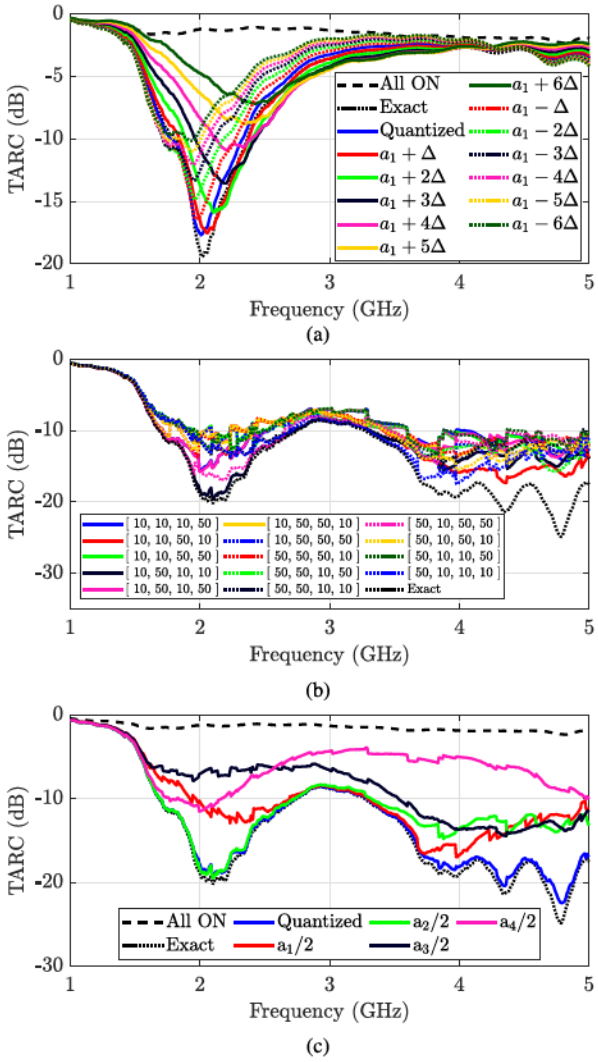

Fig. 4. (a) Effect of amplitude variations for 2-GHz case: Feed 1 amplitude a_1 is analyzed for various error steps where $\Delta = \pm 0.1$ V. (b) Effect of simultaneous error in all amplitudes a_1–a_4 with two different error sizes: 10% and 50%. (c) Effect of amplitude variations on antenna TARC profile for $a_i/2$ such that $a_{i\neq j}$ and φ_i are intact, where $i, j = 1, \ldots, 4$.

the amplitude variation for each feed is also analyzed separately in order to visualize its contribution in antenna tuning. Fig. 4(c) shows this special scenario where the weighted signal amplitude a_i is being reduced to one half of the actual amplitude, i.e., $a_i \rightarrow a_i/2$.

The effect of amplitude reduction for Feed1 and Feed2 amplitudes, i.e., $\{a_1 \rightarrow a_1/2, a_2 \rightarrow a_2/2\}$, affects the least, whereas the other feeds amplitude $\{a_3 \rightarrow a_3/2, a_4 \rightarrow a_4/2\}$ result into deteriorated TARC performance across the spectrum. As a consequence, the amplitudes $\{a_1$ and $a_2\}$ are less sensitive to amplitude variations even if their amplitudes are relaxed by 6 dB. On the contrary, the variations in amplitudes $\{a_3$ and $a_4\}$ must be minimum in order to have sufficient tuning. Table I gives insight about the weighted amplitudes for the tuning of antenna from 1.5 to 5 GHz. It is clear that the amplitude resolution is coarse for all feed amplitudes. Furthermore, the integrated system must generate amplitudes a_i from 0 dB to the lowest possible amplitude. These lowest amplitudes indeed define the amplitude specification for the

TABLE I
RELATIVE WEIGHTED AMPLITUDES (dB)

Freq. (GHz)	a_1	a_2	a_3	a_4
1.5	0	-28*	-5.3	-14.8
2	-1.3	-22*	0	-6
2.5	-7.8	-16	0	-2
3	-15.2	-11.7	-3.1	0
3.5	-16.5	-9.7	-7.3	0
4	-10.3	-6.5	-9.3	0
4.5	-3.9	-3.2	-8.2	0
5	0	-3.3	-4.7	-3.7
Range= $\lvert \min(a_i) \rvert$	16.5	16	9.3	14.8

* a_2 amplitude can withstand more than 6 dB variation. For very smaller amplitudes, this feed can be considered in an off state.

integrated circuit (IC). Therefore, the antenna used in this design demands the on-chip amplitude tuning to have at least amplitude range coverage of $\{16.5, 16, 9.3, 14.8\}$ dB for all four feeds amplitude $\{a_1 \ldots a_4\}$, respectively.

B. Phase Resolution

Similar to amplitudes a_i, the accuracy of phases φ_i affects the antenna tuning performance. The extent of TARC degradation can be analyzed by disturbing the phases of the reference phase profile in Fig. 3(c). First, the effect of phase variations is studied for the 2-GHz case with the weighted signal in (5) where the phase φ_1 is under consideration. In addition, the amplitudes $\{a_1, \ldots, a_4\}$ and the phases $\{\varphi_2, \ldots, \varphi_4\}$ are intact. The exact and quantized signals result into nearly equal TARC performance, while the tuning performance for phase errors of $\pm 10°$, $\pm 20°$, and $\pm 30°$ gradually deteriorates, as shown in Fig. 5(a). It is a notable observation that the antenna tuning profiles shift upward representing degradation in TARC. On the contrary, the amplitude variations degrade TARC along with shifting of tuning profile to a different frequency band. Nevertheless, the error step of $\pm 30°$ still provides a reasonable tuning.

Also, the phase deviations are evaluated for the whole frequency range. In the analysis, a phase φ_i is varied by accommodating an error of $\pm 30°$ with respect to the reference value, while other phases $\varphi_{i \neq j}$ and all the feed amplitudes a_i remain intact. When the antenna feeds are excited with such weighted signals, the phase variations alter the TARC performance, as shown in Fig. 5(b). The TARC reduces to -7 dB between 2.5 and 3.5 GHz, while it also shows that the antenna feeds can withstand $\pm 30°$ error with TARC ≤ -10 dB across the remaining spectrum. To sum up, the antenna TARC is relatively less vulnerable to phase variations compared to the amplitude variations.

To determine the effect of delay resolution on antenna TARC, the phase characteristics in Fig. 3(c) are achieved with delays of fixed sizes from 5 to 40 ps. Fig. 5(c) shows the effect of various delay sizes on antenna TARC where the delay steps of 5–15 ps show sufficient TARC performance, i.e., TARC ≤ -10 dB, while it deteriorates with larger delay sizes. Thus, a delay step of 5–15 ps will be enough for the on-chip phase tuning of each antenna feed.

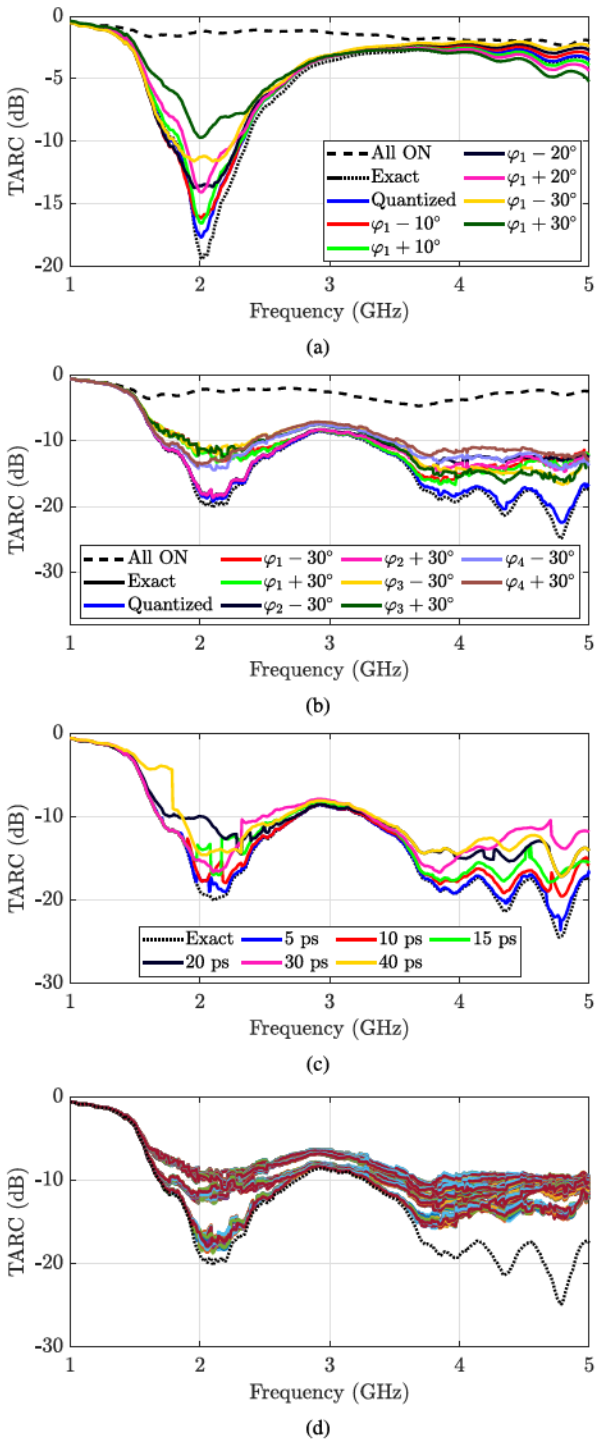

Fig. 5. (a) Effect of phase variations on antenna tuning profile for 2-GHz scenario. (b) Effect of phase variations across the spectrum. (c) Effect of various delay steps on the antenna tuning performance. (d) Effect of simultaneous amplitude variations (10%–20%) and phase anomalies ($\pm 20°$) on antenna TARC performance.

The real-time scenario encompasses the simultaneous variation both in $\{a_1, \ldots, a_4\}$ and $\{\phi_1, \ldots, \phi_4\}$. These deviations not only affect the TARC, but they also assist in determining the extent of degradation. In fact, the required antenna tuning can be described in terms of required amplitude and phase resolutions. For instance, a situation is considered where the amplitudes and phases have anomalies of 10%–20% (1–2) dB

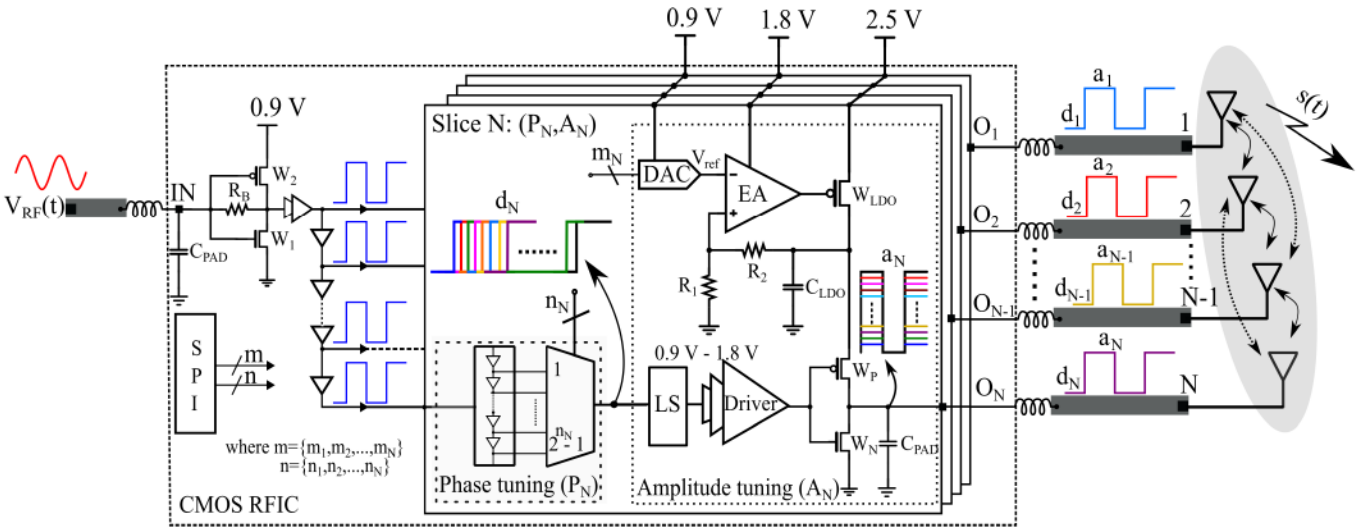

Fig. 6. Detailed system-level diagram of a generic CMOS RFIC consisting of N-tuning slices for the tuning of an N-element antenna cluster. An RF signal $V_{RF}(t)$ is transformed to 0.9-V pulse signal which is being fed to each tuning slice. The ith tuning slice weights the phase and amplitude of the ith antenna feed in accordance with the optimal phases and amplitudes. In particular, each tuning slice contains a corresponding phase tuning block (P_i) and an amplitude tuning block (A_i) with resolutions m_i and n_i, respectively, where i=1…N. In this prototype ($N = 4$), the transmitter outputs $O_1 \ldots O_N$ are wirebonded to a PCB. The PCB utilizes 50-Ω transmission lines to connect transmitter outputs $O_1, \ldots, O_N$ to feed the four-port antenna cluster comprising of four monopoles reported in [29]. By properly exciting the antenna feeds, the antenna can be tuned at the desired frequency along with the transmission of an information signal $s(t)$.

and ±20°, respectively. Fig. 5(d) shows such cases where all feeds amplitudes and phases have such diversions from the exact weighted signals. The TARC drops to −7 dB in worst case scenario between 2.5 and 3.5 GHz. Nevertheless, the TARC performance in other frequency bands is still below −9 dB. Thus, the on-chip amplitude and phase tuning implementations must be capable of providing less than 20% amplitude variations and phase deviations of ±20° for sufficient antenna tuning of −10 dB across several frequency bands.

IV. System Architecture

Fig. 6 shows the block diagram of the proposed integrated transmitter system for tuning of the antenna cluster. It consists of an input stage and N identical tuning slices corresponding to an N-port antenna. An input-stage buffer that is a resistive feedback amplifier takes an RF tone $V_{RF}(t)$ ranging from 1.5 to 5 GHz as an input and amplify it to a 0.9-V tone signal. The buffer stage converts the tone signal into a pulse signal and distributes that signal to each tuning slice. In this implemented transmitter prototype, the number of tuning slices is four corresponding to the four antenna elements or ports. Each tuning slice comprises a phase tuning block followed by an amplitude tuning block. For the ith tuning slice, the amplitude and phase tuning block specifications are described in terms of amplitude and phase resolutions (m_i, n_i). To tune the antenna cluster at an operating frequency f, the serial peripheral interface (SPI) block uploads the static settings (m, n) based on the amplitude and phase profiles in order to scale the phase and amplitude of each antenna feed. The following describes the system-level specifications for (m, n) and the implemented circuit topologies to achieve the desired amplitude and phase tuning.

A. Phase Tuning Block

In system-on-a-chip (SoC), the phase tuning is achieved with delay tuning circuits. The delay circuits are classified based on how the delay is generated by the circuit. First, the digital delay lines are where the digital input directly maps to the required delay value. In contrast, the analog delay lines are controlled with analog signals. Accurate high-speed CMOS delay elements have been recently emerged and can be adapted to the needs of active matching [34], [35]. Opting for digital control, a digitally controlled delay line (DCDL) is selected. The delay line has two characteristics: the delay step that is the smallest possible time step and the delay range (DR) corresponding to the maximum time a signal can be delayed. In this prototype, the delay characteristics for each antenna feed is implemented with a phase tuning block that pours down to a tapped delay line and a multiplexer, similar to one used in [36].

By choosing the 10-ps delay step, the total number of delay elements DE_i required for the delay tuning of the ith antenna feed is shown in Fig. 7(a). The number of delay elements determines the delay tuning specification of the ith phase tuning block, i.e., $n_i = \max[\log_2(\mathrm{DE}_i)]$. Therefore, the desired delay tuning specifications are $n = \mathrm{ceil}\{n_i\} = \mathrm{ceil}\,(\log_2\{58, 47, 35, 58\}) = \{6, 6, 6, 6\}$. The digital control input n_i allows 6-bit resolution with the selection of 2^6 delayed versions of the 0.9-V pulse signal. The significance of ceil(·) function reflects the additional delay offset compensation, which is utilized in routing input signal to each phase tuning block. The delay tuning block performance is usually represented in terms of delay characteristics. The measured delay characteristics of all four phase tuning blocks are shown in Fig. 7(b). The delay characteristics (d_3 and d_4) of the phase tuning blocks (P_3 and P_4) has delay offset. This delay

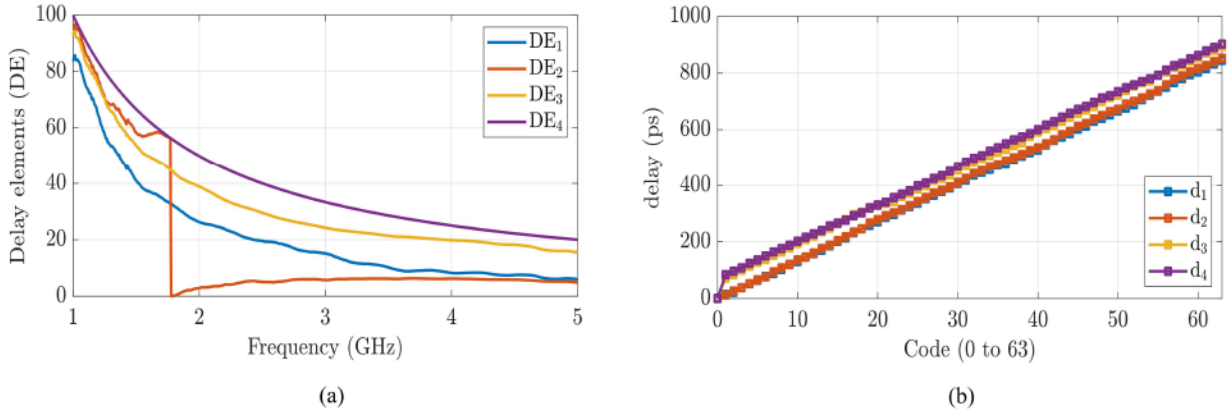

Fig. 7. (a) Number of delay elements for 10-ps delay step across 1–5-GHz spectrum. (b) Measured delay tuning performance of all four phase tuning blocks P_1–P_4.

offset should be compensated while generating the optimal phases. In addition, the phase tuning block should provide at least one cycle or 360° phase coverage from 1.5 to 5 GHz. In this prototype, each tuning block $P_1, \ldots, P_4$ provides the DR of 830 ps, which is an ample amount of delay tuning for signals ranging between 1.5 (1 cycle≈666 ps) and 5 GHz (1 cycle≈200 ps). Furthermore, the 10-ps delay step at both extremes is equivalent to the phase step of 5.4° and 18°, respectively, which is actually less than 30° phase variation.

B. Amplitude Tuning Block

The transmitter IC also contains an amplitude tuning block in each tuning slice. The amplitude tuning block follows the phase tuning block in order to scale the amplitude of the antenna feeds. This block has two main objectives: the amplitude scaling of the phase tuned signal and driving of the antenna as a load. Table I describes the desired relative amplitude scaling for each antenna feed. The amplitude scaling step is coarse for these weights among different frequencies of the spectrum. It is also clear that the feed amplitudes $\{a_1, \ldots, a_4\}$ occupy different scaling ranges between 9.3 dB $\leq a_i \leq$ 16.5 dB. To ensure that each feed covers the maximum range of 16.5 dB, all amplitude tuning blocks are identical. This, in fact, provides us freedom to connect the antenna feeds arbitrarily to any transmitter output O_1–O_4.

With the multiport antenna tuning technique, the amplitude tuning demands static amplitude scaling in all four amplitude tuning blocks A_1–A_4. In this design, we have utilized a simple supply voltage scaling method enabling supply tuning of a switch-mode power amplifier (PA), i.e., class-d, as shown in Fig. 6. The output of a switch-mode PA mainly depends on the supply voltage. By scaling the supply voltage, one can tune the amplitude or power of the respective antenna feed. Nevertheless, this amplitude scaling could also be embedded on an actual transmitter, such as polar [37]–[39] and multilevel outphasing architectures, which tolerate PA nonlinearity and inherently support high-power switching PA's [40] and wide-band phase modulation [26] and provide means for amplitude control [36], [41], [42].

To scale the ith feed amplitude a_i, the implemented amplitude tuning block A_i contains a digital-to-analog converter (DAC), low-dropout (LDO) regulator, class-d driving stage, and the level shifter (LS) along with driver circuitry at the input of the block. The input of the amplitude tuning block is a 0.9-V phase-tuned pulse signal that needs to be scaled according to the optimal amplitude a_i. The LS transforms 0.9-V phase-tuned signal to 1.8-V signal to drive 1.8-V class-D output stage. The output of the block O_i is simply scaled by varying the supply of these devices, i.e., the LDO output V_{LDO}. The LDO takes the reference voltage V_{ref} from the resistive voltage DAC as an input. The resolution of the DAC m_i in fact determines the amplitude resolution of the block A_i. Table I shows that the amplitude scaling step is coarse for the weights among different frequencies of the spectrum. In this prototype, $m_i = 4$ is selected, and the DAC generates 2^4 linearly scaled reference voltages residing in the range: 500 mV $\leq V_{\text{ref}} \leq$ 800 mV. The voltage V_{ref} is being fed to the error amplifier of the LDO, which is basically a differential amplifier with current mirror load. The voltage V_{ref}, the resistors R_1 and R_2, and the error amplifier open-loop gain determine the LDO output voltage: $V_{\text{LDO}} \approx (1 + R_1/R_2)V_{\text{ref}}$, where $R_1 = R_2 = 10\ k\Omega$ and 0.8 V $\leq V_{\text{LDO}} \leq$ 1.72 V across the capacitor $C_{\text{LDO}} = 30$ pF. Hence, the amplitude block linearly scales V_{LDO} in order to produce linearly scaled amplitude signals at the output, as shown in Fig. 8(c).

The supply scaling demonstrates the amplitude scaling for all four amplitude tuning blocks A_1–A_4. One notable observation is to consider the effects V_{LDO} on the class-D pMOS device turn-on resistance Z_{on}. This resistance can be described by the following relation: $Z_{\text{on}} = (1/KW/L(V_{\text{SG}} - |V_{\text{th}}|))$. From a design perspective, the smaller values of Z_{on} demands significant device width W, which increases the driver size and the power consumption. Therefore, the device width was optimized for sufficient amplitude tuning with minimal device size. The resistance Z_{on} is plotted in Fig. 8(d) for 16 different scaled versions of V_{LDO}. Besides, the main focus is to consider the relative amplitude scaling among different amplitude tuning block outputs. In order to demonstrate the concept with modern CMOS process and reasonable chip size, we chose to use a moderate output power of approximately 7 dBm from each IC output. The fundamental output power of a single amplitude tuning block is described in Fig. 8(a) in comparison with the simulated output powers at 1.5 and 5 GHz. Each IC

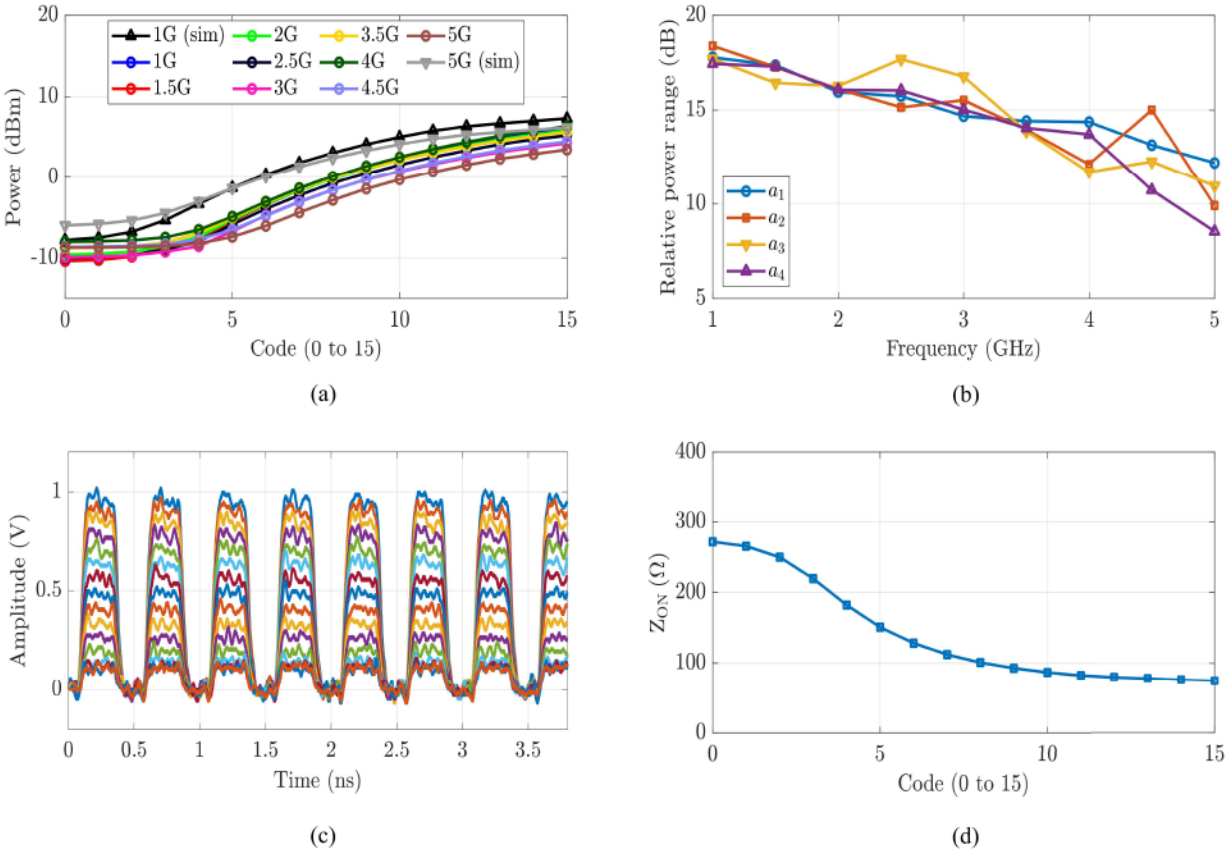

Fig. 8. (a) Measured power scaling of a single transmitter output from 1.5 to 5 GHz. (b) Measured output power ranges of all four IC outputs O_1–O_4. (c) Measured amplitude scaling performance at 2 GHz for one single amplitude tuning block. (d) Simulated turn-on resistance of class-d device for scaling of V_{LDO}.

output O_1–O_4 features the maximum measured output power of 6 dBm at lower frequencies, while the power level gradually decreases to 3.4 dBm at higher frequencies. In addition, the amplitude tuning range also shrinks at higher frequencies due to the reduction in output power resulting from increased parasitics and switching losses. The corresponding tuning range of all four amplitude tuning blocks A_1–A_4 across the spectrum is shown in Fig. 8(b). It clearly demonstrates that the implemented prototype has enough scaling range for all transmitter outputs covering at least 8 dB $\leq a_i \leq$ 18 dB across the spectrum.

To generate a weighted signal, the implemented amplitude tuning blocks A_i and phase tuning blocks P_i have certain resolutions, i.e., ($m_i = 4$ and $n_i = 6$, where $i = 1 \ldots 4$) to cover the desired amplitudes and delays. These settings are in fact controlled through the SPI block. To clarify it further, Table II presents the control settings (m_i and n_i) based on amplitude and phase profiles. The amplitude settings m_i are relative, so the maximum amplitude is represented with a value 15. Similarly, the phase settings n_i enable required phase coverage for all four antenna feeds. From the lookup table, it can be seen that the weight settings also vary across the spectrum depending on the weighted signal amplitude and phase requirements. These settings are loaded into the logic settings via SPI providing the antenna cluster tuning for the desired operation frequency.

TABLE II
WEIGHTED SIGNAL SETTINGS (m, n)

Freq. (GHz)	m_1	m_2	m_3	m_4	n_1	n_2	n_3	n_4
1.5	15	0	8	3	30	43	22	25
2	12	0	15	8	19	2	10	13
2.5	6	2	15	12	14	4	2	4
3	2	4	10	15	34	29	24	25
3.5	0	5	6	15	27	25	17	18
4	5	7	6	15	23	23	13	13
4.5	9	10	6	15	21	20	10	9
5	15	9	8	9	18	18	6	5

For these resolutions $(m_i, n_i) = (4, 6)$, the corresponding ranges are $0 \leq m_i \leq 15$ and $0 \leq n_i \leq 63$ where $i = 1 \ldots 4$.

V. MEASUREMENT RESULTS

The implemented transmitter for the multiport antenna tuning is implemented in a 28-nm CMOS process. The transmitter chip is wirebonded to the printed circuit board (PCB), which includes RF transmission lines connecting transmitter outputs to the antenna feeds. For prototyping and verification purposes, both the antenna and the IC are implemented on separate PCBs enabling detailed IC outputs phase and amplitude characterization. The chip and PCB interface is modeled in ADS accounting for the IC pad capacitances, wirebond inductances, and the RF transmission lines. An electromagnetic (EM) model was extracted and simulated in order to determine the characteristics of the interface. Fig. 9(a)–(c) shows the

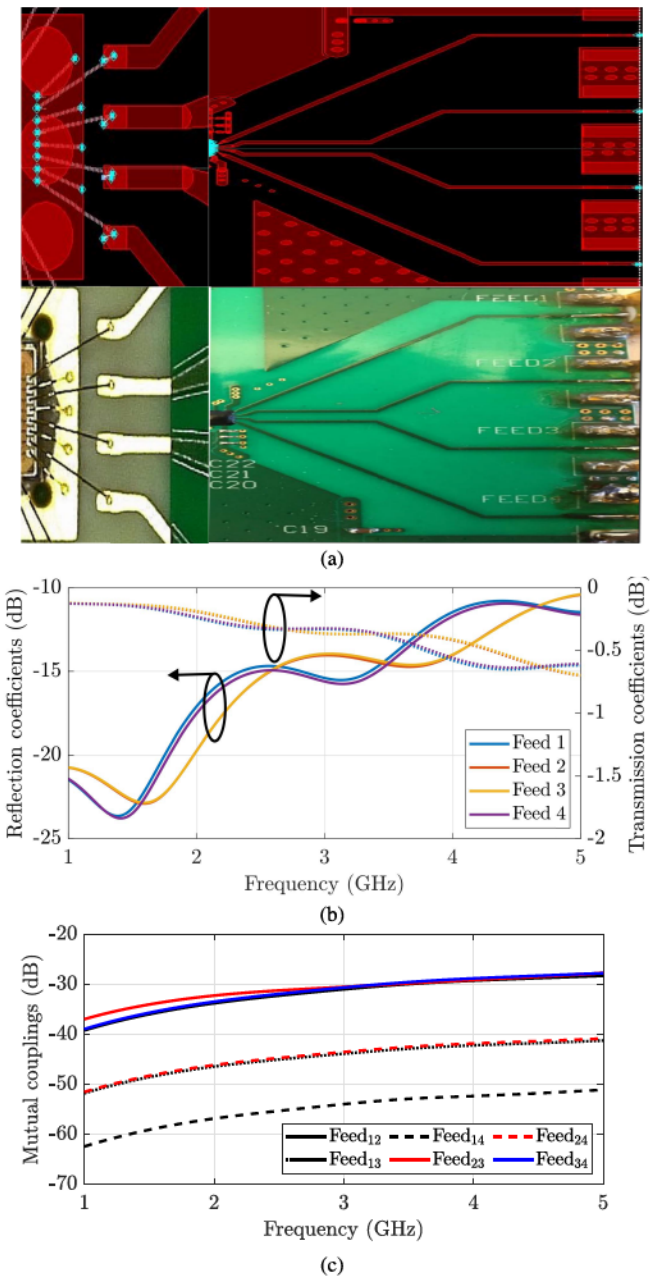

Fig. 9. (a) ADS layout and implementation of IC/PCB interface. (b) Simulated reflection/transmission coefficients of the ADS-based EM model. (c) Simulated mutual couplings of the four feeding paths based on the EM model.

designed ADS layout and the prototyped IC/PCB cross section along with the simulation results based on the EM model. From the design perspective, the transmission lines are designed in such a way that the mismatch among the weighted antenna feeding signals is minimum. However, the transmission line routing leads to delay offset among the feeding signals. This offset has already been considered while generating the SPI settings (m, n) for the optimal feeding signals. The transmission lines Feed1 . . . Feed4 are designed in such a way that the feeds (Feed1, Feed4) and (Feed2, Feed3) have similar geometry and characteristics, as shown in Fig. 9(b). The return loss better than 10 dB provides nearly 50-Ω interface between the IC outputs A_1–A_4 and the antenna cluster feeds. Furthermore, Fig. 9(c) shows the effect of mutual coupling among different feeds. The coupling between ith and jth feed is represented by Feed_{ij}. The results indicate that the adjacent feeds have nearly −28-dB coupling, while this effect drops from −40 to −50 dB for other neighboring feeds.

The measurement setup mainly consists of integrated vector network analyzer (VNA) and an antenna scanning probe array built inside the equipment. Traditionally, a broadband horn antenna calibration is usually performed in order to have a reference for the measurements. Then, one port of the VNA is connected to the antenna under test, whereas the second port of the VNA is connected to the antenna probe array, which in fact scans the far-field radiations of the antenna under test; thus, the relation between VNA port1 and port2 can provide several antenna performance metrics, such as gain, directivity, beamwidth, radiation patterns, and antenna efficiency. In contrast to traditional antenna measurements, the four IC outputs are initially characterized with a broadband horn antenna. One port of the VNA is connected to IC input, whereas one IC output drives the broadband horn antenna with a maximum amplitude for reference calibration measurement. Since the RFIC contains four same amplitude and phase tuning blocks, therefore, the horn antenna calibration data are also similar to each IC output. Afterward, the IC outputs are connected to the antenna cluster under consideration, and the complete system (IC+ANT) is mounted inside the MVG StarLab 6-GHz equipment, as shown in Fig. 10.

One port of the VNA is connected to the IC input, and it sweeps the IC input with an RF tone ranging from 1.5 to 5 GHz with a 50-MHz frequency step. To tune the antenna cluster at the desired operation frequency, the IC loads the respective SPI settings (m, n) described in Table II. The IC transforms the input tone to four amplitude-/phase-scaled RF signal outputs driving the four-port antenna. The antenna cluster accordingly transmits/radiates, and these radiations are then scanned by the equipment antenna probe array attached to another port of the VNA. In this way, we have the measurement data from both VNA ports enabling the characterization of the mounted system. The equipment software processes the data and provides the antenna cluster efficiency. By substituting the efficiency data in (2), i.e., $\text{TARC} = (1 - \eta_{\text{match}})^{1/2}$, one can determine the antenna cluster tuning performance in terms of the TARC.

One disadvantage of the measurement setup is that it is not possible to separate the antenna matching efficiency η_{match} from the antenna radiation efficiency η_{rad}. Instead of the matching efficiency, we obtain the antenna total efficiency $\eta_{\text{tot}} = \eta_{\text{match}}\eta_{\text{rad}}$. However, the antenna is manufactured on a low-loss substrate, so the radiation efficiency is quite high, i.e., $\eta_{\text{tot}} \approx \eta_{\text{match}}$. This in turn allows us to utilize the total efficiency instead of the matching efficiency to calculate the TARC. While this approximation does not comply with the exact representation of TARC in (1), it is useful for describing the overall antenna performance.

Fig. 11(a) and (b) shows the tuning performance of antenna cluster at 2 and 4.5 GHz, respectively, in comparison to the simulated result with an exact weighted signal excitation. The TARC performance of less than −10 dB in both cases is

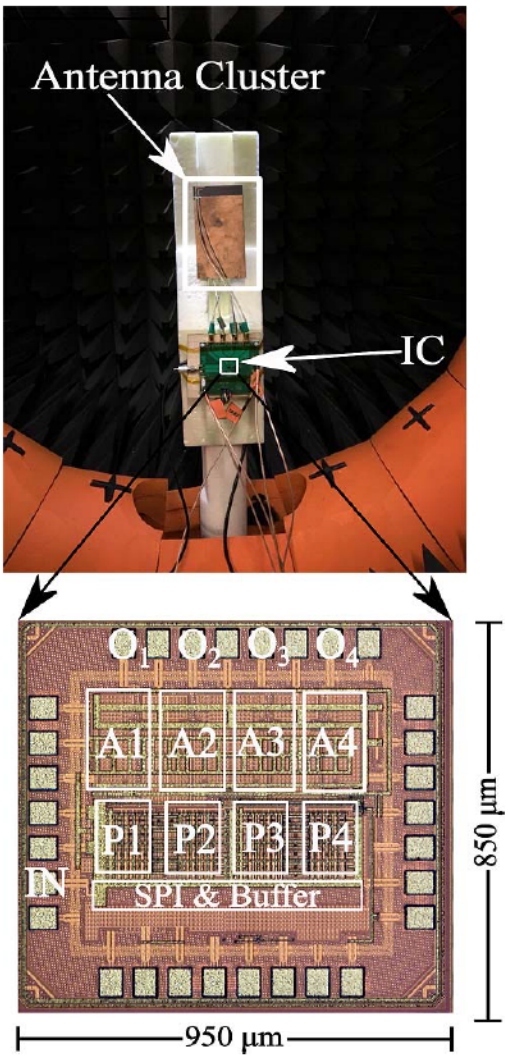

Fig. 10. Measurement setup for the implemented prototype consisting of IC wirebonded to PCB driving the antenna cluster.

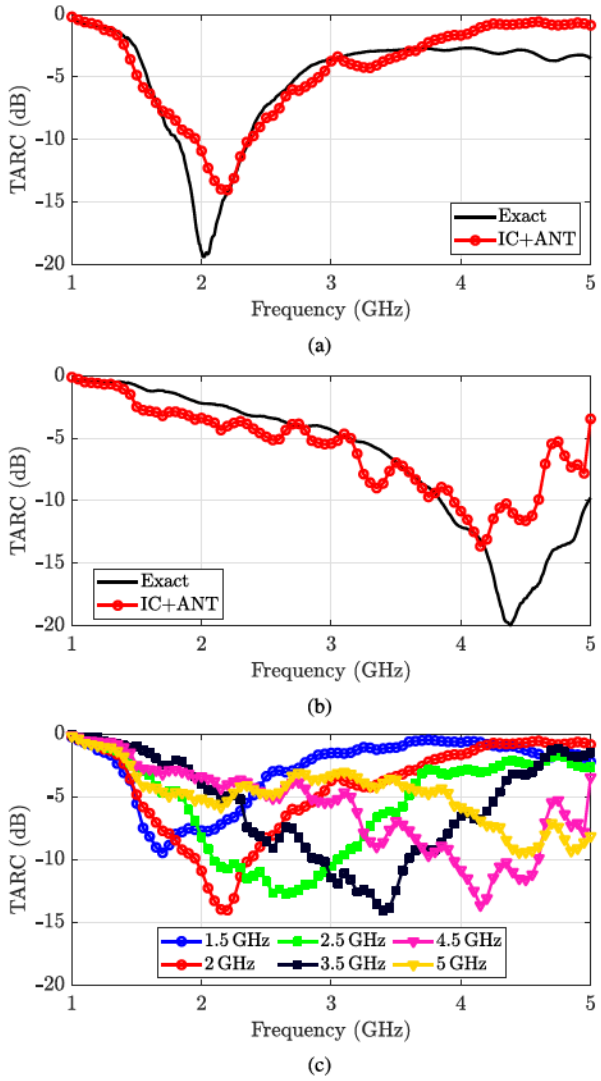

Fig. 11. Measured tuning performance of antenna cluster at (a) 2 and (b) 4.5 GHz. (c) Measured wideband antenna tuning performance across the spectrum.

considered sufficient for antenna tuning. However, the 4.5-GHz case depicts that the antenna tuning performance is degrading at higher frequencies. The deviation in the measurement results highlights the impedance mismatch effect between the IC output and the antenna interface. Neither the IC output nor the antenna is perfectly matched to 50 Ω. Despite nonideal properties on both sides of the interface, the system is capable of desired tuning performance across the entire designated spectrum, as shown in Fig. 11(c). This describes the wideband antenna tuning performance of the antenna cluster for several difference cases. In order to scale the amplitude and phase of one antenna feed across the spectrum, each amplitude/phase tuning block consumes roughly 8–40/5–20 mW or in total 13–60 mW. Most importantly, the antenna cluster tuning of less than −10 dB is demonstrated for several frequency bands. Thus, these measured results indicate that the proposed prototype validates the multiport antenna tuning concept across the desired frequency spectrum.

The main target of this work is to verify the multiport antenna tuning with an IC. Moreover, the IC statically controls the amplitude and phase of each antenna feed and supports only phase-modulated signals. Nevertheless, this feature can be investigated in further research for multilevel modulations. In the future, the transmitter and the antenna cluster should be integrated together on the same substrate to reduce the effect of connectors and transmission lines. In particular to transmitter, the critical parameters, such as output power and efficiency, must be considered along with the effect of impedance mismatch. Furthermore, the number of antenna elements and the transmitter outputs can be optimized by adopting the antenna IC codesign approach.

VI. Conclusion

This article demonstrates an integrated RF transmitter front end addressing the need for wideband antenna tuning from 1.5 to 5 GHz. The transmitter IC adjusts the antenna cluster frequency characteristics by generating frequency-dependent optimal amplitude- and phase-tuned signals. Resolution analysis showed that the accuracy of amplitude and phase tuning performed with the IC is adequate to retain the antenna cluster tuning capability. The TARC parameter of less than −10 dB

is measured across several frequency bands. This proof-of-concept implementation fully utilizes the capabilities of 28-nm CMOS process with four on-chip amplitude and phase tuning blocks to tune the four-port antenna cluster. The chip size is around 0.85 mm x 0.95 mm, including custom electro static discharge (ESD)-protected RF pads. Measurement results confirm the operation of the proposed system and feasibility of novel wideband tuning concept.

REFERENCES

[1] G. Jin, C. Deng, J. Yang, Y. Xu, and S. Liao, "A new differentially-fed frequency reconfigurable antenna for WLAN and sub-6GHz 5G applications," *IEEE Access*, vol. 7, pp. 56539–56546, 2019.

[2] Y. Braham Chaouche, I. Messaoudene, I. Benmabrouk, M. Nedil, and F. Bouttout, "Compact coplanar waveguide-fed reconfigurable fractal antenna for switchable multiband systems," *IET Microw., Antennas Propag.*, vol. 13, no. 1, pp. 1–8, Jan. 2019.

[3] A. N. Kulkarni and S. K. Sharma, "Frequency reconfigurable microstrip loop antenna covering LTE bands with MIMO implementation and wideband microstrip slot antenna all for portable wireless DTV media player," *IEEE Trans. Antennas Propag.*, vol. 61, no. 2, pp. 964–968, Feb. 2013.

[4] Y. Li, Z. Zhang, J. Zheng, Z. Feng, and M. F. Iskander, "A compact hepta-band loop-inverted f reconfigurable antenna for mobile phone," *IEEE Trans. Antennas Propag.*, vol. 60, no. 1, pp. 389–392, Jan. 2012.

[5] H. F. Abutarboush *et al.*, "A reconfigurable wideband and multiband antenna using dual-patch elements for compact wireless devices," *IEEE Trans. Antennas Propag.*, vol. 60, no. 1, pp. 36–43, Jan. 2012.

[6] A.-F. Sheta and S. F. Mahmoud, "A widely tunable compact patch antenna," *IEEE Antennas Wireless Propag. Lett.*, vol. 7, pp. 40–42, 2008.

[7] S. Riaz, X. Zhao, and S. Geng, "A compact frequency agile patch antenna with agile microstrip feedline," in *Proc. 2nd Int. Conf. Comput., Math. Eng. Technol. (iCoMET)*, Jan. 2019, pp. 1–4.

[8] E. de Foucauld, R. Severino, D. Nicolas, A. Giry, and C. Delaveaud, "A 433-MHz SOI CMOS automatic impedance matching circuit," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 6, pp. 958–962, Jun. 2019.

[9] T. Li, H. Zhai, L. Li, and C. Liang, "Frequency-reconfigurable bow-tie antenna with a wide tuning range," *IEEE Antennas Wireless Propag. Lett.*, vol. 13, pp. 1549–1552, 2014.

[10] X. L. Sun, S. W. Cheung, and T. I. Yuk, "Dual-band monopole antenna with frequency-tunable feature for WiMAX applications," *IEEE Antennas Wireless Propag. Lett.*, vol. 12, pp. 100–103, 2013.

[11] A. Zohur, H. Mopidevi, D. Rodrigo, M. Unlu, L. Jofre, and B. A. Cetiner, "RF MEMS reconfigurable two-band antenna," *IEEE Antennas Wireless Propag. Lett.*, vol. 12, pp. 72–75, 2013.

[12] V. Kumar, D. R. Jahagirdar, A. Basu, and S. K. Koul, "Intra-band frequency reconfigurable antenna using RF MEMS technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Dec. 2013, pp. 1–4.

[13] I. Kim and Y. Rahmat-Samii, "RF MEMS switchable slot patch antenna integrated with bias network," *IEEE Trans. Antennas Propag.*, vol. 59, no. 12, pp. 4811–4815, Dec. 2011.

[14] T. Yamagajo and Y. Koga, "Frequency reconfigurable antenna with MEMS switches for mobile terminals," in *Proc. IEEE-APS Top. Conf. Antennas Propag. Wireless Commun.*, Sep. 2011, pp. 1213–1216.

[15] R. Valkonen, C. Luxey, J. Holopainen, C. Icheln, and P. Vainikainen, "Frequency-reconfigurable mobile terminal antenna with MEMS switches," in *Proc. 4th Eur. Conf. Antennas Propag. (EuCAP)*, Apr. 2010, pp. 1–5.

[16] D. Molinero, S. Aghaei, A. S. Morris, and S. Cunningham, "Linearity and RF power handling on capacitive RF MEMS switches," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 12, pp. 4905–4913, Dec. 2019.

[17] B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz, "A miniature DC-70 GHz SP4T switch in 0.13-μm CMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2009, pp. 1093–1096.

[18] D. Wang *et al.*, "High performance SOI RF switches for wireless applications," in *Proc. 10th IEEE Int. Conf. Solid-State Integr. Circuit Technol.*, Nov. 2010, pp. 611–614.

[19] V. Blaschke, A. Unikovski, and R. Zwingman, "An ultra-compact SP4T cellular antenna switch in 3.3 V CMOS thick-film SOI," in *Proc. IEEE Int. Wireless Symp. (IWS)*, Apr. 2013, pp. 1–4.

[20] V. Blaschke, A. Unikovski, and R. Zwingman, "An ultra-compact SP4T cellular antenna switch in 3.3 V CMOS thick-film SOI," in *Proc. IEEE Int. Wireless Symp. (IWS)*, Apr. 2013, pp. 1–4.

[21] W.-W. Lee and B. Jang, "A tunable MIMO antenna with dual-port structure for mobile phones," *IEEE Access*, vol. 7, pp. 34113–34120, 2019.

[22] R. Valkonen, M. Kaltiokallio, and C. Icheln, "Capacitive coupling element antennas for multi-standard mobile handsets," *IEEE Trans. Antennas Propag.*, vol. 61, no. 5, pp. 2783–2791, May 2013.

[23] R. Valkonen, J. Ilvonen, P. Vainikainen, and C. Icheln, "Inherently non-resonant multi-band mobile terminal antenna," *Electron. Lett.*, vol. 49, no. 1, pp. 11–13, Jan. 2013.

[24] K. Lim *et al.*, "A 65-nm CMOS 2 $\times$ 2 MIMO multi-band LTE RF transceiver for small cell base stations," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 1960–1976, Jul. 2018.

[25] N.-C. Kuo *et al.*, "A 0.4-to-4-GHz all-digital RF transmitter package with a band-selecting interposer combining three wideband CMOS transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 11, pp. 4967–4984, Nov. 2018.

[26] M. Kosunen *et al.*, "A 0.35-to-2.6GHz multilevel outphasing transmitter with a digital interpolating phase modulator enabling up to 400MHz instantaneous bandwidth," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 224–225.

[27] A. Behzad *et al.*, "A fully integrated MIMO multiband direct conversion CMOS transceiver for WLAN applications (802.11n)," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2795–2808, Dec. 2007.

[28] J.-M. Hannula, J. Holopainen, and V. Viikari, "Concept for frequency-reconfigurable antenna based on distributed transceivers," *IEEE Antennas Wireless Propag. Lett.*, vol. 16, pp. 764–767, Apr. 2017.

[29] J.-M. Hannula, T. Saarinen, J. Holopainen, and V. Viikari, "Frequency reconfigurable multiband handset antenna based on a multichannel transceiver," *IEEE Trans. Antennas Propag.*, vol. 65, no. 9, pp. 4452–4460, Sep. 2017.

[30] S. Han, C.-L. I, Z. Xu, and C. Rowell, "Large-scale antenna systems with hybrid analog and digital beamforming for millimeter wave 5G," *IEEE Commun. Mag.*, vol. 53, no. 1, pp. 186–194, Jan. 2015.

[31] J.-M. Hannula *et al.*, "Performance analysis of frequency-reconfigurable antenna cluster with integrated radio transceivers," *IEEE Antennas Wireless Propag. Lett.*, vol. 17, no. 5, pp. 756–759, May 2018.

[32] R. Luomaniemi, A. Salmi, A. Lehtovuori, and V. Viikari, "Reducing user effect on mobile antenna systems with antenna cluster technique," in *Proc. 14th Eur. Conf. Antennas Propag. (EuCAP)*, Mar. 2020, pp. 1–5.

[33] J.-M. Hannula, A. Lehtovuori, R. Luomaniemi, T. O. Saarinen, and V. Viikari, "Beneficial interaction of coupling and mismatch in a two-antenna system," in *Proc. 13th Eur. Conf. Antennas Propag. (EuCAP)*, 2019, pp. 1–4.

[34] P. A. J. Nuyts, P. Reynaert, and W. Dehaene, "Continuous-time digital design techniques," in *Continuous-Time Digital Front-Ends for Multistandard Wireless Transmission*. Cham, Switzerland: Springer, 2014, pp. 125–185.

[35] Y. Antonov *et al.*, "A delay-based LO phase-shifting generator for a 2-5GHz beamsteering receiver in 28nm CMOS," in *Proc. IEEE 45th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2019, pp. 389–392.

[36] J. Lemberg *et al.*, "A 1.5–1.9-GHz all-digital tri-phasing transmitter with an integrated multilevel Class-D power amplifier achieving 100-MHz RF bandwidth," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1517–1527, Jun. 2019.

[37] R. Shrestha, R. van der Zee, A. de Graauw, and B. Nauta, "A wideband supply modulator for 20 MHz RF bandwidth polar PAs in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1272–1280, Apr. 2009.

[38] P. Y. Wu and P. K. T. Mok, "A two-phase switching hybrid supply modulator for RF power amplifiers with 9% efficiency improvement," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2543–2556, Dec. 2010.

[39] B. Park *et al.*, "High-performance CMOS power amplifier with improved envelope tracking supply modulator," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 3, pp. 798–809, Mar. 2016.

[40] M. Martelius *et al.*, "A class-D tri-phasing CMOS power amplifier with an extended Marchand-Balun power combiner," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 3, pp. 1022–1034, Mar. 2020.

[41] P. A. Godoy, S. Chung, T. W. Barton, D. J. Perreault, and J. L. Dawson, "A 2.5-GHz asymmetric multilevel outphasing power amplifier in 65-nm CMOS," in *Proc. IEEE Top. Conf. Power Modeling Wireless Radio Appl.*, Jan. 2011, pp. 57–60.

[42] P. Madoglio *et al.*, "A 20dBm 2.4GHz digital outphasing transmitter for WLAN application in 32nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2012, pp. 168–170.

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