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Design of a 240-GHz LNA in 0.13 μm SiGe BiCMOS Technology

Md Najmussadat[#1], Raju Ahamed[#2], Mikko Varonen[*3], Dristy Parveg[*4], Yehia Tawfik[#5], Kari A. I. Halonen[#6]

[#]Department of Electronics and Nanoengineering, Aalto University, Espoo, Finland

[*]VTT Technical Research Centre of Finland Ltd, Espoo, Finland

{[1]md.najmussadat, [2]raju.ahamed,[5]yehia.tawfik, [6]kari.halonen}@aalto.fi, {[3]mikko.varonen,[4]dristy.parveg}@vtt.fi

***Abstract*— In this paper, a seven stage low noise amplifier (LNA) in a 0.13 μm SiGe BiCMOS technology is presented. The LNA has a measured peak gain of 28.5 dB at 240 GHz with a 3-dB bandwidth of 14 GHz. It shows a simulated noise figure of 13.7 dB at 240 GHz. The DC power consumption of this LNA is 97.2 mW with a supply voltage of 3V. This LNA so far represents the highest gain reported in SiGe BiCMOS technology around 240 GHz. The total chip area including the pads of this LNA is 0.45 mm^2.**

***Keywords*— Low Noise Amplifier (LNA), BiCMOS, SiGe, millimeter-wave, MMIC.**

I. Introduction

Due to higher spatial resolution and wider spectral coverage in higher frequency, mm-wave and THz bands became an interesting region for security and medical imaging. Imaging systems operating in these frequency bands consist of heterodyne or direct detection radiometers made of monolithic microwave integrated circuits (MMIC). Resolution of the MMIC based imaging system can be improved if a significant amplification is possible by a low noise amplifier (LNA) with low noise figure (NF). Also, different applications in mm-wave frequencies such as communication system receivers and transceivers for radar systems require LNA [1], [2], [3].

With the evolution of scaling in III-V semiconductor technology, receiver circuits in 200-300 GHz range typically built by InP HEMTs, GaAs mHEMTs or InP HBTs with very good performance have been demonstrated [3], [4], [5]. However, recent advancement in SiGe BiCMOS technology has progressed towards the maximum oscillation frequencies (f_{max}) in the range of 500 GHz. SiGe technology also possesses the feature of high integration level and low cost, capable for good performance in mm-wave applications due to its high f_{max}. Thus SiGe technology becomes a cost effective alternative to conventional III-V for large volume implementation [6].

LNAs with different topologies using SiGe technology over 200 GHz have been previously reported in different studies [7], [8], [9], [10]. In this paper, a seven stage cascode low noise amplifier as shown in Fig. 1 is presented at 240 GHz in a 0.13 μm SiGe BiCMOS technology. This LNA demonstrated a maximum measured gain of 28.5 dB at 240 GHz and a simulated noise figure of 13.7 dB with a 14 GHz bandwidth while dissipating 97.2 mW of DC power.

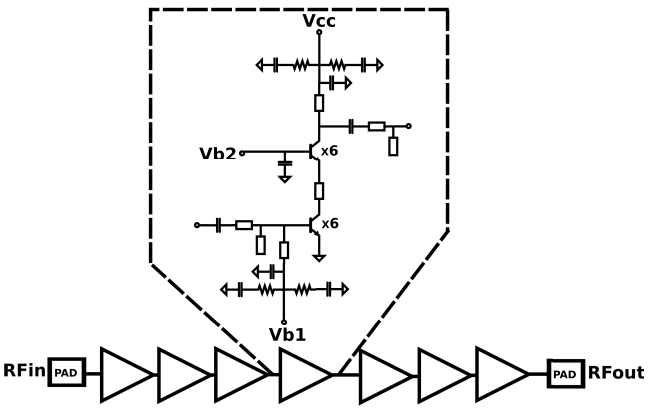

Fig. 1. Schematic of the designed Low Noise Amplifier.

II. Circuit Design

Low noise amplifiers (LNA) are important building blocks in receivers. Since LNA is the first block in the receiver chain, the gain and noise figure of the LNA plays a critical role to determine the noise figure of whole receiver system. Therefore, low noise figure and high gain are major requirements for the LNA design over the frequency band of interest.

In LNA design, choosing appropriate topology plays an important role at higher frequency. It still remains a challenge to design a stable amplifier at very high frequencies with high gain due to lower breakdown voltage of the transistors. If we compare the commonly used LNA topologies in mm-wave applications, it is seen that common-emitter (CE) topology has the lowest noise figure in comparison to common-base (CB) and cascode topologies [11]. However, in the frequency range above 240 GHz, maximum available gain (MAG) of the transistors drops significantly for most of the applications [12]. Due to this, gain in each stage of common emitter topology at 240 GHz reduces dramatically compared to frequency range below 100 GHz. It is seen in [8] that, cascode topology provides much higher gain compared to CE or CB topology. However, noise figure in cascode topology is somewhat higher in comparison to single stage CE and CB topology but it is reasonable if we compare it with two stages of CE. Fig. 2 shows the comparison of different topologies for maximum gain and minimum noise figure. In this design, cascode topology is chosen for each stage due to higher gain, higher

isolation and higher 3-dB bandwidth.

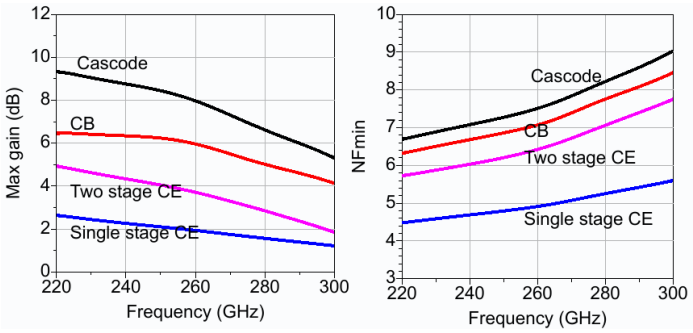

Fig. 2. Comparison between different topologies.

The simplified block diagram of the designed LNA with a schematic of a single stage is shown in Fig. 1. The amplifier has seven cascode stages and each stage contains two transistors and each transistor contains 06 multipliers (X6) in cascode topology. Transistor size are chosen considering the favorable source impedance point for minimum noise figure and higher gain. Source impedance points for minimum noise figure in a single cascode stage with different transistor sizes are shown in Fig. 3. From Fig. 3, it seems that X4 has better source impedance for matching. However, X6 provides better gain compared to X4. Transistor modelling is done with careful attention as it has significant effect on gain perfromance [13]. High frequency parasitic effects were taken into account by performing RC extraction of the transistor upto circuit ground level. For accessing the transistor terminals at topmost metal level, an access structure was made from ground layer to topmost metal layer which is shown in Fig. 4. Input matching, output matching as well as inter-stage matching are done by transmission lines.

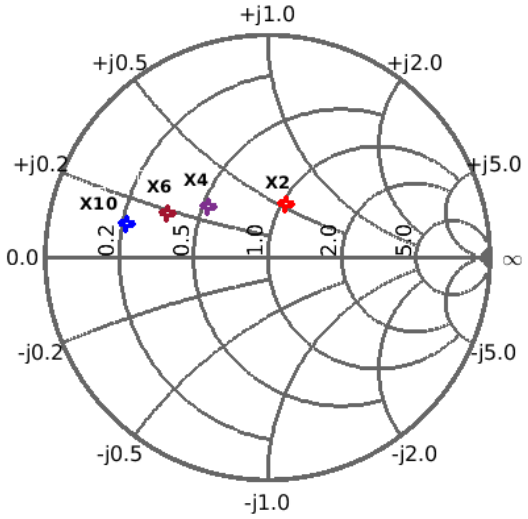

Fig. 3. Source impedance points for minimum noise figure with different transistor size.

Unconditional stability of each stage of the amplifier was checked by stability factor (K) simulation and found each stage unconditionally stable. Overall amplifier's K factor value was greater than one from 1-300 GHz range which indicate the unconditional stability of the designed seven stage cascode LNA. We also simulated stability measure (B1) and Mu factor which ensure the stability of the LNA.

It is seen in electromagnetic (EM) simulation that increasing pad size has a significant effect on macthing at 240 GHz due to higher pad capacitances. Therefore, a smaller pad with a dimension of 40 µm x 40 µm was used in this design. EM simulation to obtain accurate modeling of the transistor access, transmission lines, MIM capacitors and RF pads were performed in ADS momentum.

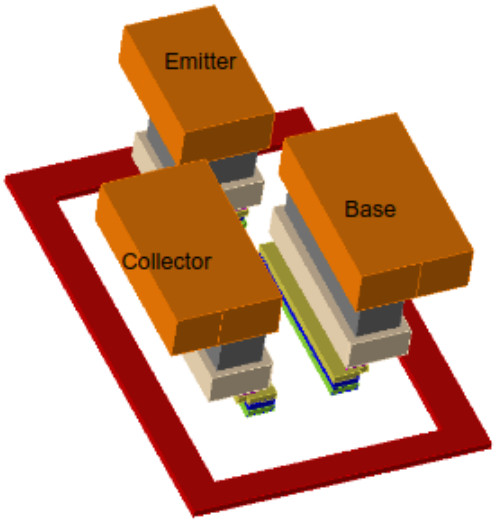

Fig. 4. Access structure for transistor terminals.

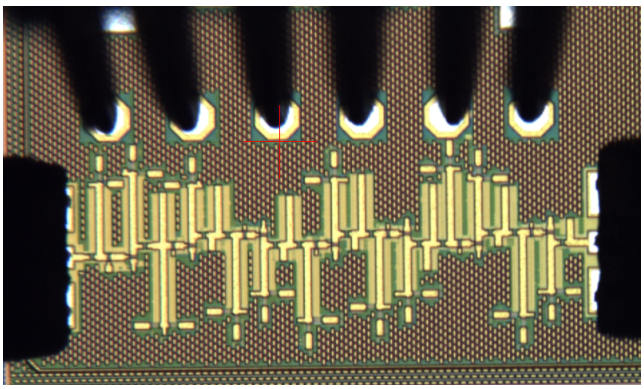

Fig. 5. The micrograph of seven stage cascode LNA

III. Measurement Results

The LNA was fabricated in IHP's 0.13 µm SiGe BiCMOS process. This process exibits of f_t/f_{max} of 300/500 GHz. The process BEOL provides seven metal layers including two thick top layers and MIM capacitors [14]. The chip photo is shown

Table 1. Performance comparison of LNAs around 240 GHz

Reference	Technology	Frequency (GHz)	Gain (dB)	Bandwidth (GHz)	Noise Figure (dB)	Pdc (mW)	FOM (GHz/mW)	Area (mm^2)
[6]	130nm BiCMOS	210	14	28	13 (simulated)	151.2	0.04	0.059
[7]	130nm BiCMOS	245	18	8	11	303.4	0.018	0.155
[8]	250nm BiCMOS	245	12	26	13.7 (simulated)	28	0.17	0.193
[9]	130nm BiCMOS	233	22.5	10	12.5 (simulated)	68	0.117	0.07
[10]	130nm BiCMOS	260	15	16.5	–	112	–	0.35
This work	130nm BiCMOS	240	28.5	14	13.7 (simulated)	97.2	0.17	0.45

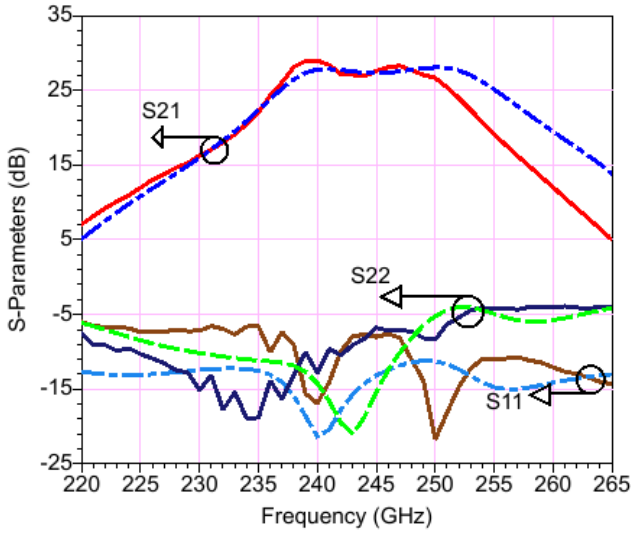

Fig. 6. S-parameter of LNA. Solid lines represent the measured data. The dashed line represent simulated values.

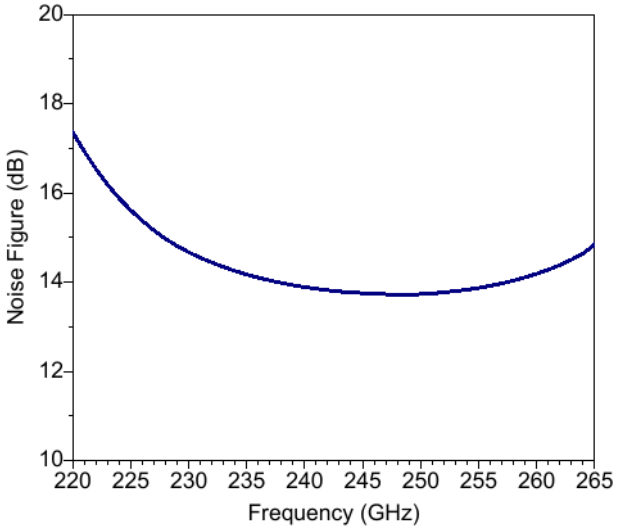

Fig. 7. Simulated noise figure of the LNA.

in Fig. 5. The total area of the LNA is 1000 µm x 450 µm including the RF and DC pads.

S-parameters of the implemented LNA were measured on-wafer over 220-325 GHz. An Agilent millimeter-wave PNA E8361C network analyzer in combination with WR3 VNA extender using 100 µm pitch GSG on-wafer probes. Calibration was done in LRRM calibration method. Fig. 6 represents the measured and simulated S-parameters of the LNA. Bias points of the LNA was Vb1=0.89V, Vb2=2.3V and Vcc=3V which results a DC power consumption (P_{dc}) of 97.2 mW. The LNA shows a measured peak gain of 28.5 dB at 240 GHz. The 3-dB bandwidth is 14 GHz from 236.8 GHz to 250.8 GHz. It can be seen from Fig. 6 that the input and output return losses of this LNA around 240 GHz are better than 15 dB and 10 dB, respectively. It exhibits a simulated noise figure of 13.7 dB which is shown in Fig. 7.

The performance of this LNA and other published LNAs over 210 GHz are presented in Table 1. The LNAs performance can be compared by the figure of merit (FOM) [15], [16]. The FOM is defined as:

$$\text{FOM} = \frac{S21_{mag} \cdot \text{Bandwidth (GHz)}}{[NF_{mag} - 1] \cdot P_{dc}\,(\text{mW})} \tag{1}$$

where $S21_{mag}$ and NF_{mag} are the magnitudes of S21 and noise figure respectively. From the Table 1, it can be found that implemented cascode LNA has highest gain and highest FOM compared to others LNA in the frequency range of 240 GHz.

IV. Conclusion

The design and implementation of a low noise amplifier (LNA) has been presented in a 0.13 µm SiGe BiCMOS technology. The measured LNA achieved a gain of 28.5 dB with a bandwidth of 14 GHz. The LNA consumes 97.2 mW of DC power with a chip area of 0.45 mm^2 including pads. This LNA demonstrate highest gain around 240 GHz SiGe LNAs reported so far. Also the higher FOM represents that designed LNA has better performance in terms of GHz/mW.

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