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All-parylene flexible wafer-scale graphene thin film transistor

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ABSTRACT

Graphene is an ideal candidate as a component of flexible/wearable electronics due to its two-dimensional nature and low gate bias requirements for high quality devices. However, the proven methods for fabrication of graphene thin film transistors (TFTs) on fixed substrates involve using a sacrificial polymer layer to transfer graphene to a desired surface have led to mixed results for flexible devices. Here, by using the same polymer layer (parylene C) for both graphene transfer and the flexible substrate itself, we produced graphene TFTs on the wafer-scale requiring less than |2 V| gate bias and with high mechanical resilience of 30,000 bending cycles.

1. Introduction

Two-dimensional (2D) materials have been extensively studied since the seminal work with graphene in 2004 [1]. In recent years, its research has transferred from fundamental to be more industrially targeted. Besides high charge carrier mobility (μ), flexibility and optical transparency make graphene desirable for next-generation flexible electronic devices. For many applications, such as transparent conductors, the current market standard is indium tin oxide (ITO), while for flexible applications ITO cannot provide even minimal flexibility or mechanical resilience usually associated with polymers [2]. Meanwhile, miniaturization in the semiconductor industry and introduction of additional performance requirements such as mechanical stress and low power consumption create new figures of merit (FOM) for the future electronic components [3].

Graphene, as one of the most known 2D material, has shown rapid progress towards flexible electronic applications over the last several years [4–7]. The application area and role of graphene in devices may vary from simple transparent conductive electrodes or active material in physical, chemical and biological sensors to channel layer in transistors [8]. A key features for an ideal transistor, as the central device building block in modern electronics, would be a high on/off ratio, high carrier mobility and thermal conductivity, long-term stability of semiconductor–dielectric interface and many others [9]. Unfortunately, limitations of material's properties force us to agree with some tradeoffs. Hence, graphene-based field-effect transistors (GFET) possess high off-current and a low on/off ratio, which limits their logic application [10]. A typical on/off ratio of CVD graphene-based devices is as low as 5, thus we are we are not focusing on improvement of this characteristic [11]. On the other hand, extraordinarily high mobility opens path to high-frequency application [12,13]. Moreover, considerable efforts have been done to "broaden" graphene zero-band gap and enhance on/off ratio by utilizing bilayer, patterning graphene to nanoribbons and using hybrid graphene/organic semiconductor as active layers [14,15]. Particularly, hybrid materials can be beneficial for both parts as organic field-effect transistors (OFET) have achieved significant results in on/off ratio, however the average field-effect mobility remains very low [16]. Nevertheless, a successful integration of graphene-based TFTs on flexible substrates can be considered as a one step forward. A significant challenge in such devices brings the requirement for optimized gate dielectrics to achieve stable and reliable performance. Low operating voltages (achieved either through high-k gate, or with devices with low residual carrier doping), as well as bending tolerance are very important for successful operation of flexible graphene devices. Great efforts on high-capacitance (high-k) gate dielectrics for flexible low-voltage transistors have been reported in various research articles [17–19]. However, a top-gate geometry significantly limits process temperatures and post-thermal treatments for gate dielectric materials to 200 °C or lower. On the other hand, poly-para-xylylene polymer (known as parylene) has been reported in recent research as a gate dielectric [16,20–22], a substrate [6,23] and a passivation layer against moisture [24,25]. In particular, parylene C, which has chlorine functional group added to the

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monomer unit, is known for improved dielectric constant and the highest biocompatibility rating for plastics (ISO-10993, USP class VI). The parylene deposition process taking place in vacuum enables pinhole-free thin film formation and mechanical flexibility.

Thus, parylene C can contribute to the development of scalable integrated manufacturing pathways for the most industrially favored graphene growth process: chemical vapor deposition (CVD) on catalytic substrates such as Cu or Ni. A direct graphene transfer from catalytic substrate without supporting polymers and irreplaceable protective layer would preserve it from undesired contaminants during processing [26,27]. Compare with other polymers such as PMMA and PDMS, parylene C is more suitable for processing due to stability at high temperatures and ability to resist basic solvents. The cleanest graphene device interfaces have been achieved with h-BN crystals [28–30] and metal oxide layers such as Al_2O_3, TiO_2 and NiO [25,31,32]. However, the use of these materials is limited by either scalability, or post-process functionality in device performance. The use of parylene C to transfer graphene or as a dielectric layer would be efficient and clean way to process graphene-based devices. In particular, a reduction of thermal or physical stresses on graphene layer during parylene deposition and nanometer accuracy control of film thickness allow to utilize it in transfer and fabrication processes [6].

In this paper, we utilize parylene C (from here and below also as parylene) as the support layer for transfer of wafer-scale CVD-grown graphene, and fabricate flexible TFT with graphene as channel and parylene C as both gate and substrate. The graphene transistors have a top-gate coplanar structure and fabrication steps are compatible with standard planar processes. In order to improve adhesion between graphene transferred on parylene we tune surface property by deposition of thin alumina (Al_2O_3) film by low temperature atomic layer deposition (ALD) and characterize its wettability. The fabricated structures are carefully evaluated and show high electric performance as well as parylene C demonstrate reliable dielectric strength.

2. Description of fabrication process

The initial preparation was based on standard SiO_2/Si substrates which are fully compatible with existing cleanroom processes. 25 μm of parylene C was deposited on HMDS treated SiO_2/Si, and followed by annealing at 360 °C for 30 min on the prefabricated substrate to decrease surface roughness (see Supporting information Figure S1). In order to achieve good adhesion and high mobility of parylene/graphene film on parylene/SiO_2/Si substrate, we utilized 10 nm of ALD Al_2O_3 as an intermediate layer between graphene and parylene substrate. Thin ALD Al_2O_3 layers could incorporate with other polymer to improve barrier performance without detrimental impact on flexibility [24]. In this work, Al_2O_3 incorporates with parylene to tune surface wettability. The adhesion of graphene to the substrate and unintended doping remain the most critical barriers for large-scale flexible graphene devices. Surface roughness of parylene/SiO_2/Si substrate and Al_2O_3/parylene/SiO_2/Si stacks were evaluated by atomic force microscopy (AFM) and wettability surface properties by contact angle (CA) measurements. Ideally, pristine graphene has hydrophobic behaviour with CA ~ 92° [33], which turns to more hydrophilic (or slightly hydrophobic) in real experiments with CA ~ 68° [34]. Substrates with hydrophobic behaviour (CA > 92°) would be beneficial for pristine graphene [35]. However, while wettability of CVD graphene films increases with processing, a substrate with matching hydrophobicity would be more favourable because surfaces with similar wetting properties would have similar surface energies that result in better bonding. ALD Al_2O_3 tends to change surface properties of graphene depending on deposition conditions [34]. The final Al_2O_3 surface chemistry can be controlled by ending the ALD process at trimethylaluminum (TMA) pulse and purge or water vapor pulse and purge, which makes surface more hydrophobic or hydrophilic, respectively. Roughness independent tunable wettability of Al_2O_3 films has allowed to find the most energy preferable surface of prefabricated substrate for graphene transfer.

Fig. 1 shows graphene TFT fabrication process with parylene C used for both dielectric layer and substrate itself. Prior to Cu removal, CVD grown graphene film covered with 500 nm thick parylene C layer was immersed to deionized water (DIW) to oxidize Cu and reduce adhesion with graphene (step 1) [36]. After parylene/graphene film was transferred onto the prefabricated Al_2O_3/parylene/SiO_2/Si substrate (step 2), the stack was annealed at 360 °C for 30 min, which caused a reduction of parylene C thickness deposited on graphene to ~ 300 nm. Optimization data on parylene C thickness, roughness and thickness reduction by annealing is shown in Supporting information Table S1. Then one-dimensional (1D), edge type of contacts were formed by O_2 plasma parylene/graphene etching, followed by Cr/Au evaporation at an angle of 5° from each side (step 3). These 1D metal-to-graphene contacts show very low line resistivity of ~ 100 Ω/μm in comparison to traditional surface contacts [37]. Graphene TFT channel patterning was followed by gate electrode formation divided into two parts (step 4). Firstly, Ti/Au metal finger above fluorinated parylene C channel area were patterned. The fluorination improves adhesion to parylene surface [38–40], however it reduces the parylene C thickness by 150 nm, resulting in final 150 nm thickness parylene film on the graphene TFT. Moreover, Ti was chosen as better adhesion metal layer for the parylene top gate [41,42]. Secondly, the whole structure was covered with a 50 nm parylene layer to avoid edge contacting of gate electrode. Finally, through openings to the gate electrode performed by O_2 plasma etching of parylene, metal finger was connected to distant contact pads by Ti/Au evaporation. At the last stage of fabrication process, parylene/graphene/Al_2O_3/parylene structure was delaminated from SiO_2/Si substrate by gentle peeling (step 5). Using the reduced adhesion energy between parylene and SiO_2/Si by HMDS [43], cutting parylene layer around the edges with a sharp blade and gentle manual force was sufficient to achieve delamination. In order to facilitate reliability of fabrication process, several arrays consisted of 6 devices in each were manufactured and served for different examination. Fig. 2 shows example of parylene/graphene/parylene TFT arrays fabricated on 4 in.

A reference array was also fabricated, where graphene layer was transferred via a conventional PMMA method and 30 nm of ALD Al_2O_3 served as a gate dielectric. Fabrication of a such reference devices using exactly the same processes, chemicals, and cleanroom allows us to determine that the TFTs performance improvements are directly as a result of our parylene process and not due to potentially many other confounding factors that would be introduced if compared to PMMA-based devices made by other methods. For the reference devices, the bottom contact patterning was fabricated first, then 2 nm of seeding layer was deposited prior to ALD of Al_2O_3. Comparison of graphene doping level by different seeding layers utilized for further Al_2O_3 deposition is shown in Supporting information Figure S2 and the deposition details in Table S2.

3. Results and discussion

Fig. 3 shows AFM images of parylene/SiO_2/Si substrate roughness before and after Al_2O_3 deposition, the insets show CA measurement results. It is important to mention, that there was no significant change in average roughness (R_{ave}) or the root mean square roughness (R_{rms}) before and after Al2O3 deposition R_{ave} remained ~ 6 nm. Meanwhile, the substrate with deposited Al_2O_3 showed better adhesion to graphene and resulted in higher transfer uniformity.

Utilizing the supporting substrate as a functional layer in further processing has a number of benefits, such as protecting graphene film from undesired polymer residues affecting the transport properties of graphene [44] as well as providing a consistent moisture barrier present from the beginning of graphene processing. Our graphene films were transferred with the support of 500 nm parylene film directly deposited on graphene on Cu, and after several processing steps the thickness of parylene C film was reduced to 150 nm in the final device structure

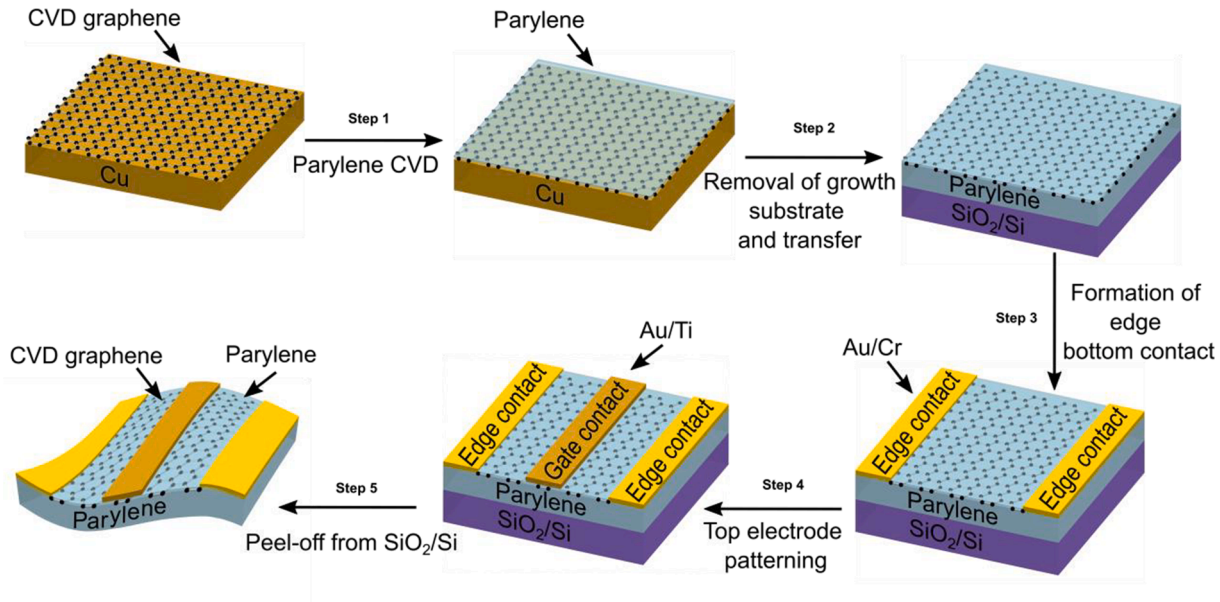

Fig. 1. Fabrication process of graphene TFT with parylene C as dielectric layer and the substrate. Step 1: 500 nm parylene C deposition. Step 2: graphene/parylene film transfer onto the prefabricated Al_2O_3/parylene/SiO_2/Si substrate and annealing of whole structure. Step 3: Formation of edge bottom contact. Step 4: Channel patterning, fluorination of channel area, gate electrode formation. Step 5: Peel-off from SiO_2/Si.

where it was utilized as a gate dielectric.

3.1. Transport measurements

Transferred parylene/graphene films with dimensions of 2 × 2 cm^2 were electrically characterized in air using a Linkam LN600P stage [11]. Fig. 4(a) shows average gate-dependent transport curves for a devices array after removal from the Si substrate (black dashed line), and after 1000 bends (blue solid line). Prior to bending the device showed a low level of residual n-doping (≈ 1.5 × 10^{11} cm^{-2}) and μ of ≈ 4500 cm^2/Vs. Despite polymer *residues* being attributed to decreased graphene device performance, graphene on smooth/continuous polymer can lead to excellent transport characteristics [45], consistent with our polymer-on-graphene device design. The device required V_G <|1 V| to observe the charge neutrality point (CNP).

This array was then subjected to 1000 bending cycles and the TFT characteristics were remeasured. The CNP shifted to right and a residual p-doping was observed at ≈0.5 × 10^{11} cm^{-2}, with μ at ≈ 1500 cm^2/Vs. The post-bending device performance degraded (increased n, decreased μ) which is attributed to mechanical damage from bending introducing defects which provide electrons to the channel requiring additional positive V_G to observe the CNP, and with the defects acting as scatterers reducing μ [46]. Importantly, the total applied gate bias required to observe the CNP was less than |1 V| for both conditions. Moreover, leakage currents through the top-gate were always less than 0.1 nA/μm^{-2} over the full $V_{gs\text{-}top}$ bias range (see supporting information Figure S3a). For the PMMA-transferred reference array (no bending) the residual doping was significantly larger, measured as $n \approx 2 \times 10^{12}$ cm^{-2} (CNP at $V_G = 16$ V) with μ of ≈ 1000 cm^2/Vs as shown in supporting information Figure S3b.

In addition, device capacitance and dielectric breakdown were measured using the device configuration shown in supporting information Figure S5. With 12 devices (2 arrays) measured, the median capacitance was 10 nF/cm^2, which is consistent with previous measurements of parylene C of similar thicknesses [47]. The median breakdown voltage was 160 V, indicating a dielectric strength of 0.89 V/nm. The breakdown voltage was nearly two orders of magnitude greater than the measurement range required for graphene TFTs in Fig. 4 (a).

In order to test degradation in ambient conditions, additional devices were measured by van der Pauw method using a Hall system at a room temperature in ambient air, with magnetic field strength of 1 T. A parylene-gated device with Hall mobility of ~ 2000 cm^2/Vs was measured on the first day after bottom contact patterning and again at the end of the fabrication process. The device was stored for a month in ambient conditions showed no degradation in comparison with a reference sample, where gate dielectric deposition was performed after bottom contact patterning (see Supporting information Figure S4). In addition to low mobility degradation, device processing sequence shown on Fig. 1 enables fabrication of hysteresis-free GFET with long-term stability by measuring graphene device at a rate of approximately 1 V/s change for the gate bias [11]. Moreover, consistent fabrication process including annealing in vacuum, deposition of passivation/dielectric layer and following annealing has proven low residual charge hysteresis [48] and linked to that neglectable mobility degradation.

3.2. Bending measurements

The performance of a flexible parylene gated array was measured as a function of *number of bends* as described previously [6] and shown in Fig. 4(b) inset. No significant change in devices conductivity was observed between 1 and 10,000 bending cycles with each bend equivalent to 2% strain (as determined [6]). A slight increase in conductivity (σ) (>5%) is measurable over the 10,000 cycles, this effect may be attributed to reversible doping changes from variations in ambient humidity [49] or permanent damage resulting in a doping increase and the subsequent increase in measured σ. The devices then showed significant σ degradation of over 90% after ≈30,000 cycles before becoming unmeasurable. In comparison, the reference array (Figure S4) was no longer measurable when removed from the fixed substrate before even a single bend. The full degradation of devices is likely caused by cracks caused physical separation from a source and drain contacts or because of separation of graphene from a metal contact.

4. Conclusion

Fabrication of a scalable flexible parylene-graphene transistors was realised and requirement for low operating voltages (V_G< |1 V|) fulfilled. Parylene/graphene/parylene transistors showed mobilities of μ

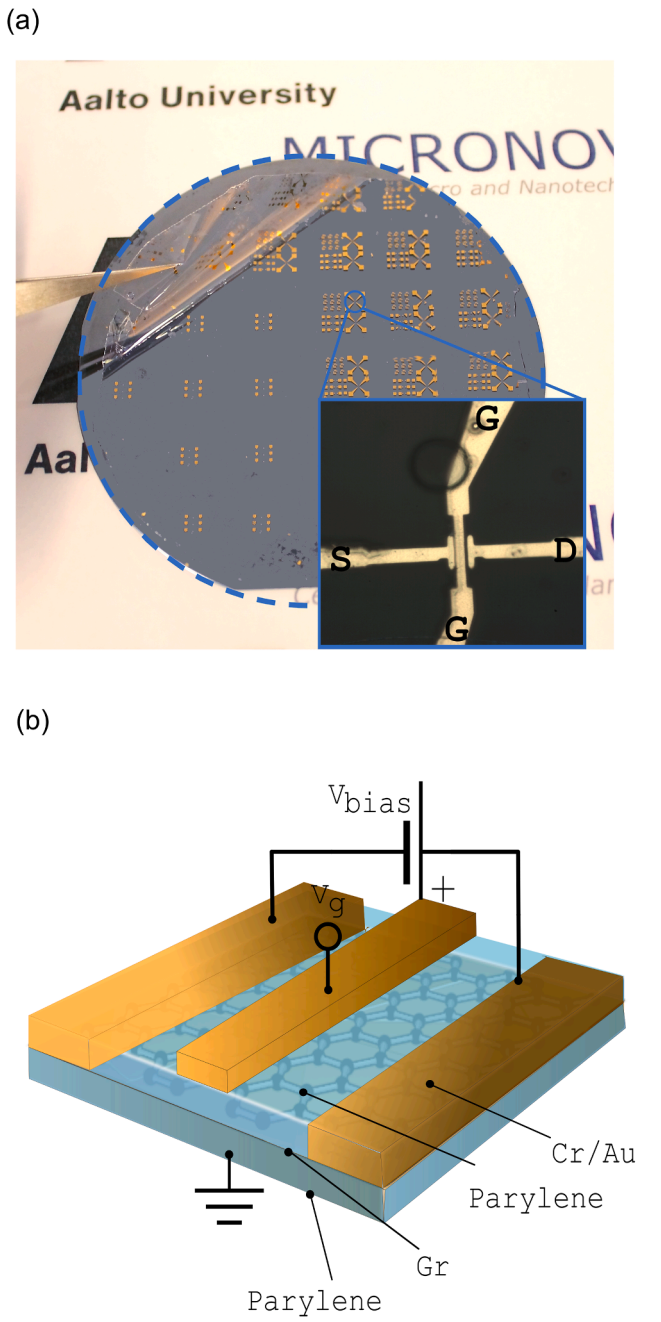

Fig. 2. (a) Graphene based TFT arrays on 4″ wafer, the inset shows optical microscope image of a fabricated TFT device, (b) Schematic illustration showing the structure of the parylene/graphene/parylene TFT device.

= 4500 cm^2/Vs before bending and 1500 cm^2/Vs and after 1000 bending cycles of 2% strain. The conductance of parylene/graphene/parylene devices showed no significant change in conductance after 10,000 bending cycles, and were still operating after 30,000 cycles. Such a result can be explained by mechanical stress during bending causing the degradation of the metal-contact parylene interface or large isolating cracks in graphene. Devices with full parylene fabrication showed significantly better device performance and flexibility resilience in comparison to an equivalent traditional PMMA-transferred devices.

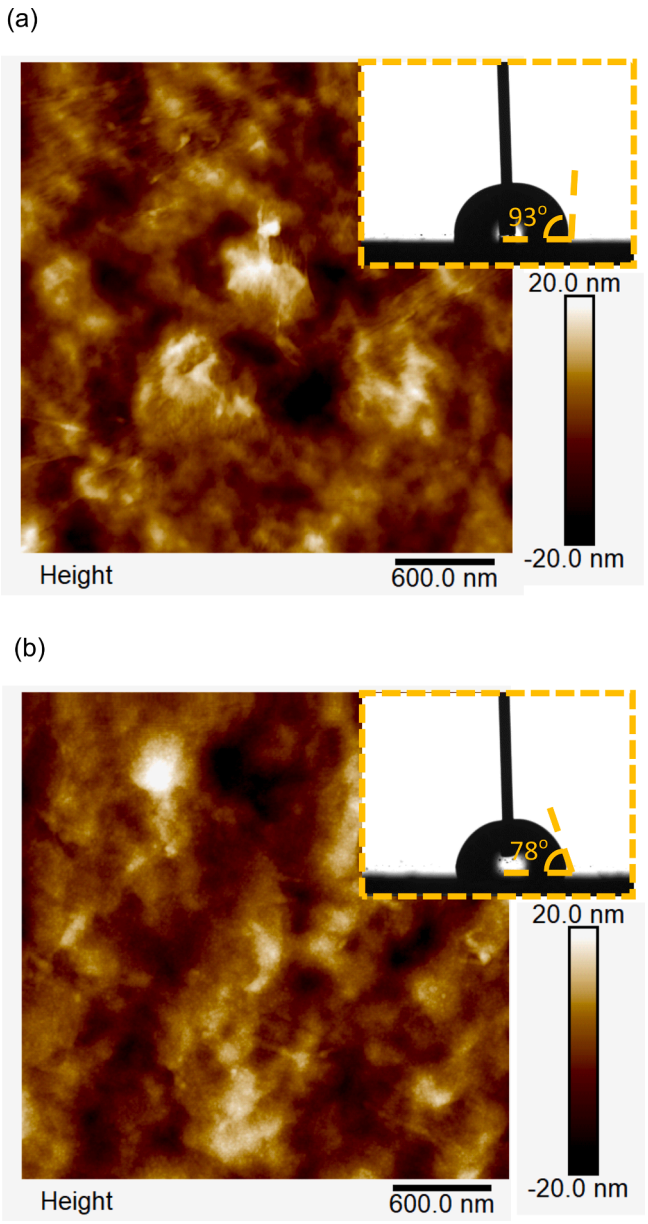

Fig. 3. AFM images of substrate roughness (a) parylene/SiO_2/Si substrate roughness, (b) Al_2O_3/parylene/SiO_2/Si substrate roughness. The insets show CA measurements.

5. Methods

5.1. CVD

Growth of Graphene. Growth of large-area 6″ monolayer graphene was carried out by commercial CVD system (Black Magic CVD system Aixtron BM6) and home-built rapid photo-thermal CVD system [50]. Commercial Cu foils (25 μm, 99.8% purity, Alfa Aesar product 7440508) were used as the substrate. Typical growth process in Black Magic CVD system was performed at a constant pressure of 4.1 mbar. First, Cu foil was annealed for 30 min at 850 °C using a 20 sccm flow of H_2 diluted by 1500 sccm of Ar. Reduction step was followed by a 10 min graphene deposition at 1025 °C by introducing additional 7 sccm of CH_4. Subsequently, the CH_4 flow was closed, and the chamber was cooled to a temperature below 150 °C and opened to ambient air. Electropolishing in orthophosphoric acid for 15 min removed tarnishing and roughness of Cu surface. The electrolytic solution was prepared using 55% H_3PO_4 and

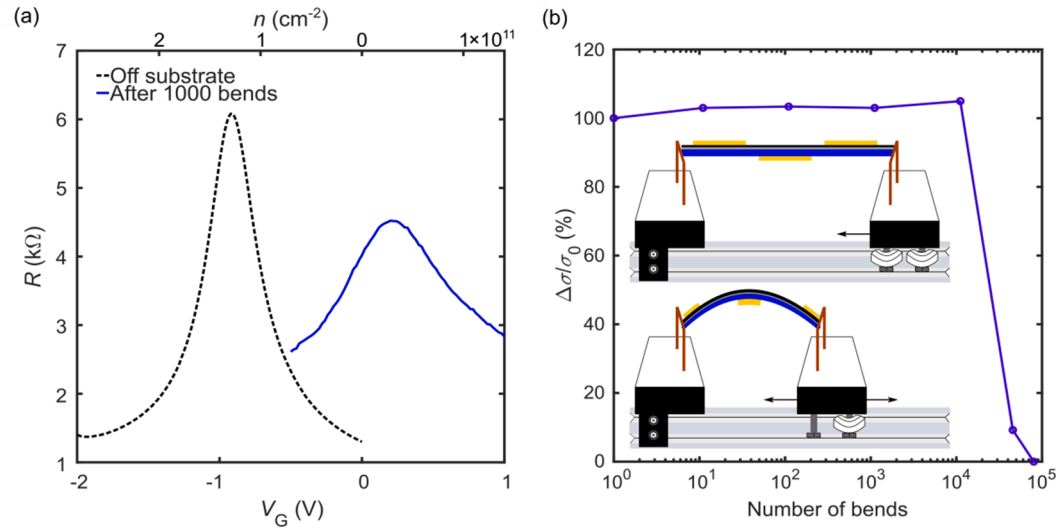

Fig. 4. (a) Gate-dependent transport properties of parylene-based graphene devices. (b) Change in conductance of flexible graphene device. Inset: Schematic of bending machine in extended and bent position equivalent to 2% strain.

two-Cu-electrode system was polarized by −1.5 V.

5.2. Graphene/parylene films preparation

Parylene C deposition was carried out in a commercially available deposition system PDS-2010 Labcoater 2 (Specialty Coating Systems). 25 g and 15 g of di-para-xylylene (Parylene C dimer) were used to conformally deposit 25 μm and 15 μm films, respectively. An aqueous solution of NaOH was employed for electrochemical delamination (bubbling transfer) as an electrolyte while Cu was polarized at −5 V to delaminate parylene/graphene.

5.3. ALD

Deposition of Al_2O_3 layers was carried out by commercial ALD reactor Beneq TFS-500 at 120 °C with TMA and H_2O as precursors with nitrogen as the carrier gas. For Al_2O_3 deposition on graphene, a thin Al film (nominally 2 nm) was used as a seeding.

5.4. Characterization

Commercially available Reflectometer FilmTek 2000M was utilised for parylene thickness measurements. Data was collected and averaged from several points according to software measurement map and fitting curve. All thickness measurements were carried out on monitor parylene/SiO_2/Si piece.

AFM images and surface roughness were characterized by using an atomic force microscope (AFM, Dimension 3100 by Digital Instruments-Veeco, Plainview, NY) and silicon AFM tips with apex radius of 10 nm in tapping mode.

The contact angle (CA) measurements were carried out on commercial Biolin Theta Contact Angle Meter, where water drops on the surface of graphene/Cu samples were measured as follows: a droplet of the liquid was deposited by a syringe which was positioned above the sample surface and the image captured by a high resolution camera was analysed to determine the contact angles.

Hall system used to perform measurements by van der Pauw method had a sample size of 2 × 2 cm^2 and it operated at a room temperature in ambient air, with the magnetic field strength of 1 T.

Graphene TFT measurements were performed with a custom-built setup based on a Linkam LN600P stage with environmental and temperature control described here [51]. The LabVIEW program was used to control source–drain and gate voltages (Keithley 2400), multiplexing/voltage measurements (Keithley 2700 with Keithley 7709 multiplexing unit). The measurements were performed at room temperature at atmospheric pressure.

5.5. Fabrication process

The parylene/graphene etching for contact defining was performed in Oxford Instruments Plasmalab80Plus parallel plate RIE system with water cooled graphite biased substrate electrode. The process gases were O_2 and Ar at pressure of 10 mTorr and forward power of 50 W for 3 min. Fluorination of parylene C film was performed also in Oxford Instruments Plasmalab80Plus with SF_6 flow of 100 sccm, forward power of 100 W and 20 mTorr pressure for 1 min.

Declaration of Competing Interest

None.

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Appendix A. Supplementary material

Supplementary data to this article can be found online at https://doi.org/10.1016/j.apsusc.2021.149410.

References

[1] K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, Y. Zhang, S.V. Dubonos, I. V. Grigorieva, A.A. Firsov, Electric field effect in atomically thin carbon films, Science. 306 (2004) 666–669, https://doi.org/10.1126/science.1102896.
[2] P. Mustonen, D.M.A. Mackenzie, H. Lipsanen, Review of fabrication methods of large-area transparent graphene electrodes for industry, Front. Optoelectron. (2020) 1–23.
[3] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee, L. Colombo, Electronics based on two-dimensional materials, Nat. Nanotechnol. 9 (2014) 768–779, https://doi.org/10.1038/nnano.2014.207.

[4] S. Bae, H. Kim, Y. Lee, X. Xu, J. Park, Y. Zheng, J. Balakrishnan, T. Lei, H.R. Kim, Y. I. Song, Y. Kim, K.S. Kim, B. Ozyilmaz, J. Ahn, B.H. Hong, S. Iijima, Roll-to-roll production of 30-inch graphene films for transparent electrodes, Nat. Nanotech. 5 (2010) 574–578, https://doi.org/10.1038/nnano.2010.132.

[5] S. Lee, J. Kim, H. Jang, S.C. Yoon, C. Lee, B.H. Hong, J.A. Rogers, J.H. Cho, J. Ahn, Stretchable Graphene Transistors with Printed Dielectrics and Gate Electrodes, Nano Lett. 11 (2011) 4642–4646, https://doi.org/10.1021/nl202134z.

[6] M. Kim, A. Shah, C. Li, P. Mustonen, J. Susoma, F. Manoocheri, J. Riikonen, H. Lipsanen, Direct transfer of wafer-scale graphene films, 2D Materials, 2017.

[7] M. Marchena, F. Wagner, T. Arliguie, B. Zhu, B. Johnson, M. Fern, Dry transfer of graphene to dielectrics and flexible substrates using polyimide as a transparent and stable intermediate layer Dry transfer of graphene to dielectrics and flexible substrates using polyimide as a transparent and stable intermediate layer, 2D Mater. 5 (2018).

[8] B. Zhan, C. Li, J. Yang, G. Jenkins, W. Huang, X. Dong, Graphene field-effect transistor and its application for electronic sensing, Small. 10 (2014) 4042–4065.

[9] F. Schwierz, Graphene transistors: status, prospects, and problems, Proc IEEE. 101 (2013) 1567–1584.

[10] Z. Zhu, I. Murtaza, H. Meng, W. Huang, Thin film transistors based on two dimensional graphene and graphene/semiconductor heterojunctions, RSC Adv. 7 (2017) 17387–17397.

[11] D.M.A. Mackenzie, J.D. Buron, P.R. Whelan, J.M. Caridad, M. Bjergfelt, B. Luo, A. Shivayogimath, A.L. Smitshuysen, J.D. Thomsen, T.J. Booth, L. Gammelgaard, J. Zultak, B.S. Jessen, P. Bøggild, D.H. Petersen, Quality assessment of graphene : Continuity, uniformity, and accuracy of mobility measurements, Nano Res. 10 (2017) 3596–3605, https://doi.org/10.1007/s12274-017-1570-y.

[12] C. Yan, J.H. Cho, J. Ahn, Graphene-based flexible and stretchable thin film transistors, Nanoscale. 4 (2012) 4870–4882.

[13] S. Lee, H.Y. Jang, S. Jang, E. Choi, B.H. Hong, J. Lee, S. Park, J. Ahn, All graphene-based thin film transistors on flexible plastic substrates, Nano Lett. 12 (2012) 3472–3476, https://doi.org/10.1021/nl300948c.

[14] P. Jangid, D. Pathan, A. Kottantharayil, Graphene nanoribbon transistors with high ION/IOFF ratio and mobility, Carbon. 132 (2018) 65–70.

[15] T. Ha, D. Akinwande, A. Dodabalapur, Hybrid graphene/organic semiconductor field-effect transistors, Appl. Phys. Lett. 101 (2012), 033309.

[16] E. Stucchi, G. Dell'Erba, P. Colpani, Y. Kim, M. Caironi, Low-voltage, printed, all-polymer integrated circuits employing a low-leakage and high-yield polymer dielectric, Adv. Electron. Mater. 4 (2018) 1800340.

[17] M. Xiao, C. Qiu, Z. Zhang, L.M. Peng, Atomic-layer-deposition growth of an ultrathin HfO2film on graphene, ACS Appl. Mater. Interfaces. 9 (2017) 34050–34056, https://doi.org/10.1021/acsami.7b09408.

[18] H.G. Kim, H.B.R. Lee, Atomic Layer Deposition on 2D Materials, Chem. Mater. 29 (2017) 3809–3826, https://doi.org/10.1021/acs.chemmater.6b05103.

[19] B. Wang, W. Huang, L. Chi, M. Al-Hashimi, T.J. Marks, A. Facchetti, High- k Gate Dielectrics for Emerging Flexible and Stretchable Electronics, Chem. Rev. 118 (2018) 5690–5754, https://doi.org/10.1021/acs.chemrev.8b00045.

[20] S.S. Sabri, P.L. Levesque, C.M. Aguirre, J. Guillemette, R. Martel, T. Szkopek, Graphene field effect transistors with parylene gate dielectric, Appl. Phys. Lett. 95 (2009) 10–13, https://doi.org/10.1063/1.3273396.

[21] E.Y. Shin, E.Y. Choi, Y.Y. Noh, Parylene based bilayer flexible gate dielectric layer for top-gated organic field-effect transistors, Organ. Electron.: Phys., Mater., Appl. 46 (2017) 14–21, https://doi.org/10.1016/j.orgel.2017.04.005.

[22] D.W. Park, H. Kim, J. Bong, S. Mikael, T.J. Kim, J.C. Williams, Z. Ma, Flexible bottom-gate graphene transistors on Parylene C substrate and the effect of current annealing, Appl. Phys. Lett. 109 (2016), https://doi.org/10.1063/1.4964853.

[23] B. Chamlagain, Q. Li, N.J. Ghimire, H.J. Chuang, M.M. Perera, H. Tu, Y. Xu, M. Pan, D. Xaio, J. Yan, D. Mandrus, Z. Zhou, Mobility improvement and temperature dependence in MoSe2 field-effect transistors on parylene-C substrate, ACS Nano. 8 (2014) 5079–5088, https://doi.org/10.1021/nn501150r.

[24] H. Huang, Y. Xu, H.Y. Low, Effects of film thickness on moisture sorption, glass transition temperature and morphology of poly(chloro-p-xylylene) film, Polymer. 46 (2005) 5949–5955, https://doi.org/10.1016/j.polymer.2005.05.076.

[25] J. Alexander-Webber, A.A. Sagade, A.I. Aria, Z.A. Van Veldhoven, P. Braeuninger-Weimer, R. Wang, A. Cabrero-Vilatela, M.B. Martin, J. Sui, M.R. Connolly, S. Hofmann, Encapsulation of graphene transistors and vertical device integration by interface engineering with atomic layer deposited oxide, 2D Mater. 4 (2017), https://doi.org/10.1088/2053-1583/4/1/011008.

[26] P.L. Levesque, S.S. Sabri, C.M. Aguirre, J. Guillemette, M. Siaj, P. Desjardins, T. Szkopek, R. Martel, Probing charge transfer at surfaces using graphene transistors, Nano Lett. 11 (2011) 132–137, https://doi.org/10.1021/nl103015w.

[27] S. Ryu, L. Liu, S. Berciaud, Y.J. Yu, H. Liu, P. Kim, G.W. Flynn, L.E. Brus, Atmospheric oxygen binding and hole doping in deformed graphene on a SiO2 substrate, Nano Lett. 10 (2010) 4944–4951, https://doi.org/10.1021/nl1029607.

[28] F. Pizzocchero, L. Gammelgaard, B.S. Jessen, J.M. Caridad, L. Wang, J. Hone, P. BÃ¸ggild, T.J. Booth, The hot pick-up technique for batch assembly of van der Waals heterostructures, Nat. Commun. 7 (2016). doi:10.1038/ncomms11894.

[29] C.R. Dean, A.F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. Kim, K.L. Shepard, J. Hone, Boron nitride substrates for high-quality graphene electronics, Nat. Nanotechnol. 5 (2010) 722–726, https://doi.org/10.1038/nnano.2010.172.

[30] J.D. Thomsen, T. Gunst, S.S. Gregersen, L. Gammelgaard, B.S. Jessen, D. M. Mackenzie, K. Watanabe, T. Taniguchi, P. Bøggild, T.J. Booth, Suppression of intrinsic roughness in encapsulated graphene, Phys. Rev. B. 96 (2017), 014101.

[31] A. Cabrero-Vilatela, J. Alexander-Webber, A.A. Sagade, A.I. Aria, P. Braeuninger-Weimer, M.B. Martin, R.S. Weatherup, S. Hofmann, Atomic layer deposited oxide films as protective interface layers for integrated graphene transfer, Nanotechnology. 28 (2017), https://doi.org/10.1088/1361-6528/aa940c.

[32] A.A. Sagade, D. Neumaier, D. Schall, M. Otto, A. Pesquera, A. Centeno, A.Z. Elorza, H. Kurz, Highly air stable passivation of graphene based field effect devices, Nanoscale. 7 (2015) 3558–3564, https://doi.org/10.1039/c4nr07457b.

[33] Y.J. Shin, Y. Wang, H. Huang, G. Kalon, A.T.S. Wee, Z. Shen, C.S. Bhatia, H. Yang, Surface-energy engineering of graphene, Langmuir. 26 (2010) 3798–3802, https://doi.org/10.1021/la100231u.

[34] D.W. Park, S. Mikael, T.H. Chang, S. Gong, Z. Ma, Bottom-gate coplanar graphene transistors with enhanced graphene adhesion on atomic layer deposition Al2O3, Appl. Phys. Lett. 106 (2015), https://doi.org/10.1063/1.4914926.

[35] F. Kafiah, Z. Khan, A. Ibrahim, M. Atieh, T. Laoui, Synthesis of graphene based membranes: Effect of substrate surface properties on monolayer graphene transfer, Materials. 10 (2017), https://doi.org/10.3390/ma10010086.

[36] M. Kim, C. Li, J. Susoma, J. Riikonen, and Lipsanen Harri, Versatile Water-Based Transfer of Large-Area Graphene Films onto Flexible Substrates, MRS Adv. 2 (2017) 3749–3754, https://doi.org/10.1557/adv.2017.565.

[37] L. Wang, I. Meric, P.Y. Huang, Q. Gao, Y. Gao, H. Tran, T. Taniguchi, K. Watanabe, L.M. Campos, D.A. Muller, J. Guo, P. Kim, J. Hone, K.L. Shepard, C.R. Dean, One-dimensional electrical contact to a two-dimensional material, Science. 342 (2013) 614–617, https://doi.org/10.1126/science.1244358.

[38] J. Ortigoza-diaz, K.S. Id, C.L. Id, A. Cobo, T. Hudson, J.Y. Id, A.B. Id, A. W. Hirschberg, E. Meng, Techniques and Considerations in the Microfabrication of Parylene C Microelectromechanical Systems, Micromachines. 9 (2018) 422, https://doi.org/10.3390/mi9090422.

[39] A. Heid, R. Von Metzen, A. Stett, V. Bucher, Examination of dielectric strength of thin Parylene C films under various conditions, Curr. Direct. Biomed. Eng. 2 (2016) 39–41, https://doi.org/10.1515/cdbme-2016-0012.

[40] L. Brancato, D. Decrop, J. Lammertyn, R. Puers, Surface nanostructuring of Parylene-C coatings for blood contacting implants, Materials. 11 (2018) 1–16, https://doi.org/10.3390/ma11071109.

[41] J.J. Shea, Low dielectric constant materials for IC applications [Book Review], IEEE Electr. Insulat. Magaz. 20 (2004) 53–54, https://doi.org/10.1109/MEI.2004.1283280.

[42] V. Radun, R.P. von Metzen, T. Stieglitz, V. Bucher, A. Stett, Evaluation of adhesion promoters for Parylene C on gold metallization, Curr. Direct. Biomed. Eng. 1 (2015) 493–497, https://doi.org/10.1515/cdbme-2015-0118.

[43] X.C. Ong, G.K. Fedder, P.J. Gilgunn, Modulation of Parylene-C to silicon adhesion using HMDS priming, J. Micromech. Microeng. 24 (2014), https://doi.org/10.1088/0960-1317/24/10/105001.

[44] L. Gammelgaard, J.M. Caridad, A. Cagliani, D.M.A. Mackenzie, D.H. Petersen, T.J. Booth, P. Bøggild, Graphene transport properties upon exposure to PMMA processing and heat treatments Graphene transport properties upon exposure to PMMA processing and heat treatments, 2D Mater. 1 (2014). doi:10.1088/2053-1583/1/3/035005.

[45] M. Jose, M.A. David, S. Bjarke, J. Timothy, High-quality graphene flakes exfoliated on a flat hydrophobic polymer High-quality graphene flakes exfoliated on a flat hydrophobic polymer, Appl. Phys. Lett. 112 (2018), https://doi.org/10.1063/1.5009168.

[46] H.S. Song, S.L. Li, H. Miyazaki, S. Sato, K. Hayashi, A. Yamada, N. Yokoyama, K. Tsukagoshi, Origin of the relatively low transport mobility of graphene grown through chemical vapor deposition, Scient. Rep. 2 (2012) 1–6.

[47] I.d.O. Martins, Parylene C as substrate, dielectric and encapsulation for flexible electronics applications, 2017.

[48] Y.J. Kim, Y.G. Lee, U. Jung, S. Lee, S.K. Lee, B.H. Lee, A facile process to achieve hysteresis-free and fully stabilized graphene field-effect transistors, Nanoscale. 7 (2015) 4013–4019.

[49] D.M.A. Mackenzie, P.R. Whelan, P. Bøggild, P.U. Jepsen, A. Redo-Sanchez, D. Etayo, N. Fabricius, D.H. Petersen, Quality assessment of terahertz time-domain spectroscopy transmission and reflection modes for graphene conductivity mapping, Opt. Exp. 26 (2018) 9220–9229, https://doi.org/10.1364/OE.26.009220.

[50] J. Riikonen, W. Kim, C. Li, O. Svensk, S. Arpiainen, M. Kainlauri, H. Lipsanen, Photo-thermal chemical vapor deposition of graphene on copper, Carbon. 62 (2013) 43–50, https://doi.org/10.1016/j.carbon.2013.05.050.

[51] D.M. Mackenzie, K. Smistrup, P.R. Whelan, B. Luo, A. Shivayogimath, T. Nielsen, D.H. Petersen, S.A. Messina, P. Bøggild, Batch fabrication of nanopatterned graphene devices via nanoimprint lithography, Appl. Phys. Lett. 111 (2017), 193103.