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Injection Locking of Ring Oscillators With Digitally Controlled Delay Modulation

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***Abstract*—A digital-friendly approach to implement injection-locked ring oscillators is proposed. We show that lock can be achieved by dynamically switching the delay of a delay element in a ring oscillator. A logic gate that generates the control signal for switching the delay, together with a one-bit controlled oscillator, inherently realizes a locking mechanism. Measurement results from a prototype circuit fabricated with a 28 nm CMOS process demonstrate the feasibility of the concept. The circuit with a measured lock range of 2.4-3.7 GHz occupies an area of 0.00043 mm^2 and consumes 0.18 mW power.**

***Index Terms*—Injection locking, ring oscillator, lock range, phase noise, digital, switched delay, delay modulation.**

I. Introduction

Locking the frequency and phase of an electrical oscillator to those of a reference signal has a wide range of applications including accurate timing generation, reduction of phase noise in oscillators, quadrature signal generation in communication transceivers, and synchronization of LO and clock domains. A common way to achieve lock is by embedding the target oscillator in a feedback system that locks the oscillator to the reference signal, thus forming a phase-locked loop (PLL). Alternatively, lock can also be achieved with injection locking where a suitable means of coupling between the oscillator and the reference signal source pulls the oscillator to follow the frequency and phase of the reference [1], [2]. Injection locking typically enables simpler design, higher frequency of operation, and better energy efficiency, leading to its use in numerous applications like clock generation in systems-on-chip, and high-speed frequency division and multiplication.

Ring oscillator is easy to design and integrate, and occupies a significantly smaller silicon area compared to an LC-tank oscillator. It consists of a ring of inverting delay stages where the net phase shift along the ring is π. The integral relationship between the frequency and phase of an oscillator, together with the multi-phase output inherent to the ring structure, enables the use of a ring oscillator as a continuous-time lossless integrator and as a time-domain signal quantizer. As a result of such interesting properties that present a host of opportunities in analog signal processing, the research interest in ring oscillators has sharply increased recently thereby extending its use to digital-intensive analog-to-digital converters (ADCs) [3], time-to-digital converters, and all-digital PLLs [4].

In this work, we seek digital-friendly ways to implement injection-locked ring oscillators due to our interest in developing circuit techniques for digital-intensive analog/mixed-mode signal processing systems that employ time as a medium for signal representation. A method to implement injection-locked ring oscillators is presented, where lock is achieved by dynamically switching the delay of a delay stage in the ring. It is distinctly different from conventional implementation methods like driving a circuit node with multiple drive circuits, edge insertion, current modulation, impedance modulation, or coupling with passive elements.

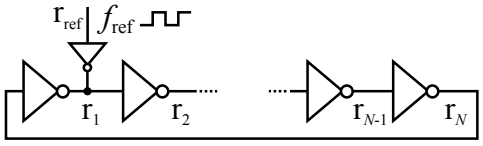

Fig. 1. Multi-drive injection in a single-ended ring oscillator.

The technique can be implemented exclusively with logic gates, enabling design automation with the computer-aided design (CAD) framework available for digital design besides taking full advantage of the benefits offered by technology scaling to deliver improved speed, area efficiency, and energy efficiency as the feature-size reduces. Further, the technique provides a means to realize locking systems with minimal hardware consuming a small area and low power. A prototype circuit is fabricated in a 28 nm CMOS process to demonstrate the feasibility of the concept. The measurement results show that the circuit locks well to the reference signal. The circuit with a measured lock range of 2.4-3.7 GHz occupies 0.00043 mm^2 and consumes 0.18 mW of power.

The remaining part of the paper is organized as follows. Section II briefly reviews existing techniques to implement injection locking of ring oscillators. Section III presents the proposed locking technique. Section IV describes the prototype circuit and simulation results. Section V presents the measurement results and section VI concludes the paper.

II. Injection locking ring oscillators: Prior art

The phenomenon of coupling, pulling, and locking of oscillators is well-studied in general [1], [2], [5], while an understanding about the trade-offs in implementation techniques specific to a ring oscillator is still evolving [6], [7]. In this section, we briefly review the major implementation techniques applied to injection-lock a ring oscillator to a reference signal, to place the proposed technique in perspective.

Multi-drive injection refers to implementations where the reference signal is driven into a circuit node of the target

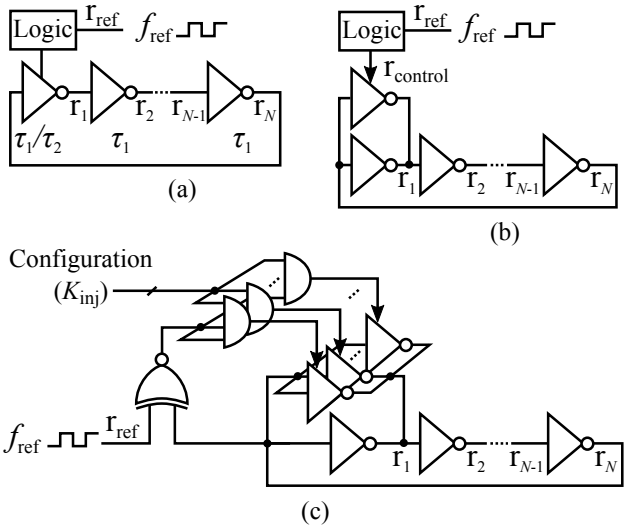

Fig. 2. The proposed method of injection-locking: (a) the abstract idea where one delay element in the ring has a switchable delay, (b) a circuit realization where the switched delay stage is implemented with a tristate inverter parallel-connected to an inverter in the ring, and (c) the implemented circuit with configurable injection strength.

oscillator in the form of current or charge. A circuit realization is shown in Fig. 1 with the example of an N-stage single-ended ring oscillator. f_{ref} represents the reference signal. The inverter driven by the reference signal typically has weaker drive-strength than the inverters in the ring.

Passive coupling involves transfer of energy between a circuit node in the oscillator and the reference signal source by means of a passive circuit element. An example can be obtained by replacing the inverter driven by the reference signal in Fig. 1 with a capacitor.

Current modulation is another method of injection where a current in the oscillator is modulated with a transconductance or a similar active circuit element. A common example is the application of the reference signal into the tail current of a differential pair that realizes the delay stage of a differential ring oscillator [8].

Impedance modulation is yet another technique where reference signal is injected into the oscillator by using the signal to modulate the impedance between different circuit nodes in the oscillator [9]. When the signal fed to the injection terminal is a narrow digital pulse, the technique is also referred to as pulse injection [10].

Edge injection is used to suppress the effect of accumulated jitter in a free-running ring oscillator by inserting an accurate reference transition periodically into the ring oscillator using a multiplexer circuit [11], [12]. In order to obtain a glitch-free output, the select signal to the multiplexer should be generated by a carefully designed logic that monitors the phase of the reference signal and the ring oscillator.

III. Proposed locking technique

In this work, we propose a digital-friendly approach to implement injection-locked ring oscillators by dynamically switching the delay of the delay stages of the ring in discrete steps, which can be realized entirely with logic gates. The technique is inspired by the observation that the inverter driven by the reference signal in Fig. 1 affects the frequency or phase of the oscillator only when the cyclically propagating transition in the ring reaches node r_1. Further, the net effect of the reference signal drive is a modulation of the delay of the inverter driving the node r_1 depending on the instantaneous phase of the reference signal. We implement the delay modulation with digital circuits instead, thereby eliminating the static power consumption in a multi-drive implementation. The ring oscillator and the reference signal source are assumed to generate square wave outputs.

TABLE I
Truth table for injection locking in ring oscillator

r_N	r_{ref}	r_N - r_1 transition	$r_{control}$
0	0	fast	1
0	1	slow	0
1	0	slow	0
1	1	fast	1

A. Locking with switched delay

We propose to realize a locking ring oscillator by making at least one delay stage dynamically configurable with a one-bit digital input such that its delay can be switched between two values. This is illustrated in Fig. 2 (a) where one delay stage in a ring oscillator can have a delay of either τ_1 or τ_2 depending on the state of the control input, while all other stages have a delay of τ_1. A practical realization where the switched delay is implemented with a tristate inverter parallel-connected to an inverter in the ring is shown in Fig. 2 (b). The switched delay is controlled by a logic depending on the phase difference between the oscillator and the reference signal such that a locking mechanism is realized. We describe the design of the logic in the next subsection.

B. Delay control logic

The effect of the reference signal drive in Fig. 1 on the delay of the inverter driving r_1 depends on whether the inputs to the two inverters driving r_1 are at conflicting logic states or not. The transition is fast when the drive circuits agree on the state to be asserted at r_1, and it is slow when the drive circuits disagree. The possible cases are summarized in Table I. We use this rationale to arrive at the logic to dynamically control the delay in Fig. 2 (a)/(b) so that the switched delay creates a similar impact on the phase of the oscillator. Assuming that the delay between the nodes r_N and r_1 reduces by enabling the tristate inverter in Fig. 2 (b), the logic relating the control signal of the tristate inverter, $r_{control}$, the phase of the oscillator given by the state of r_N, and the node with reference signal, r_{ref}, can be obtained as

$$r_{control} = \overline{r_N \oplus r_{ref}}. \quad (1)$$

The respective states of $r_{control}$ are given in Table I. Hence, the logic block in Fig. 2 (b) can be replaced with a two-input XNOR gate with the inputs connected to r_{ref} and r_N respectively.

C. Injection strength

The injection strength is usually measured as the reference signal energy injected into the oscillator. Since the proposed technique injects the reference signal as a variation in delay, we define a delay-based injection factor, $K_{inj,\tau}$, as the ratio of the variation in the delay of the switched delay element to the nominal delay of a delay element as given below.

$$K_{inj,\tau} = \frac{\tau_1 - \tau_2}{\tau_1} \tag{2}$$

It is assumed that the delay τ_2 in the model in Fig. 2 (a) corresponds to the delay between nodes r_N and r_1 when the tristate inverter in Fig. 2 (b) is enabled. That is, $\tau_2 < \tau_1$.

D. Power saving

In the reference circuit in (Fig. 1), there is static power consumption due to the short-circuit current flowing from supply to ground when the two inverters driving node r_1 have conflicting inputs. It is observed that the inverters are driven by conflicting inputs nearly half of the time when the oscillator is locked, resulting in high power consumption. The proposed method of locking completely eliminates the static power consumption while implementing essentially the same signal processing, providing significantly higher energy-efficiency compared to the reference circuit.

IV. Prototype Circuit

A test circuit as shown in Fig. 2 (c) is designed with a 28 nm CMOS process to study injection locking with switched delay. As discussed in section III-B, the control signal for dynamically switching the delay is generated by an XNOR gate with inputs connected to r_N and r_1. An array of tristate inverters is used to vary the injection strength, K_{inj}. The output from the XNOR gate is connected to the enable inputs of the tristate inverters through an array of AND gates such that the number of operational tristate inverters can be configured with a digital input. N is set to 13. Transistor-level simulations are used to verify the feasibility of the proposed locking technique.

According to post-layout parasitic extracted simulation, τ_1 = 40 ps and the minimum configurable value for τ_2 is 14 ps. The free-running frequency of the oscillator for $\tau_2 = \tau_1$ (no injection) is around 3.2 GHz. In order to study the locking behavior, the reference frequency f_{ref} is swept over a range around the free-running frequency of the oscillator. The sweep is performed by running a large number of transient simulations where f_{ref} is progressively incremented in small steps. To reduce the resulting large simulation time, the pre-layout circuit with added post-layout equivalent lumped capacitors is used. The variation of the oscillator frequency as a function of f_{ref} for a certain injection strength is shown in Fig. 3. It can be seen that f_{out} gets pulled toward f_{ref} when the difference between them is large while f_{out} locks to f_{ref} over a certain range of frequencies when the difference is small, demonstrating locking of the oscillator.

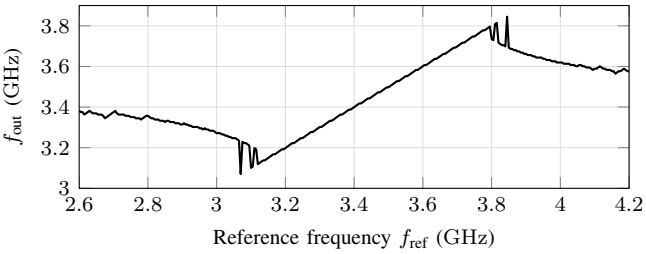

Fig. 3. Simulated locking behavior.

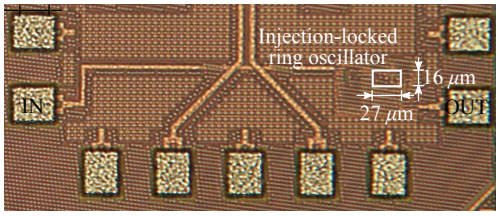

Fig. 4. Micrograph of the chip.

The power saving discussed in section III-D is evaluated by comparing the power consumption of the drive and control circuitry at node r_1 in the proposed circuit and in a reference multi-drive injection circuit (Fig. 1) with comparable drive strengths. The static power observed in the reference circuit is absent in the proposed circuit as expected, reducing the power consumption by around 80%.

V. Measurement Results

The chip micrograph of the test circuit fabricated in 28 nm CMOS is shown in Fig. 4. The circuit occupies a very small area of 0.00043 mm^2. It is measured by directly probing the bare die. The free-running frequency of the oscillator when $\tau_2 = \tau_1$ (no injection) is around 2.5 GHz.

Fig. 5 shows the locking behavior of the oscillator, where measured f_{out} is plotted against f_{ref}. Fig. 6 plots the measured lock range of the circuit as a function of the injection strength. Since the delay between r_N and r_1 could not directly be measured, injection strength is computed in terms of frequency as $K_{inj,f} = \frac{f_2 - f_1}{f_1}$ where f_1 is the free-running frequency of the oscillator when no tristate inverters are connected ($K_{inj,\tau} = 0$, $\tau_2 = \tau_1$), and f_2 is the free-running frequency when tristate inverter of a certain strength is connected and no reference signal is applied. The lock range linearly increases with $K_{inj,f}$, with a maximum range of 2.4-3.7 GHz. The asymmetry of the lock range around f_1=2.53 GHz is due to the fact that only τ_2 changes its value while τ_1 remains constant when $K_{inj,\tau}$ is varied.

Fig. 7 presents the measured phase noise of the output for the free-running and the locked cases. A wide-range spectrum of the output with frequencies from around DC up to the second harmonic of the reference signal when the oscillator is locked is shown in Fig. 8. The spectrum is free of spurious tones since the locking happens to the first harmonic of the

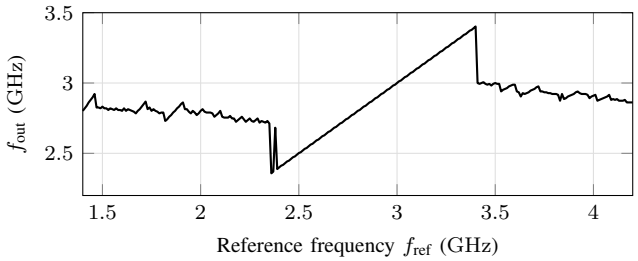

Fig. 5. Measured demonstration of locking with switched delay.

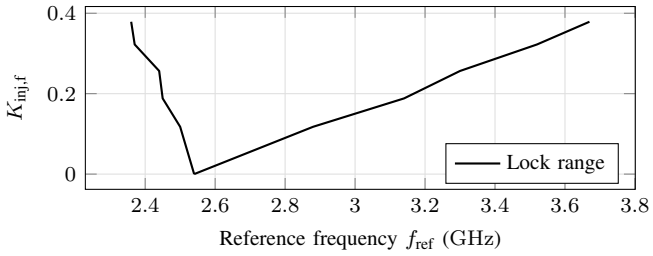

Fig. 6. Measured variation of lock range as a function of injection strength.

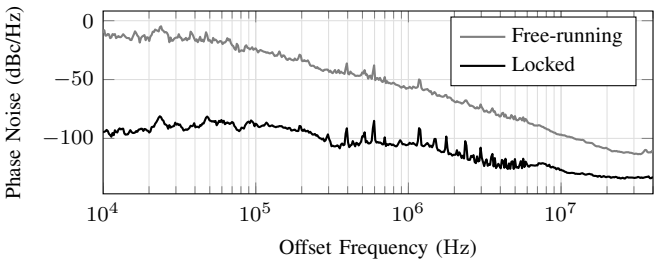

Fig. 7. Measured phase noise with and without lock.

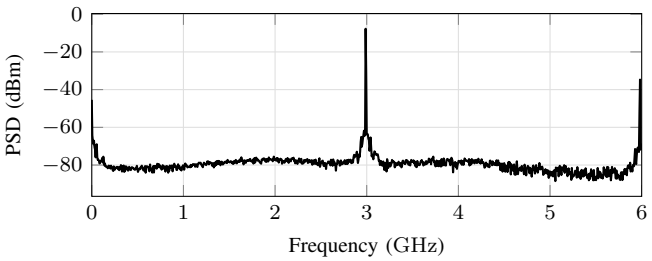

Fig. 8. Spectrum from DC up to the second harmonic when the oscillator is locked, free from spurious tones.

oscillator and the concept does not introduce any additional periodicity. The measured performance of the injection-locked oscillator is summarized in Table II. Power consumption is low at 0.18 mW. When locked, the phase noise at 1 MHz offset is -105 dBc/Hz and the integrated phase noise over the range of 10 kHz-40 MHz is 1.52 ps. Since the circuit is measured with first-harmonic locking with the goal of demonstrating the feasibility of locking, we could not find works that can be fairly compared with the measured performance.

TABLE II
MEASURED PERFORMANCE OF INJECTION LOCKING

Metric	Performance
Lock range (GHz)	2.4 - 3.7
Phase noise (dBc/Hz @1 MHz)	-105
Integrated phase noise (ps) [10 kHz - 40 MHz]	1.52
Area (mm^2)	0.00043
Power (mW)	0.18
Technology	28 nm

VI. Conclusion

A digital-friendly technique to implement injection-locked ring oscillators is proposed, where lock is achieved by dynamically switching the delay of a delay stage in a ring oscillator. Measured results from a prototype circuit fabricated with a 28 nm CMOS process show the feasibility of the concept. The circuit has a lock range of 2.4-3.7 GHz while occupying an area of 0.00043 mm^2 and consuming 0.18 mW of power. The technique enables the design of highly area- and energy-efficient frequency-locked ring oscillators.

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